DATA SHEET

VES1820X
Single chip DVB-C channel receiver

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

FEATURES

- 16/32/64/128/256 QAM demodulator (DVB-C compatible : ETS 300-429).
- On chip 9-bit ADC.
- On chip PLL for crystal frequency multiplication.
- Digital down conversion.
- Half Nyquist filters (roll off = 15 %).
- Automatic gain control PWM output (AGC).
- Symbol timing recovery, with programmable second order loop filter.
- Variable symbol rate capability from SACLK/64 to SACLK/4
  (SACLK max = 36 MHz)
- Programmable anti-aliasing filters.
- Full digital carrier recovery loop.
- Carrier acquisition range up to 8 % of symbol rate.
- Integrated adaptative equalizer (Linear Transversal Equalizer or Decision Feedback Equalizer).
- On chip FEC decoder (Deinterleaver & RS decoder), full DVB-C compliant.
- DVB compatible differential decoding and mapping.
- Parallel or serial transport stream interface.
- I2C bus interface, for easy control.
- CMOS 0.35µm technology.

APPLICATIONS

- DVB-C fully compatible.
- Digital data transmission using QAM modulations.
- Cable demodulation.
- Cable modems
- MMDS (ETS 300-429).

DESCRIPTION

The VES1820X is a single chip channel receiver for 16, 32, 64, 128 and 256-QAM modulated signals. The device interfaces directly to the IF signal, which is sampled by a 9-bit AD converter.

The VES1820X performs the clock and the carrier recovery functions. The digital loop filters for both clock and carrier recovery are programmable in order to optimize their characteristics according to the current application.

After base band conversion, equalization filters are used for echo cancellation in cable applications. These filters are configured as T-spaced transversal equalizer or DFE equalizer, so that the system performance can be optimized according to the network characteristics. A proprietary equalization algorithm, independent of carrier offset, is achieved in order to assist carrier recovery. Then a decision directed algorithm takes place, to achieve final equalization convergence.

The VES1820X implements a FORNEY convolutional deinterleaver of depth 12 blocks and a Reed-Solomon decoder which corrects up to 8 erroneous bytes. The deinterleaver and the RS decoder are automatically synchronized thanks to the frame synchronization algorithm which uses the MPEG2 sync byte. Finally descrambling according to DVB-C standard, is achieved at the Reed Solomon output. This device is controlled via an I2C bus.

Designed in 0.35 µm CMOS technology and housed in a 100 pin MQFP package, the VES1820X operates over the commercial temperature range.

FIGURE 1 : FUNCTIONAL BLOCK DIAGRAM

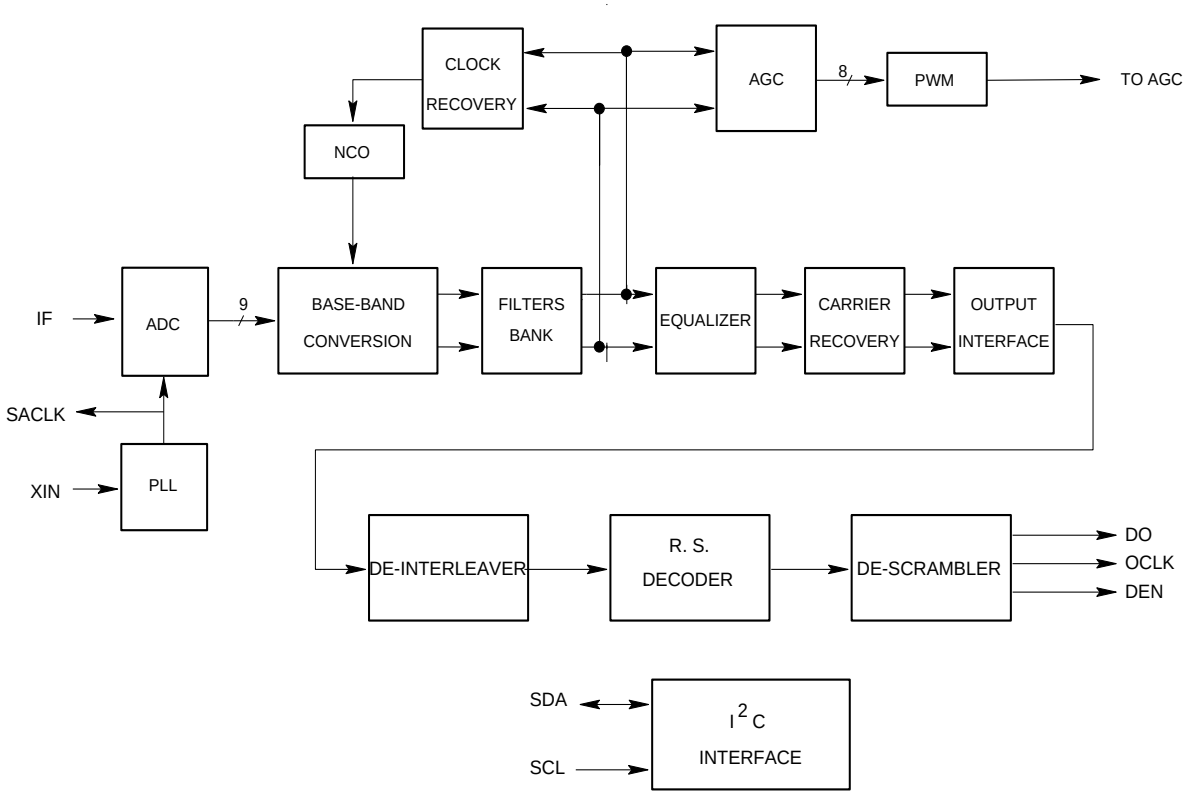


TABLE 1 : ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Ambient operating temperature : Ta	0	70	°C
DC supply voltage	- 0.5	+ 4.1	V
DC Input voltage	- 0.5	VDD + 0.5	V
DC Input Current		± 20	mA
Lead Temperature		+300	°C
Junction Temperature		+150	°C

Stresses above the absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 2 : RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD	Digital supply voltage	3.14	3.3	3.46	V	3.3V ±5%
VCC	5V supply	4.75	5	5.25	V	pin 17
Ta	Operating temperature	0		70	°C	Ambient temperature
VIH[1]	High-level input voltage	2		VCC + 0.3	V	TTL input
VIL	Low-level input voltage	-0.5		0.8	V	TTL input
VOH[2]	High-level output voltage	VDD -0.1 2.4			V	@ IOH = -0.8 mA @ IOH = + 2mA
VOL[2]	Low-level output voltage			0.1 0.4	V	@ IOL = 0.8 mA @ IOL = + 2mA
IDD	Supply current		200		mA	@XIN = 57.84Mhz Symbol Rate =6Mbd
CIN	Input capacitance		15		pF	
COUT	Output capacitance		15		pF	
VD2, VD3, VD4	Analog supply voltage	3.14	3.3	3.46	V	3.3V ± 5%
VIP	Positive analog input		0.5		V	
VIM	Negative analog input		-0.5		V	

[1] All inputs are 5V tolerant
[2] IOH, IOL = ± 4mA only for pins SACLK, OCLK, SDA, CTRL1, CTRL2, IT

FUNCTIONAL DESCRIPTION

- **ADC**
  The VES1820X implements a 9-bit analog to digital converter. No external voltage references are required to use the ADC.

- **PLL**
  The VES1820X implements a PLL used as clock multiplier by 1, 2, 3, 4, 5, 6, 7 or 8, so that the crystal can be low frequency (fundamental tone).

- **DOWN CONVERTER AND NYQUIST FILTERS**
  The digital down converter performs the down conversion of the bandpass input signal into the 2 classical quadrature I & Q channels. Then these two signals are passed through anti-alias filters and through a half Nyquist filter having a fixed roll-off of 0.15. The digital filter gives a stop band attenuation of more than 40 dB.

- **EQUALIZER**
  After Nyquist filtering, the signal is fed to an equalization filter, for echo cancellation. This equalizer can be configured as either a transversal Equalizer or a decision feedback equalizer. The following table shows some echos configuration that the VES1820X corrects with an equivalent degradation of less than 1dB @ BER = 10^{-4}.

DELAY (nS)	AMPLITUDE (dB)	PHASE
50	-10	worst
150 and 800	-12 and -20	worst
1600	-20	worst

- **CARRIER RECOVERY**
  The carrier synchronizer implements a fully digital algorithm allowing to recover carrier frequency offsets up to ± 8 % symbol rate. A phase error detector followed by a programmable second order loop filter provides an estimation of the carrier phase, to compensate the input carrier frequency offset.

- **CLOCK RECOVERY**
  A timing error detector implements an application of Gardner algorithm for digital clock recovery.
  The resulting error is fed to a programmable second order loop filter, which provides a 8-bit command to the NCO block. This one allows to determine the right sampling time instant of the input signal.

- **AUTOMATIC GAIN CONTROL**
  An estimation of input signal magnitude is performed and compared to a threshold value which is programmable via the microcontroller interface. The resulting error is then filtered to produce an 10-bit command which is then PWM encoded and provided on pin VAGC. The PWM signal can be passed through a single RC filter to control the input gain amplifier.

- **OUTPUT INTERFACE**
  After carrier recovery, the demodulated output symbol must be decoded according to the constellation diagram given by DVB standard for 16, 32, 64, 128 and 256 QAM. The resulting symbols are then differentially decoded (DVB compliant) and serially provided to the FEC part.

- **BLOCK SYNCHRONIZATION**
  At demodulator output, the length of some error bursts may exceed that which can be reliably corrected by the Reed-Solomon decoder. The implemented de-interleaving is a convolutional one (Forney) of depth 12. The first operation consists in synchronizing the de-interleaver. This is accomplished by detecting α consecutive MPEG2 sync words (or $\overline{\text{sync}}$) which are present as the first byte of each packet.

Next, the RAM memory associated with the deinterleaver fills up and the first deinterleaved bytes are provided to the input of the Reed-Solomon decoder. The state machine of the de-interleaver goes to the control phase which counts β consecutive missed MPEG2 sync words (or $\overline{\text{sync}}$) before declaring the system desynchronized and going back to the synchronization phase. α and β are programmable through the I2C interface.
When the inverted sync word is detected at the input of the de-interleaver, the bytes provided to the Reed-Solomon decoder are inverted at the output of the deinterleaver.

- **REED-SOLOMON DECODER**

The Reed-Solomon decoder decodes the symbol stream from the de-interleaver according to the (204, 188) shortened Reed-Solomon code. Synchronization to Reed-Solomon code is defined over the finite Galois field GF (2^8). The field generator polynomial is given by :

$$G(x) = \prod_{i=0}^{15} (x + \alpha^i)$$

This Reed-Solomon decoder corrects up to eight erroneous symbols in each block. When the correction capability of the decoder is exceeded, the block is not changed and is provided as it has been entered. In this case the flag UNCOR is set and the MSB of the second byte in the MPEG2 frame is forced to one (error indicator). The correction capability of the RS decoder can be inhibited.

- **DESCRAMBLER**

In order to comply with energy dispersal requirements of radio transmission regulations and to ensure adequate binary transitions, the MPEG2 frames are scrambled at the encoder side. Dual operation is achieved at the output of the Reed-Solomon decoder using the same scrambler/descrambler. The polynomial for the pseudo random binary sequence (PRBS generator is $1 + x^{14} + x^{15}$. The PRBS registers are initialized at the start of every eight transport packets. To provide an initialization signal for the descrambler, the MPEG2 sync byte of the first transport packet is inverted from 47_{16} to $B8_{16}$. When detected, the descrambler is loaded with the initial sequence "100101010000000". The descrambler can be inhibited.

- **INTERFACE**

The VES1820X integrates an I2C interface in slave mode. This I2C interface fulfills the Philips component I2C bus specification.

INPUT - OUTPUT SIGNAL DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CLR#	27	I	The CLR# input is asynchronous and active low, and clears the VES1820X. When CLR# goes low, the circuit immediately enters its RESET mode and normal operation will resume 4 XIN falling edges later after CLR# returned high. The I2C register contents are all initialized to their default values. The minimum width of CLR# at low level is 4 XIN clock periods.
XIN	2	I	XTAL oscillator input pin. Typically a fundamental XTAL oscillator is connected between the XIN and XOUT pins (see typical application on FIGURE 10 page 15). The XTAL frequency MUST be chosen so that the system frequency SYSCLK (= XIN * multiplying factor of the PLL) equals to 1.6 times the tuner output Intermediate Frequency : SYSCLK = 1.6 x IF.
XOUT	3	O	XTAL oscillator output pin. Typically a fundamental XTAL oscillator is connected between the XIN and XOUT pins (see typical application FIGURE 10 page 15).
SACLK	18	O (5V)	Sampling CLocK. This output clock can be fed to an external 9-bit ADC as the sampling clock.SACLK = SYSCLK/2.
FI[8:0]	5,6,7,8,12, 13,14,15,16	I	FI [8:0] is the 9-bit input of the IF signal. FI[8:0] is the output of an external A/D converter. FI[8] is the MSB. When not used, must be tied to ground.
VAGC	20	O (5V)	PWM encoded output signal for AGC. This signal is typically fed to the AGC amplifier through a single RC network (see typical application FIGURE 11 page 16). The maximum signal frequency on VAGC output is XIN/16. AGC information is refreshed every 1024 symbols.
DO[7:0]	46,49,50,51 52,53,54,55	O (3.3V)	Data Output bus . These 8-bit parallel data are the outputs of the VES1820X after demodulation, de-interleaving, RS decoding and de-scrambling. When one of the two possible parallel interfaces is selected (Parameter SERINT=0, index 20_{16}) then DO[7:0] is the transport stream output. When the serial interface is selected (Parameter SERINT=1, index 20_{16}) then the serial output is on pin DO[0] (pin 55).
OCLK	44	O (3.3V)	Output CLock. OCLK is the output clock for the parallel DO[7:0] outputs. OCLK is internally generated depending on which interface is selected.
DEN	45	O (3.3V)	Data ENable : this output signal is high when there is a valid data on output bus DO[7 :0].
UNCOR	42	O (3.3V)	UNCORrectable packet. This output signal is high when the provided packet is uncorrectable (during the 188 bytes of the packet). The uncorrectable packet is not affected by the Reed Solomon decoder, but the MSB of the byte following the sync. byte is forced « 1 » for the MPEG2 process : Error Flag Indicator (if RSI and IEI are set low in the I2C table).
PSYNC	43	O (3.3V)	Pulse SYNChro. This output signal goes high when the sync byte (47_{16}) is provided, then it goes low until the next sync byte. If the serial interface is selected, then PSYNC is high only during the first bit of the sync byte (47_{16}). See FIGURE 8 page 14.
TESTO[16:0]	78,77,76,75,74 71,70,69,68,67 64,63,62,61,60 57,56	O (3.3V)	TESTO [16:0] is 17-bit Test output bus.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
IICDIV[1:0]	21,22	I	IICDIV[1:0] allow to select the frequency of the I2C internal system clock, depending on the crystal frequency. Internal I2C clock is a division of XIN by 2^{IICDIV} and must be between 6 and 20 MHz.
SADDR[1:0]	23,24	I	SADDR[1:0] are the 2 LSBs of the I2C address of the VES1820X. The MSBs are internally set to 00010. Therefore the complete I2C address of the VES1820X is (MSB to LSB) : 0, 0, 0, 1, 0, SADDR[1], SADDR[0].
SDA	26	I/O (5V)	SDA is a bidirectional signal. It is the serial input/output of the I2C internal block. A pull-up resistor (typically 4.7 kΩ) must be connected between SDA and VDD for proper operation (Open Drain output).
SCL	25	I	I2C clock input. SCL should nominally be a square wave with a maximum frequency of 400KHz. SCL is generated by the system I2C master.
TEST	19	I	Test input pin. For normal operation of the VES1820X, TEST must be grounded.
TRST	35	I	Test ReSeT. This active low input signal is used to reset the TAP controller when in boundary scan mode. In normal mode of operation TRST must be set low.
TDO	37	O (5V)	Test Data Out. This is the serial Test output pin used in boundary scan mode. Serial Data are provided on the falling edge of TCK.
TCK	33	I	Test ClocK : an independant clock used to drive the TAP controller when in boundary scan mode. In normal mode of operation, TCK must be grounded.
TDI	34	I	Test Data In. The serial input for Test data and instruction when in boundary scan mode. In normal mode of operation, TDI must be set to GND.
TMS	36	I	Test Mode Select. This input signal provides the logic levels needed to change the TAP controller from state to state. In normal mode of operation, TMS must be set to VDD.
CTRL1	31	I/O (5V)	CTRL1 is equivalent to SDA I/O of VES1820X but can be tri-stated by I2C programmation. It is actually the output of a switch controlled by parameter BYPIIC of register TEST (index $0F_{16}$). CTRL1 is open drain output, and therefore requires an external pull up resistor.
CTRL2	32	O (5V)	CTRL2 can be configured to be a control line output or to output SCL input. This is controlled by parameter BYPIIC of register TEST (index $0F_{16}$). CTRL2 is an open drain output and therefore requires an external pull up resistor.
IT	38	O (5V)	InTerrupt line. This active low output interrupt line can be configured by the I2C interface. See registers ITsel (index 32_{16}) and ITstat (index 33_{16}). IT is an open drain output and therefore requires an external pull up resistor.
FEL	39	O (5V)	By default FEL is a front-end lock indicator. In this case FEL is an open drain output and therefore requires an external pull up resistor. But FEL can also be configured to output a PWM signal, which value can be programmed through the I2C interface (see register PWMREF, index 34_{16}).
VIP	92	I	Positive input to the A/D converter. This pin is DC biased to half-supply through an internal resistor divider (2 x 10kΩ resistors). In order to remain in the range of the ADC, the voltage difference between pins VIP and VIM should be between -0.5 and 0.5 volts.
VIM	91	I	Negative input to the A/D converter. This pin is DC biased to half-supply through an internal resistor divider (2 x 10kΩ resistors). In order to remain in the range of the ADC, the voltage difference between pins VIP and VIM should be between -0.5 and 0.5 volts.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CMCAP	85	I	This pin is connected to a tap point on an internal resistor divider used to create CMO and CMI. An external capacitor of value 0.1µf should be connected between this point and ground to provide good power supply rejection from the positive supply at higher frequencies.
RBIAS	82	I	An external resistor of value 3.3kΩ should be connected between this pin and ground to provide good accurate bias currents for the analog circuits on the ADC.
VREF	88	O	This is the output of an on-chip resistor divider. An external capacitor of value 0.1µf should be connected between this point and ground to provide good power supply rejection from the positive supply at higher frequencies. Reference voltages VREFP and VREFM are derived from the voltage on VREF.
VREFP	87	O	This is a positive voltage reference for the A/D converter. It is derived from the voltage on pin VREF through an on-chip fully-differential amplifier. The voltage on this pin is nominally equal to CMO + 0.25 volts.
VREFM	86	O	This is the negative voltage reference for the A/D converter. It is derived from the voltage on pin VREF through an on-chip fully-differential amplifier. The voltage on this pin is nominally equal to CMO- 0.25 volts.
CMO	84	O	This pin provides the common-mode out voltage for the analog circuits on the ADC. It is the buffered version of a voltage derived from an on-chip resistor devider, and has a nominal value of 0.5 x VD3.
CMI	83	O	This pin provides the common-mode in voltage for the analog circuits on the ADC. It is the buffered version of a voltage derived from an on-chip resistor devider, and has a nominal value of 0.75 x VD3.
VD1	81	I	Power supply input for the digital switching circuitry (3.3 typ).
VS1	80	I	Ground return for the digital switching circuitry.
VD2	94	I	Power supply input for the analog clock drivers (3.3V typ).
VS2	93	I	Ground return for the analog clock drivers.
VD3	89	I	Power supply input for the analog circuits (3.3V typ).
VS3	90	I	Ground return for analog circuits.
VD4	95	I	Power supply input that connects to an n-well guard ring that surrounds the ADC (3.3V typ).
DVCC	96	I	3.3V supply for the digital section of the PLL.
DGND	97	I	Ground connection for the digital section of the PLL.
PLLGND	98	I	Ground connection for the analog section of the PLL.
PLLVCC	99	I	3.3V supply for the analog section of the PLL.
PPLUS	100	I	P-well bias for the analog section of the PLL. Must be tied to 0V.

FIGURE 2 : BLOCK DIAGRAM

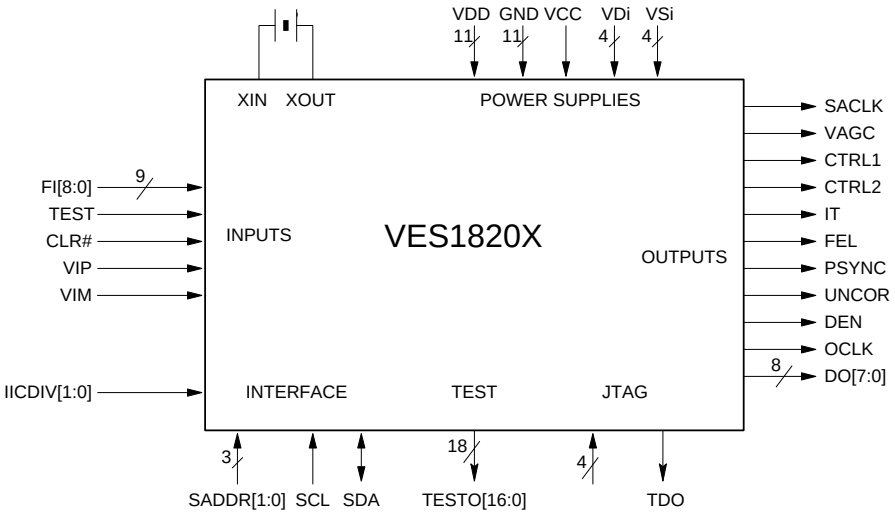


FIGURE 3 : PIN DIAGRAM

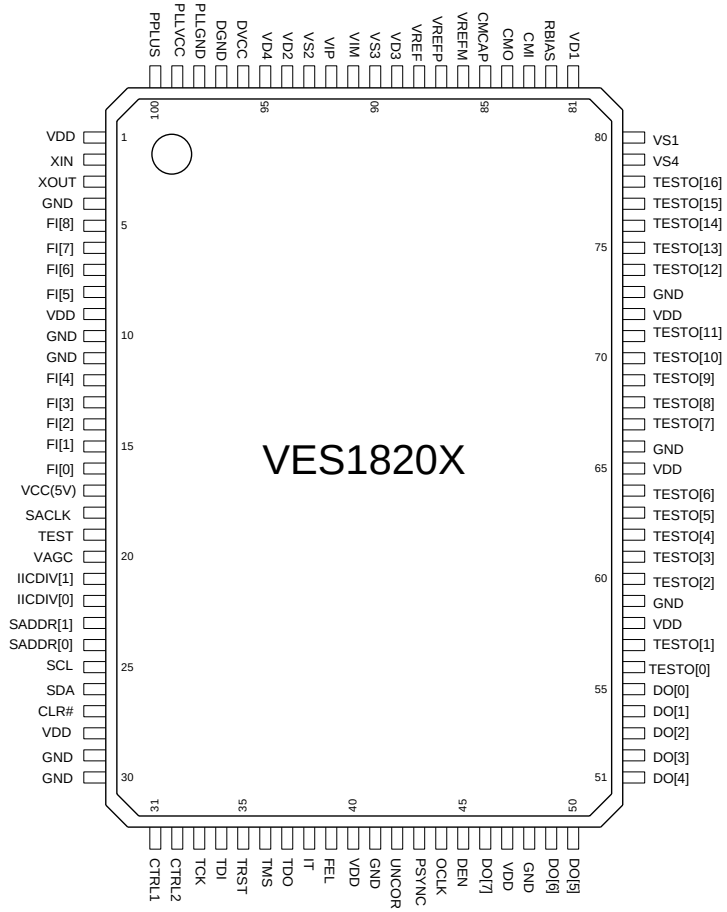


TABLE 3 : PIN DESCRIPTION

Pin	Pin Name	Direction
1	VDD	-
2	XIN	I
3	XOUT	O
4	GND	-
5	FI[8]	I
6	FI[7]	I
7	FI[6]	I
8	FI[5]	I
9	VDD	-
10	GND	-
11	GND	-
12	FI[4]	I
13	FI[3]	I
14	FI[2]	I
15	FI[1]	I
16	FI[0]	I
17	VCC	-
18	SACLK	O
19	TEST	I
20	VAGC	O
21	IICDIV[1]	I
22	IICDIV[1]	I
23	SADDR[1]	I
24	SADDR[0]	I
25	SCL	I
26	SDA	I/O
27	CLR#	I
28	VDD	-
29	GND	-
30	GND	-
31	CTRL1	I/O
32	CTRL2	OD
33	TCK	I

Pin	Pin Name	Direction
34	TDI	I
35	TRST	I
36	TMS	I
37	TDO	OD
38	IT	OD
39	FEL	OD
40	VDD	-
41	GND	-
42	UNCOR	O
43	PSYNC	O
44	OCLK	O
45	DEN	O
46	DO[7]	O
47	VDD	-
48	GND	-
49	DO[6]	O
50	DO[5]	O
51	DO[4]	O
52	DO[3]	O
53	DO[2]	O
54	DO[1]	O
55	DO[0]	O
56	TESTO[0]	O
57	TESTO[1]	O
58	VDD	-
59	GND	-
60	TESTO[2]	O
61	TESTO[3]	O
62	TESTO[4]	O
63	TESTO[5]	O
64	TESTO[6]	O
65	VDD	-
66	GND	-

Pin	Pin Name	Direction
67	TESTO[7]	O
68	TESTO[8]	O
69	TESTO[9]	O
70	TESTO[10]	O
71	TESTO[11]	O
72	VDD	-
73	GND	-
74	TESTO[12]	O
75	TESTO[13]	O
76	TESTO[14]	O
77	TESTO[15]	O
78	TESTO[16]	O
79	VS4	-
80	VS1	-
81	VD1	-
82	RBIAS	I
83	CMI	O
84	CMO	O
85	CMCAP	I
86	VREFM	O
87	VREFP	O
88	VREF	O
89	VD3	-
90	VS3	-
91	VIM	I
92	VIP	I
93	VS2	-
94	VD2	-
95	VD4	-
96	DVCC	-
97	DGND	-
98	PLLGND	-
99	PLLVCC	-
100	PPLUS	-

Notes :
1.All inputs (I) are TTL, 5V tolerant inputs
2.OD are Open Drain 5V outputs, so they must be connected to a pull-up resistor to either VDD or VCC

FIGURE 4 : INPUT TIMING

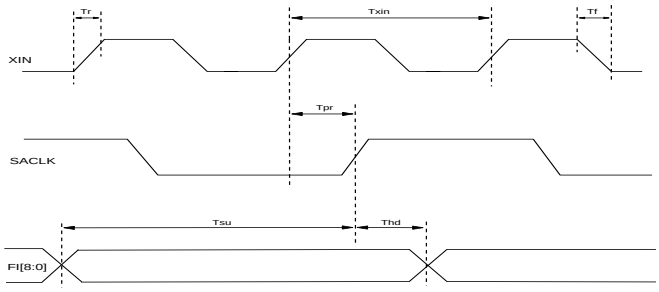


FIGURE 5 : OUTPUT TIMING

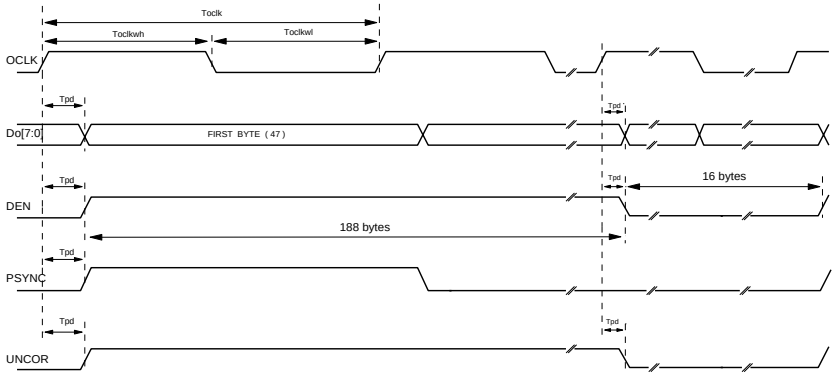
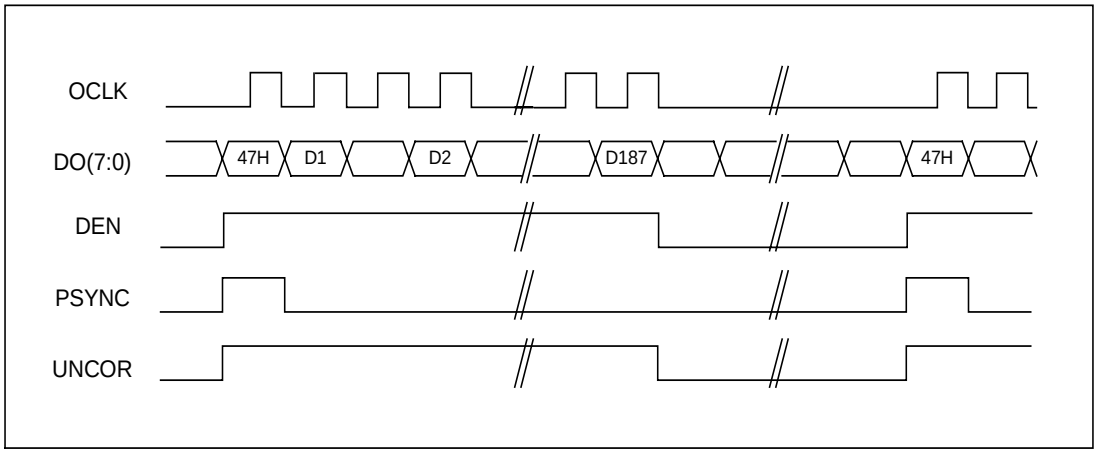


TABLE 4 : TIMING CHARACTERISTICS

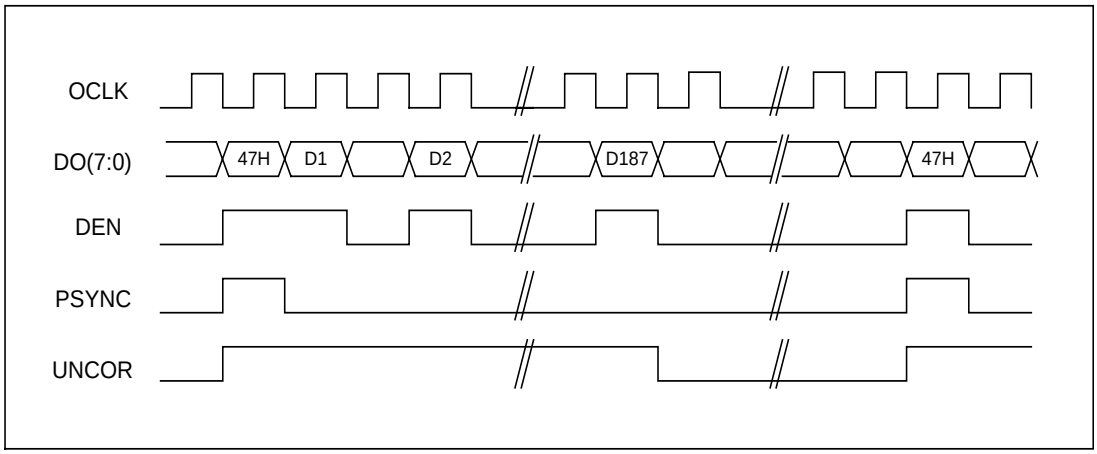
Symbol	Parameter	Min	Max	Unit	Notes
Txin	XIN period	14		nS	
Tr	Rising edge		2	nS	
Tf	Falling edge		2	nS	
Tsu	Set-up time to SACLK rising	3		nS	
Thd	Hold time to SACLK rising	0		nS	
Tpr	Propagation delay from rising edge of XIN	3	8	nS	
Toclk	OCLK period	112		nS	Parallel interface
		14		nS	Serial interface
Toclkwh	OCLK clock high	56		nS	Parallel interface
		7		nS	Serial interface
Toclkwl	OCLK clock low	56		nS	Parallel interface
		7		nS	Serial interface
Tsus	Set-up time to OCLK falling	6		nS	Serial interface
Thds	Hold time to OCLK falling	6		nS	Serial interface
Tpd	Propagation delay from rising edge of OCLK (DO, DEN, PSYNC, UNCOR)	1		nS	CL = 20 pF

FIGURE 6 : PARALLEL OUTPUT INTERFACE MODE A



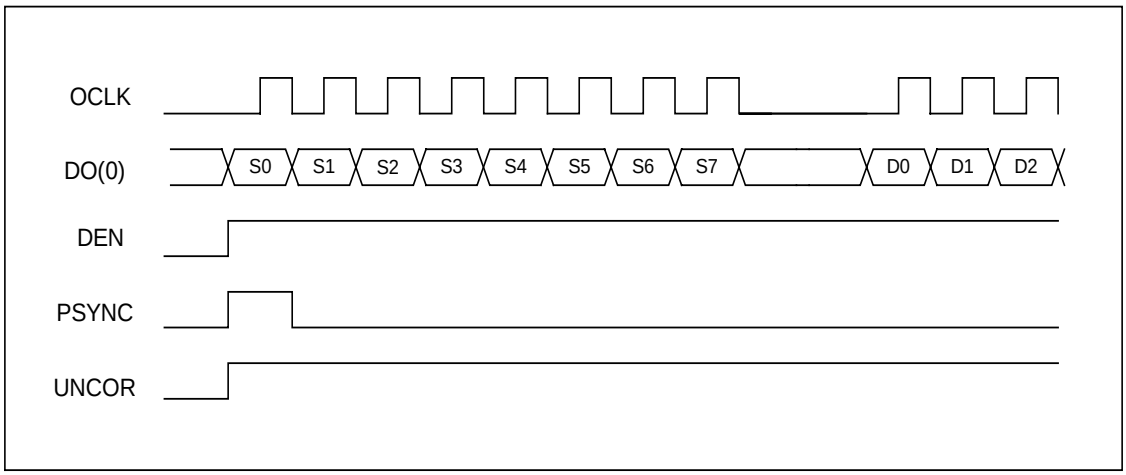
Notes : - OCLK is a jittered clock which average frequency is N*SymbolRate/8, where N is the spectral efficiency of the modulation. The polarity of OCLK is programmable.
- DEN is active high (if PDEN=0) only during the 188 bytes of a packet
- PSYNC is active high (if PPSYNC=0) only during the sync byte (47H)

FIGURE 7 : PARALLEL OUTPUT INTERFACE MODE B



Notes : - OCLK is a division of the sampling clock by a programmable factor from 1 to 16. So it is a regular clock which frequency must be greater than N*SymbolRate/8, where N is the spectral efficiency of the modulation. The polarity of OCLK is programmable.
- DEN is active high (if PDEN=0) only during the valid bytes
- PSYNC is active high (if PPSYNC=0) only during the sync byte (47H)

FIGURE 8 : SERIAL OUTPUT INTERFACE



Notes : - OCLK is a jittered clock with average frequency N*SymbolRate, where N is the spectral efficiency of the modulation. The polarity of OCLK is programmable.
- DEN is active high (if PDEN=0) only during the 1504 bits of a packet
- PSYNC is active high (if PPSYNC=0) only during the first bit of the sync byte (47H)
- The serialization of the output bytes can be either MSB first or LSB first

TYPICAL APPLICATION

FIGURE 9 : FRONT END RECEIVER SCHEMATIC

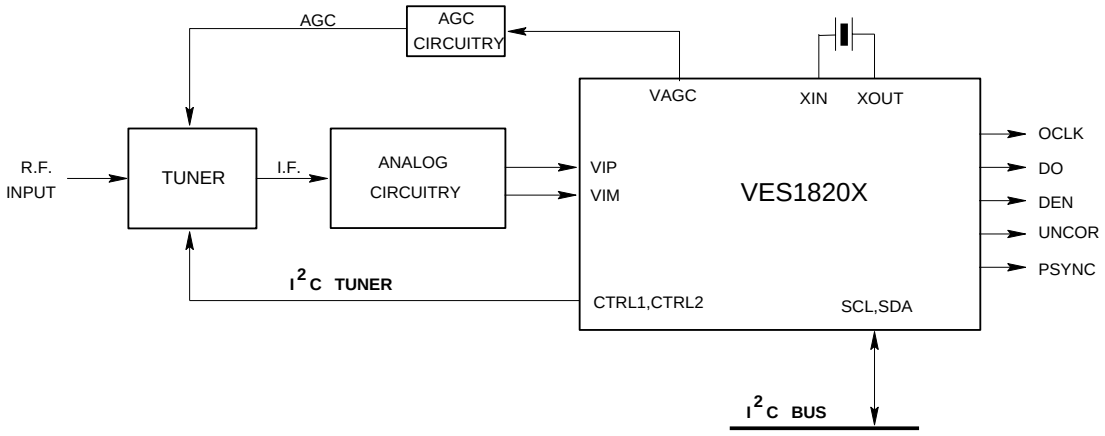
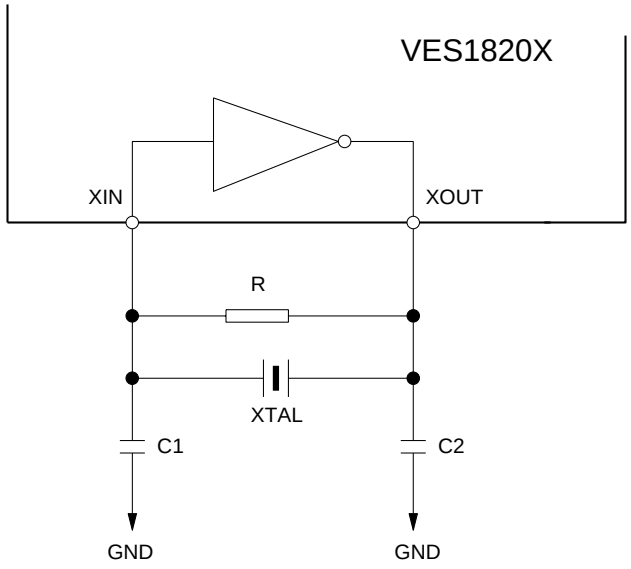
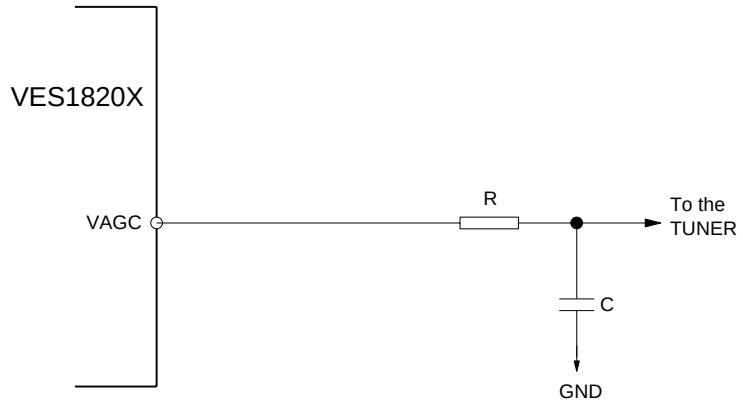


FIGURE 10 : XTAL OSCILLATOR



Notes : - Typical XTAL is on fundamental frequency
- Values of passive components are dependant on XTAL manufacturer.

FIGURE 11 : EXTERNAL AGC CIRCUITRY (SELAGC = 0)



Notes : R and C are chosen to verify RS/1024 < Fc <<< XIN/16
with R = 1.5 k• and C = 1nF, Fc#100KHz.

FIGURE 12 : EXTERNAL CIRCUITRY (SELAGC = 1)

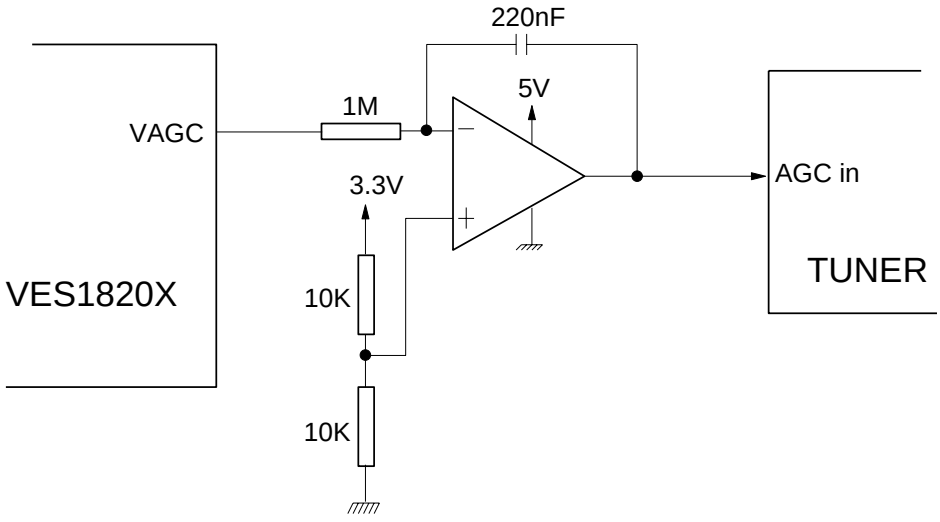
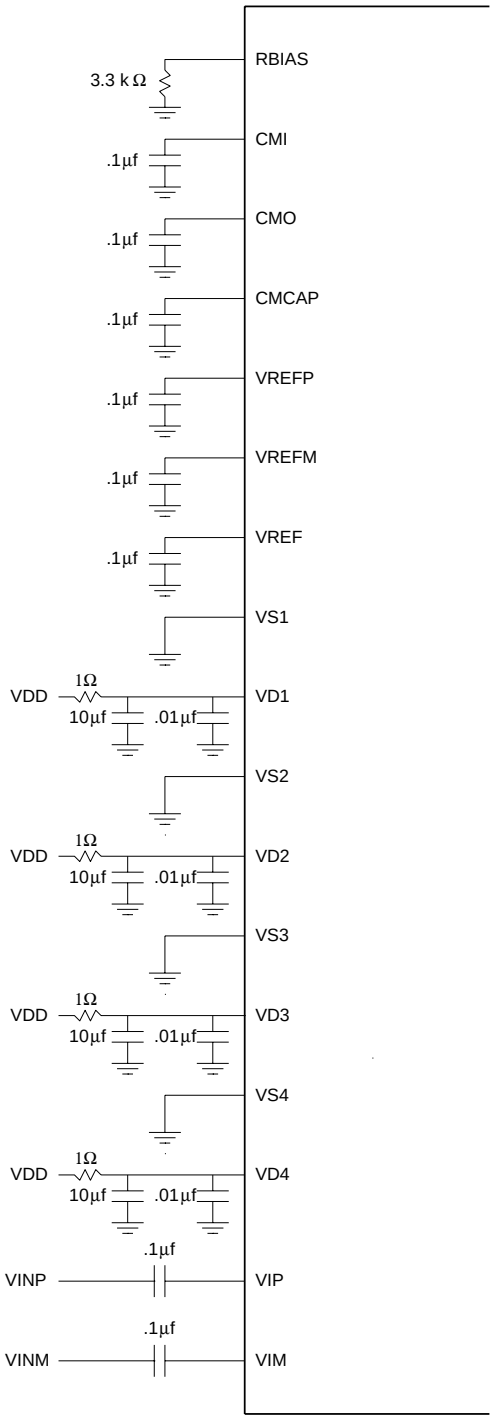
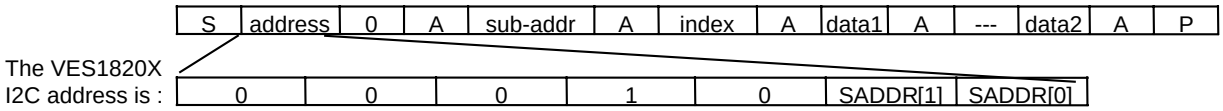


FIGURE 13 : ADC EXTERNAL CONNECTIONS



MICROCONTROLLER SERIAL INTERFACE

• I²C REGISTERS : WRITE MODE

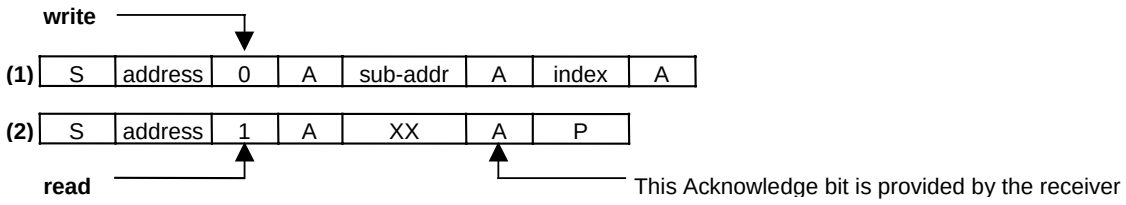


S : start bit
A : acknowledge bit
P : stop bit.

The sub-adress is always: (00)H.
Index is 8-bit format and is defined in table 6.
When data2 is written, data1 is overwritten. Data1 and data2 are 8-bit

• I²C REGISTERS : READ MODE

In this mode of operation you must first (1) write the index value of the register you will then read (2)



Notes : at the end of line (1) there is no stop bit !
Line (2) can start just after the last ackowledge bit of line

TABLE 5 : MICROCONTROLLER INTERFACE REGISTERS

PARAMETER	INDEX HEXA	7(MSB)	6	5	4	3	2	1	0(LSB)	R/W
CONF	00	STDBY	IFS	INVIQ	QAM[2]	QAM[1]	QAM[0]	TRI	CLB	R/W
AGCREF	01	AGCR[7]	AGCR[6]	AGCR[5]	AGCR[4]	AGCR[3]	AGCR[2]	AGCR[1]	AGCR[0]	R/W
AGCCONF	02	FELPWM	ADCSEL	0	1	SELAGC	PWMA	KAGC[1]	KAGC[0]	R/W
CLKCONF	03	NDEC[1]	NDEC[0]	GAIN2	GAIN3	DYN	CLK_C[2]	CLK_C[1]	CLK_C[0]	R/W
CARCONF	04	0	CAR_P[2]	CAR_P[1]	CAR_P[0]	CAR_C[3]	CAR_C[2]	CAR_C[1]	CAR_C[0]	R/W
LOCKTHR	05	LTHR[7]	LTHR[6]	LTHR[5]	LTHR[4]	LTHR[3]	LTHR[2]	LTHR[1]	LTHR[0]	R/W
EQCONF1	06		POSI[2]	POSI[1]	POSI[0]	VALI	ENADAPT	ENEQUAL	DFE	R/W
EQSTEP	07			EQST2[2]	EQST2[1]	EQST2[0]	EQST1[2]	EQST1[1]	EQST1[0]	R/W
MSETH	08	MSETH[7]	MSETH[6]	MSETH[5]	MSETH[4]	MSETH[3]	MSETH[2]	MSETH[1]	MSETH[0]	R/W
AREF	09	AREF[7]	AREF[6]	AREF[5]	AREF[4]	AREF[3]	AREF[2]	AREF[1]	AREF[0]	R/W
BDR_LSB	0A	BDR7	BDR[6]	BDR5	BDR4	BDR3	BDR2	BDR1	BDR0	R/W
BDR_MID	0B	BDR15	BDR14	BDR13	BDR12	BDR11	BDR10	BDR9	BDR8	R/W
BDR_MSB	0C			BDR21	BDR20	BDR19	BDR18	BDR17	BDR16	R/W
BDR_INV	0D	BDR17	BDR16	BDR15	BDR14	BDR13	BDR12	BDR11	BDR10	R/W
GAIN	0E	GNYQ[2]	GNYQ[1]	GNYQ[0]	SFIL	GLPF[1]	GLPF[0]	SSAT[1]	SSAT[0]	R/W
TEST	0F	BYPIIC	CTRL2	0	SELOUT[1]	SELOUT[0]	0	0	0	R/W
RSCONF	10	PVBER[1]	PVBER[0]	CLB_UNC	C[1]	C[0]	RSI	DESCI	IEI	R/W
SYNC	11		NODVB	BER[1]	BER[0]	FEL	FSYNC	CARLOCK	EQ_ALGO	R
POLA	12	1	POINT	P/MF	PFEL	PPSYNC	PUNCOR	PDEN	POCLK	R/W
CPT_UNCOR	13		CPTU[6]	CPTU[5]	CPTU[4]	CPTU[3]	CPTU[2]	CPTU[1]	CPTU[0]	R
BER_LSB	14	BER[7]	BER[6]	BER[5]	BER[4]	BER[3]	BER[2]	BER[1]	BER[0]	R
BER_MID	15	BER[15]	BER[14]	BER[13]	BER[12]	BER[11]	BER[10]	BER[9]	BER[8]	R
BER_MSB	16					BER[19]	BER[18]	BER[17]	BER[16]	R
VAGC	17	AGC[7]	AGC[6]	AGC[5]	AGC[4]	AGC[3]	AGC[2]	AGC[1]	AGC[0]	R
MSE	18	MSE[7]	MSE[6]	MSE[5]	MSE[4]	MSE[3]	MSE[2]	MSE[1]	MSE[0]	R
VAFC	19	VAFC[7]	VAFC[6]	VAFC[5]	VAFC[4]	VAFC[3]	VAFC[2]	VAFC[1]	VAFC[0]	R
IDENTITY	1A	0	1	1	1	1	0	1	1	R
ADC	1B						0	PDOWN	PCLK	R/W
EQCONF2	1C			SGNALGO	CTPHASE	CTADAPT	STEPTL[2]	STEPTL[1]	STEPTL[0]	R/W
CKOFFSET	1D	CKOFF[7]	CKOFF[6]	CKOFF[5]	CKOFF[4]	CKOFF[3]	CKOFF[2]	CKOFF[1]	CKOFF[0]	R
PLL	1E		OOLN	OOLCLRN	BYPPLL	PDPLL	DIVSEL[2]	DIVSEL[1]	DIVSEL[0]	R/W
SERINT	20	DIV[3]	DIV[2]	DIV[1]	DIV[0]	PARMOD	SWAP	MSBFIRST	INTSEL	R/W
SATNYQ	21	SATNYQ[7]	SATNYQ[6]	SATNYQ[5]	SATNYQ[4]	SATNYQ[3]	SATNYQ[2]	SATNYQ[1]	SATNYQ[0]	R
SATADC	22	SATADC[7]	SATADC[6]	SATADC[5]	SATADC[4]	SATADC[3]	SATADC[2]	SATADC[1]	SATADC[0]	R
HALFADC	23	HLFADC[7]	HLFADC[6]	HLFADC[5]	HLFADC[4]	HLFADC[3]	HLFADC[2]	HLFADC[1]	HLFADC[0]	R
SATDEC1	24	SDEC1[7]	SDEC1[6]	SDEC1[5]	SDEC1[4]	SDEC1[3]	SDEC1[2]	SDEC1[1]	SDEC1[0]	R
SATDEC2	25	SDEC2[7]	SDEC2[6]	SDEC2[5]	SDEC2[4]	SDEC2[3]	SDEC2[2]	SDEC2[1]	SDEC2[0]	R
SATDEC3	26	SDEC3[7]	SDEC3[6]	SDEC3[5]	SDEC3[4]	SDEC3[3]	SDEC3[3]	SDEC3[2]	SDEC3[1]	R
SATAAF	27	SAAF[7]	SAAF[6]	SAAF[5]	SAAF[4]	SAAF[3]	SAAF[2]	SAAF[1]	SAAF[0]	R
SATTHR	30	STHR[7]	STHR[6]	STHR[5]	STHR[4]	STHR[3]	STHR[2]	STHR[1]	STHR[0]	R/W
HALFTHR	31	HLFTHR[7]	HLFTHR[6]	HLFTHR[5]	HLFTHR[4]	HLFTHR[3]	HLFTHR[2]	HLFTHR[1]	HLFTHR[0]	R/W
ITSEL	32	ITEN	ITSEL[6]	ITSEL[5]	ITSEL[4]	ITSEL[3]	ITSEL[2]	ITSEL[1]	ITSEL[0]	R/W
ITSTAT	33		ITSTAT[6]	ITSTAT[5]	ITSTAT[4]	ITSTAT[3]	ITSTAT[2]	ITSTAT[1]	ITSTAT[0]	R
PWMREF	34	PWMR[7]	PWMR[6]	PWMR[5]	PWMR[4]	PWMR[3]	PWMR[2]	PWMR[1]	PWMR[0]	R/W

LEGEND : DEFAULT STATE = 0 DEFAULT STATE = 1

DESCRIPTION OF INTERNAL REGISTERS

1. CONF 00_{16} READ/WRITE

CLB — The CLB signal clears the VES1820X through the I2C interface (soft reset). To clear the VES1820X, first write CLB = 0 followed by CLB = 1. This soft reset will not affect the internal I2C registers contents.

TRI — When TRI is set to "1", all VES1820X outputs are tristated.
When TRI = 0 (default value) all outputs are active.

QAM[2:0] — QAM[2:0] indicates the modulation type according to the following table :

QAM[2:0]	Modulation
000	16-QAM
001	32-QAM
010	64-QAM (default)
011	128-QAM (DVB)
100	256-QAM
111	128-QAM (new mapping)

INVIQ — When INVIQ=1, I and Q internal base-band signals are swapped to match a spectral inversion. The default is INVIQ=0, no swap.

IFS — IFS determines if the input signal, FI[8:0] is interpreted in offset binary (IFS = 0, default) or in 2's complement (IFS = 1). It must be set to 1 when internal ADC is used.

STDBY — When STDBY is set to "1" the VES1820X enters a StanD-BY mode and its power consumption is reduced to TBD. The default value is STDBY = "0" which means that the VES1820X is active.

2. AGCREF 01_{16} READ/WRITE

AGCR[7:0] — AGC Reference parameter.
AGCR[7:0] allows to adjust the analog signal level at the input of the VES1820X. Depending on the modulation type, AGCR[7:0] must be set as follows (decimal values) :

AGCR[7:0]	Modulation
140	16-QAM
140	32-QAM
106	64-QAM (default)
120	128-QAM
92	256-QAM

3. AGCONF 02_{16} READ/WRITE

KAGC — KAGC[1:0] represents the AGC time constant. Default is KAGC[1:0] = 00.
The AGC loop bandwidth can be calculated with the following formula :

$$\frac{Bw}{RS} = \frac{\left(10^{\frac{Range}{10240}} - 1\right).AGCREF}{2^{13+2.Kagc}}$$ where Range is the total AGC range in dB.

PWMA PWMA indicates the polarity of the VAGC output. When PWMA =1 (default) the higher the DC level is, after low pass filtering on VAGC output, the lower the gain must be. It is the opposite when PWMA=0.

SELAGC SELAGC determines which kind of information is provided on output pin VAGC. When SELAGC = 0 (default), VAGC is the PWM encoded AGC value. When SELAGC = 1, VAGC is the sign of the amplitude error. (See FIGURE 11 and FIGURE 12 page 16).

ADCSEL ADCSEL selects if the internal ADC is used (ADCSEL = 0) or if an external ADC is used (ADCSEL = 1).

FELPWM FELPWM determines the functionality of output pin FEL.
When FELPWM = 0 (default), FEL is a front end lock indicator.
When FELPWM = 1, FEL is a PWM encoded output, which value is programmed in register PWMREF (index 34_{16}).

4. CLKCONF **03_{16} READ/WRITE**

CLK_C CLK_C[2:0] must be set to 2_{16}.

DYN DYN determines if the acquisition range for clock recovery is ± 120 ppm (DYN = 0, default) or ± 240 ppm (DYN = 1).

GAIN2 GAIN2 allows to program the gain of the second decimation filter. When GAIN2 = 0 (default), the gain is 1 and when GAIN2 = 1, the gain is 2.

GAIN3 GAIN3 allows to program the gain of the third decimation filter. When GAIN3 = 0 the gain is 1 and when GAIN3 = 1 (default) the gain is 2.

NDEC[1:0] NDEC[1:0] determines the number of decimations according to the following table

Symbol Rate (SR)	NDEC[1 :0]
SACLK/8 < SR < SACLK/4	00 (0)
SACLK/16 < SR < SACLK/8	01 (1)
SACLK/32 < SR < SACLK/16	10 (2)
SACLK/64 < SR < SACLK/32	11 (3)

5. CARCONF **04_{16} READ/WRITE**

CAR_P[2] CAR_P[2] determines whether the carrier acquisition range is ± 2.5% of the Symbol Rate (CAR_P[2]=0) or ± 8% (CAR_P[2]=1). Default is CAR_P[2]=0.

CAR_P[1:0] CAR_P[1:0] must be set to 1_{16}.

CAR_C[3:0] CAR_C[3:0] configures the coefficients of the carrier recovery loop filter, according to the table below :

CARC[3:0]	Damping factor (ξ)	Loop Bandwith (BW/RS)
0	1.3	0.007
1	0.9	0.008
2	0.7	0.01
3	0.5	0.014
4	1.8	0.014
5	1.3	0.015
6	0.9	0.017
7	0.7	0.021
8	2.6	0.027
9	1.8	0.028
A	1.3	0.03
B	0.9	0.034
C	3.7	0.054
D	2.6	0.055
E	1.8	0.056
F	1.3	0.06

6. LOCKTHR **05_{16} READ/WRITE**

LTHR[7:0] LTHR[7:0] is the threshold value used for carrier lock detection. LTHR[7:0] must be set accordingly with the following table (decimal values) :

LTHR[7:0]	Modulation
135	16-QAM
100	32-QAM
70	64-QAM (default)
54	128-QAM
38	256-QAM

7. EQCONF1 **06_{16} READ/WRITE**

POSI[2:0] POSI[2:0] determines the position of the reference coefficient of the equalizer, as shown in the following table :

POSI[2:0]	Reference
000	Tap N°2 (second tap)
001	Tap N°3
010	Tap N°4 (default)
011	Tap N°5
100	Tap N°6
101	Tap N°7
110	Tap N°8
111	Tap N°9

VALI VALI determines the initialization value of the equalizer reference coefficient. Default is VALI = 0.

ENADAPT When ENADAPT is set to 0, the adaptation algorithm is inhibited. The equalizer is running with the current value of the coefficients. When ENADAPT=1 (default), the coefficients of the equalizer are continuously adjusted.

ENEQUAL When ENEQUAL=0, the equalization function is inhibited. The equalizer coefficients are fixed to their initialization values. The default is ENEQUAL = 1.

DFE DFE determines wether the equalizer is configured as a linear transversal equalizer (DFE=0) or a decision feedback equalizer (DFE=1, default).

8. EQSTEP **07_{16} READ/WRITE**

EQST1[2:0] EQST1[2:0] sets the convergence step of the adaptation algorithm during the acquisition phase. The higher EQST1[2:0] is, the higher the step is. Default value is 2.

EQST2[2:0] EQST2[2:0] sets the convergence step of the adaptation algorithm during the tracking phase.The higher EQST2[2:0] is, the higher the step is. Default value is 3.

9. MSETH **08_{16} READ/WRITE**

MSETH[7:0] MSETH[7:0] is the threshold value used to switch from the acquisition phase to the tracking phase. MSETH[7:0] must be set as follows (decimal values) :

MSETH[7:0]	Modulation
162	16-QAM
116	32-QAM
67	64-QAM (default)
52	128-QAM
35	256-QAM

10. AREF **09_{16} READ/WRITE**

AREF[7:0] AREF[7:0] is a reference parameter that optimizes the equalizer convergence during the acquisition phase. AREF[7:0] must be set as follows (decimal values) :

AREF[7:0]	Modulation
145	16-QAM
150	32-QAM
106	64-QAM (default)
126	128-QAM
107	256-QAM

11. BDR_LSB **$0A_{16}$ READ/WRITE**

BDR_LSB 8 LSB bits : BDR[7:0] of the BAUD rate frequency to program.

12. BDR_MID **$0B_{16}$ READ/WRITE**

BDR_MID 8 MID bits : BDR[15:8] of the BAUD rate frequency to program.

13. BDR_MSB **$0C_{16}$ READ/WRITE**

BDR_MSB 6 MSB bits : BDR[21:16] of the BAUD rate frequency to program.
The value BDR[21:0] to program is a function of the system frequency (SYSCLK=2*SACLK) and of the symbol rate RS :

$$BDR[21:0] = NINT\left(\frac{2^{24} \times RS \times 2^{Ndec}}{SYSCLK}\right)$$

NINT : Nearest Integer value
Ndec : Number of decimations (see page 22)

14.BDR_INV **$0D_{16}$ READ/WRITE**

BDRI[7:0] BAUD RATE Inverse. The value BDRI[7:0] to program is a function of the cristal frequency (XIN) and of the symbol rate RS :

$$BDRI[7:0] = NINT\left(\frac{16 \times SYSCLK}{RS \times 2^{Ndec}}\right)$$

NINT : Nearest Integer value
Ndec : Number of decimations (see page 22)

If BDRI $\geq$ 255, then set BDRI to 255.

15.GAIN **OE_{16} READ/WRITE**

GNYQ[2:0] GNYQ[2:0] determines the gain of the Nyquist filter according to the following table :

GNYQ[2:0]	Gain
000	1
001	1.5
010	2
011	3
100	4
101	6
110	8
111	12

SFIL SFIL selects which anti-aliasing filter is used.

Symbol Rate (SR)	SFIL
SYSCLK/12.3 < SR < SYSCLK/8	0
SYSCLK/16 < SR < SYSCLK/12.3	1
SYSCLK/24.6 < SR < SYSCLK/16	0
SYSCLK/32 < SR < SYSCLK/24.6	1
SYSCLK/49.2 < SR < SYSCLK/32	0
SYSCLK/64 < SR < SYSCLK/49.2	1
SYSCLK/98.4 < SR < SYSCLK/64	0
SYSCLK/128 < SR < SYSCLK/98.4	1

GLPF[1:0] GLPF[1:0] determines the gain of the antialiasing filter according to the following table :

GLPF[1:0]	Gain
00	1
01	2
10	4
11	8

SSAT[1:0] SSAT[1:0] determines the number of samples during which the saturation counters accumulate the saturations.

SSAT[1:0]	Number of samples
00	2048
01	4096
10	8192
11	16384

16.TEST **$0F_{16}$ READ/WRITE**

The 3 LSBs of TEST register must be set LOW.

SELOUT[1:0] SELOUT[1:0] selects which data are sent to the TESTO outputs :
- When SELOUT[1:0]=00 (default) TESTO=0000_{16}
- When SELOUT[1:0]=01 :
  - TESTO[16:9] is the real part of the output scatter
  - TESTO[8:1] is the imaginary part of the output scatter
  - TESTO[0] is the symbol clock output
- When SELOUT[1:0]=10 :
  - TESTO[16:9] is the real part of the equalizer coefficients
  - TESTO[8:1] is the imaginary part of the equalizer coefficients
  - TESTO[0] is a corresponding synchronization signal
- When SELOUT[1:0]=11 :
  - TESTO[16:10] is the real part of the output scatter
  - TESTO[8:2] is the imaginary part of the output scatter
  - TESTO[1] is the symbol clock output
  - TESTO[9] is the demodulator data output
  - TESTO[0] is the demodulator clock output

BYPIIC When BYPIIC = 0 (default) CTRL1 output is tri-stated and CTRL2 is a control output pin, which value is programmed by parameter CTRL2 of this register.
When BYPIIC = 1, pin CTRL1 outputs SDA input and CTRL2 outputs SCL input. These 2 lines can be fed to the I2C interface of the tuner, so that this one can be made inactive after the tuner has been programmed (better phase noise characteristics).

CTRL2 CTRL2 controls the value of CTRL2 output pin when BYPIIC = 0.

17. RSCONF **10_{16} READ/WRITE**

IEI When high, IEI inhibits setting the error indicator bit (MSB of the second byte) in the MPEG2 packet in the event of an uncorrectable RS block. The default value is IEI = 0.

DESCI DESCrambler Inhibition parameter. When set high, DESCI inhibits the descrambling process within the VES1820X. The default value is DESCI = 0 which means "descrambler validated ".

RSI Reed Solomon Inhibition parameter. When set high, RSI inhibits the correction procedure of the RS decoder within the VES1820X. The MSB of the second byte (error indicator) is not set high even if the provided packet is uncorrectable. The default value is RSI = 0 which means "correction capability of RS decoder validated ".

C[1:0] C[1:0] sets the two parameters (α,β) used in the synchronization block. In the frame acquisition phase, α defines the number of consecutive MPEG2 sync (or $\overline{\text{sync}}$) that the VES1820X must find to declare the deinterleaver synchronized and to switch to the tracking phase.
In the tracking phase, β defines the number of consecutive MPEG2 sync (or $\overline{\text{sync}}$) that the VES1820X must miss to declare the deinterleaver desynchronized and to switch back to the sync phase.The default value is C[1:0] = 3_{16} which corresponds to α = 6 and β = 15.

C[1]	C[0]	α	β
0	0	5	6
0	1	5	8
1	0	6	10
1	1	6	15

CLB_UNC CLBUNC is an active low reset signal which clears the 7-bit counter used to memorize the number of uncorrectable packets contained in register CPT_UNCOR. To clear the counter first write CLB_UNC=0 then CLB_UNC=1 (default).

PVBER[1/0] These two bits allow to program the number of bits of the sequence length where the demodulator output Bit Error Rate is computed. The number of bits varies from 10^5 to 10^8 bits. The default value is PVBER = 1_{16} which corresponds to 10^6 bits.

PVBER[1]	PVBER[0]	Number of bits
0	0	10^5
0	1	10^6
1	0	10^7
1	1	10^8

18. SYNC **11_{16} READ ONLY**

EQ_ALGO EQ_ALGO indicates whether the current algorithm used for equalization is the acquisition one (EQ_ALGO=0) or the tracking one (EQ_ALGO=1).

CARLOCK CARLOCK goes high when the demodulator part within the VES1820X is synchronized : carrier has been recovered, else CARLOCK is low.

FSYNC FSYNC goes high when the deinterleaver within the VES1820X is synchronized : α consecutives MPEG2 sync pattern (or $\overline{\text{sync}}$) have been detected. FSYNC goes low when β consecutives MPEG2 sync pattern (or $\overline{\text{sync}}$) have been missed. α and β are programmable within CONF register.

FEL Front End Lock. FEL goes high when the 2 signals CARLOCK and FSYNC are both at a high level : VES1820X is synchronized according to the DVB specifications.

BER[1:0] BER[1:0] gives a rough idea of the Bit Error Rate at the demodulator output BER[1:0] determines 4 areas of BER as shown in the following table :

BER	BER[1]	BER[0]
$> 10^{-2}$	0	0
$10^{-3} < BER < 10^{-3}$	0	1
$10^{-4} < BER < 10^{-3}$	1	0
$< 10^{-4}$	1	1

NODVB When high this means that the deinterleaver has been able to synchronize in DVB mode but the framing is not DVB compliant (there is no sync byte every 8 frames).

19. POLA **12_{16} READ/WRITE**

POCLK Determines if the VES1820X output clock OCLK is inverted or not. When POCLK is set low (default), the OCLK clock is not inverted, and the falling edge of the clock is located in the middle of the provided DO[7:0] byte. When POCLK is set high, then the rising edge of the clock is located in the middle of the DO[7:0] output byte.

PDEN Determines if the VES1820X output signal DEN is inverted or not before being provided. When set low (default), DEN is not inverted and therefore is high during the 188 first bytes of each packet and low for the 16 remaining bytes. When set high DEN is low for 188 bytes and high for 16.

PUNCOR Determines if the VES1820X output signal UNCOR is inverted or not before being provided. When set low (default), UNCOR is not inverted and therefore is high during the 188 first bytes of each packet and low for the 16 remaining bytes only in case where the provided packet is declared uncorrectable by the RS decoder. If the packet is correctable UNCOR remains low for the 204 bytes. When set high, UNCOR is low for 188 bytes and high for 16, always in case of an uncorrectable packet. If the packet is correctable UNCOR remains high for the 204 bytes of the packet.

PPSYNC Determines if the VES1820X output signal PSYNC is inverted or not before being provided. When set low (default), PSYNC output signal is not inverted and therefore is high during the first byte of each packet (sync byte 47_{16} and low for the 203 remaining bytes. When set high, PSYNC is low for the first byte of each packet (sync byte 47_{16}) and high for 203 remaining bytes.

PFEL Determines if the VES1820X output signal FEL is inverted or not before being provided. When set low (default) FEL is not inverted and is high when the VES1820X is fully synchronized. When set high, FEL is inverted and is low when the VES1820X is fully synchronized.

P/MF Determines whether the PSYNC or MFSTART signal is provided on the PSYNC output pin of the VES1820X. When set high (default), PSYNC is provided. When set low, MFSTART is provided. MFSTART corresponds to the detection of the inverted sync byte $B8_{16}$: MFSTART is high one frame out of eight for a period of OCLK at the beginning of the packet.

	POINT	Programmable Output INTerface. POINT = 1 (default) allows to not provide the check bytes of the RS decoder but a low level. In that case the output clock OCLK is also fixed to a DC level depending on POCLK.

20.CPT_UNCOR **13_{16} READ ONLY**

CPTU[6:0]	7-bit counter which memorizes the number of uncorrectable packets found after a master reset (hard or soft) or between two CLB_UNC writing. When the counter reaches $7F_{16}$, it remains in this state until either a master reset or a CLB_UNC occurs. Note that reading the CPTU[7:0] register does not reset the counter. CPTU[7:0] is READ ONLY.

21. BER_LSB **14_{16} READ ONLY**

BER[7:0]	8 LSB of the BER[19:0] register.

22. BER_MID **15_{16} READ ONLY**

BER[15:8]	8 MID bit of the BER[19:0] register.

23. BER_MSB **16_{16} READ ONLY**

BER[19:16]	4 MSB bit of the BER[19:0] register. BER[19:0] indicates the contents of the 20-bit error counter used in the demodulator output Bit Error Rate measurement. These 20 bits must be interpreted as a decimal number that must be multiplied by 10^{-5}, 10^{-6} 10^{-7} or 10^{-8} depending on the programmable value of PVBER, to directly obtain the BER at demodulator output. For instance, if PVBER = « 11 » (in register RSCONF) and VBER[19:0] =25 , then the BER at demodulator output is 2.5 X 10^{-7}. (See OUTPUT SIGNAL QUALITY MEASUREMENT (BER) on page 36). Reading of BER[19:0] must occur in the following order : BER_LSB, BER_MID, BER_MSB.

24.VAGC **17_{16} READ ONLY**

VAGC[7:0]	8 bits data output in binary format for AGC information. 00_{16} corresponds to the minimum expected gain value, and FF_{16} to the maximum.

25. MSE **18_{16} READ ONLY**

MSE[7:0]	MSE[7:0] represents the Mean Square Error of the demodulated output signal. MSE[7:0] can be used as a representation of the signal quality.

26. VAFC **19_{16} READ ONLY**

VAFC [7:0]	VAFC[7:0] indicates the frequency offset •F (in 2's complement) between the transmitter and the receiver, when the carrier has been recovered. •F = (VAFC x RS) / 1024 . RS is the Symbol Rate.

27. IDENTITY **$1A_{16}$ READ ONLY**

IDENTITY	contains the value $7B_{16}$ which corresponds to revision 1 of the VES1820X.

28.ADC **$1B_{16}$ READ/WRITE**

PCLK	PCLK sets the polarity of internal sampling clock. When an external ADC is used PCLK must be set to 0 default (sampling on rising edge of SACLK). When the internal ADC is used PCLK must be set to 1 (sampling on falling edge of SACLK).

PDOWN When PDOWN is set high the internal ADC is in a stand-by mode (no consumption).
When PDOWN = 0 the ADC is active.

29. EQCONF2 $1C_{16}$ READ/WRITE

STEPTL[2 :0] STEPTL[2 :0] allow to program the step of the tap leakage algorithm that can be used in the adaptation process. Default is 000 and means that tap leakage is not used.

CTADAPT CTADAPT is used only if the equalizer is inhibited. In this case, it indicates if the center tap coefficient of the equalizer is adapted (CTADAPT=1) or not (CTADAPT=0). It can then compensate for eventual AGC residual error.

CTPHASE CTPHASE indicates if the imaginary part of the center tap coefficient is adapted (CTPHASE=1,default) or not (CTPHASE=0).

SGNALGO SGNALGO selects between 2 options in the adaptation algorithm. If DFE mode is selected then SGNALGO must be set to 1.

30. CKOFFSET $1D_{16}$ READ

CKOFF[7 :0] CKOFF[7 :0] provides the symbol clock frequency offset (SRoffset) according to the following formula :

If DYN=0 SRoffset = (CKOFF * 120 / 128) ppm
If DYN=1 SRoffset = (CKOFF * 240 / 128) ppm

31. PLL $1E_{16}$ READ/WRITE

DIVSEL[2 :0] DIVSEL[2 :0] allow to set the multiplying factor of the PLL so that the system clock (2*SACLK) is equal to XIN*(DIVSEL+1) (DIVSEL from 0 to 7). Default is DIVSEL=000.

PDPLL When PDPLL=1 (default) the PLL is in reset/power-down mode, else the PLL is active.

BYPPLL When BYPPLL=1 (default) the PLL is bypassed, else the PLL is used.

OOLCLRN When set high OOLCLRN enables Out Of Lock detection of the PLL. When set low it clears the Out Of Lock flag (OOLN) and resets the OOL circuitry.

OOLN Read only flag, indicating if the PLL is out of lock (OOLN=0).

32. INTSEL 20_{16} READ/WRITE

SERINT When SERINT=0, then the output interface is a parallel interface on pins DO[7:0] as described in FIGURE 6 and FIGURE 7 page 13.
When SERINT=1, then the output interface is a serial interface on pin DO[0], as described in FIGURE 8 page 14.

MSBFIRST If SERINT=1, MSBFIRST determines if the output bytes are serialized MSB first (MSBFIRST=1, default) or LSB first (MSBFIRST=0).
If SERINT=0, it determines if the MSB of the output byte DO[7 :0] is DO[7] (MSBFIRST=1, default) or DO[0] (MSBFIRST=0).

SWAP This parameter allows to swap the output pins UNCOR and PSYNC. When SWAP = 0 default, UNCOR is on pin 42 and PSYNC on pin 43. When SWAP = 1, UNCOR is on pin 43 and PSYNC on pin 42.

PARMOD PARMOD selects between mode A (PARMOD=0,default) and mode B (PARMOD=1) for the parallel interface when this one is selected (SERINT=0). See FIGURE 6 and FIGURE 7 page 13.

DIV[3 :0] DIV[3 :0] set the division factor for the output clock OCLK when the parallel mode B is selected, according to the following table :

DIV	OCLK
0000 (default)	2*SACLK
0001	SACLK/1
0010	SACLK/2
0011	SACLK/3
0100	SACLK/4
0101	SACLK/5
0110	SACLK/6
0111	SACLK/7
1000	SACLK/8
1001	SACLK/9
1010	SACLK/10
1011	SACLK/11
1100	SACLK/12
1101	SACLK/13
1110	SACLK/14
1111	SACLK/15

33. SATNYQ **21_{16} READ ONLY**

SATNYQ[7:0] SATNYQ represents the number of saturations that occur at the output of the Nyquist filter, during a period of 2048, 4096, 8192 or 16384 samples depending on the value programmed on parameter SSAT[1:0].

34. SATADC **22_{16} READ ONLY**

SATADC[7:0] SATADC represents the number of saturations that occur at the output of the ADC, during a period of 2048, 4096, 8192, or 16384 samples depending on the value programmed on parameter SSAT[1:0].

35. HALFADC **23_{16} READ ONLY**

HLFADC[7:0] HLFADC represents the number of times that the output of the ADC exceeds the mid-range, during a period of 2048, 4096, 8192 or 16384 samples, depending on the value programmed on parameter SSAT[1:0].

36. SATDEC1 **24_{16} READ ONLY**

SDEC1[7:0] SDEC1 represents the number of saturations that occur at the output of first decimation filter, during a period of 2048, 4096, 8192 or 16384 samples, depending on the value programmed on parameter SSAT [1:0].

37. SATDEC2 **25_{16} READ ONLY**

SDEC2[7:0] SDEC2 represents the number of saturations that occur at the output of second decimation filter, during a period of 2048, 4096, 8192 or 16384 samples, depending on the value programmed on parameter SSAT [1:0].

38. SATDEC3 **26_{16} READ ONLY**

SDEC3[7:0] SDEC3 represents the number of saturations that occur at the output of third decimation filter, during a period of 2048, 4096, 8192 or 16384 samples, depending on the value programmed on parameter SSAT [1:0].

39. SATAAF **27_{16} READ ONLY**

SAAF[7:0] SAAF represents the number of saturations that occur at the output of the anti-aliasing filter, during a period of 2048, 4096, 8192 or 16384 samples, depending on the value programmed on parameter SSAT [1:0].

40. SATTHR **30_{16} READ/WRITE**

STHR[7:0] STHR is a threshold value, compared to the register SATADC. If SATADC > STHR then an interrupt can be generated on pin IT. (See register ITSEL).

41. HALFTHR **31_{16} READ/WRITE**

HLFTHR[7:0] HLFTHR is a threshold value, compared to the register HLFADC. If HLFADC < HLFTHR then an interrupt can be generated on pin IT (See register ITSEL).

42. ITSEL **32_{H} READ/WRITE**

ITEN INTerrupt Enable. When ITEN is set to 1 then the output pin IT is configured as an interrupt pin. The event(s) that will produce an interrupt is defined by ITSEL[6:0]. When ITEN is set to 0, the output pin IT is a control line output, which value is determined by ITSEL[6].

ITSEL[0] If ITSEL[0] is set to 1, then an interrupt is generated on each rising edge of frame synchronization flag. (not synchronized ----> synchronized).

ITSEL[1] If ITSEL[1] is set to 1, then an interrupt is generated on each falling edge of frame synchronization flag. (synchronized ----> not synchronized).

ITSEL[2] If ITSEL[2] is set to 1, then an interrupt is generated on each uncorrectable packet.

ITSEL[3] If ITSEL[3] is set to 1, then an interrupt is generated each time the VBER is refreshed. So there will be an interrupt each 10^5, 10^6, 10^7 or 10^8 demodulator output bits depending on the value programmed in parameter PVBER (register RSCONF, index 10_{16}).

ITSEL[4] If ITSEL[4] is set to 1, then an interrupt is generated each time the value of register SATADC (index 22_{16}) is greater than the threshold SATTHR (index 30_{16}).

ITSEL[5] If ITSEL[5] is set to 1, then an interrupt is generated each time the value of register HALFADC (index 23_{16}) is less than the threshold HALFTHR (index 31_{16}).

ITSEL[6] If ITSEL[6] is set to 1, then an interrupt is generated each time the AGC is saturated (AGC = 0 or ACG = 255).

43. ITSTAT **33_{16} READ ONLY**

ITSTAT[6:0] is the interrupt status register. Each time the microcontroller detects an interrupt on pin IT, it can read out this register to know which event among those selected by ITSEL[6:0] has produced the interrupt (ITSTAT(i) corresponds to ITSEL(i)). This register is automatically cleared after each reading.

44. PWMREF **34_{16} READ/WRITE**

PWMR[7:0] is the value that will be PWM encoded and output on pin FEL when parameter FELPWM of register AGCCONF (index 02_{16}) is set to 1.

BOUNDARY SCAN

VES1820X implements a boundary scan architecture to allow access to, and control of, board test support features within integrated circuits through a Test Access Port (TAP). The TAP controller is a synchronous state machine that controls the sequence operations on the TAP circuitry when the Test Mode Select (TMS) signal changes. All state transitions occur on the basis of the TMS value on the rising edge of Test ClocK (TCK). The instruction register is a shift-register based design. It decodes the test to be performed and/or the test data register to be accessed. The instructions are shifted into the register through the Test Data Input (TDI) and are latched as the current instruction at the completion of the shifting process. The VES1820X implemented boundary scan architecture includes : a TAP controller, a scannable instruction register and three scannable test data registers : a boundary scan register, a device ID register, and a bypass register (see FIGURE 14 page 32).

The supported instructions are : EXTEST, SAMPLE, IDCODE, and BYPASS.

CELLS : Input cells are "observe-only" type and output cells are "observe and control" type.

ID number : It is included in a 32-bit identification register which is included in the scan register itself (first 32-bit of scan register). It contains a fixed value which identifies the chip.
ID number structure is :

ID version :	'H1
ID part number :	'H1820
ID manufacturer :	'HAB
IDCODE :	'H11820157

SCAN Register : It is composed of 61 cells. Each cell is associated either to an input, three-state output, bidirectional pad or to the bidirectional or three-state command itself.

FIGURE 14 : BOUNDARY SCAN BLOCK DIAGRAM

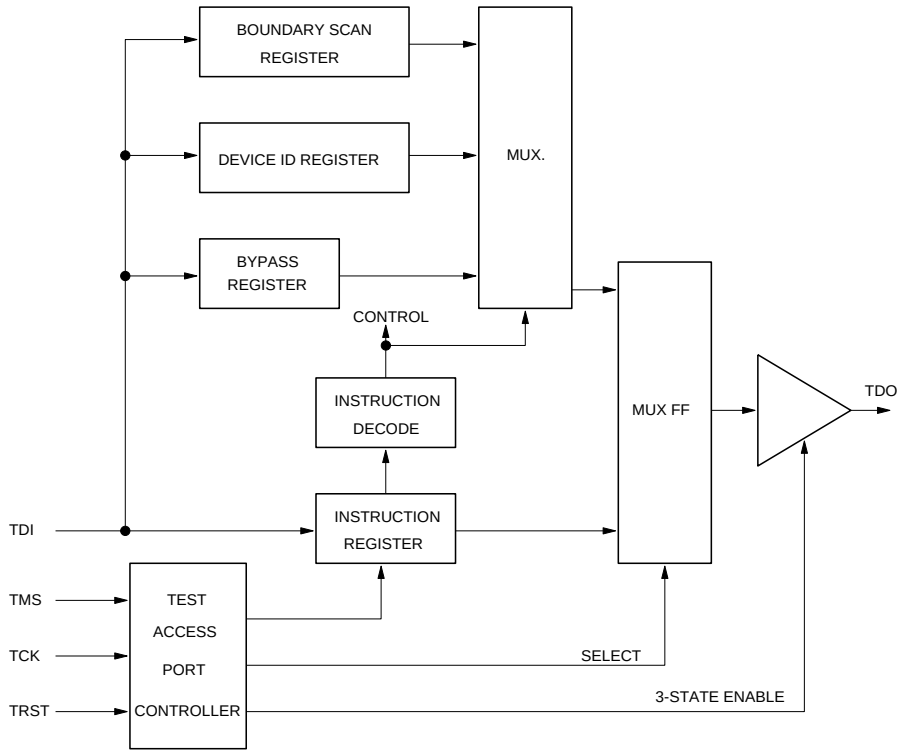


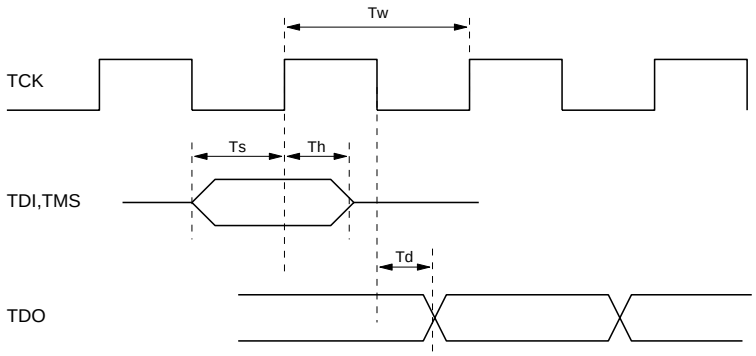
TABLE 6 : BOUNDARY SCAN CHAIN ORDER

pad signal	chain position	pad type	scan type	control signal
SCL	[56]	input	obsrv	
TEST	[55]	input	obsrv	
CLR	[54]	input	obsrv	
IICDIV[1:0]	[53:52]	input	obsrv	
SADDR[1:0]	[51:50]	input	obsrv	
-	[49]	ctrl	norm	tri
VAGC	[48]	3state	norm	U1. agc_cmd
-	[47]	ctrl	norm	U1. agc_cmd
-	[46]	ctrl	norm	U1.sda_cmd
SDA	[45]	bidir	obsrv	U1.sda_cmd
FI[8:0]	[44:36]	input	obsrv	
SACLK	[35]	3state	norm	tri
IT	[34]	3state	norm	U1.IT_cmd
-	[33]	ctrl	norm	U1.IT_cmd
CTRL2	[32]	3state	norm	U1.ctrl2_cmd
-	[31]	ctrl	norm	U1.ctrl2_cmd
TESTO[16:0]	[30:14]	3state	norm	tri
-	[13]	ctrl	norm	U1.FEL_cmd
FEL	[12]	3state	norm	U1.FEL_cmd
DO[7:0]	[11:4]	3state	norm	tri
OCLK	[3]	3state	norm	tri
DEN	[2]	3state	norm	tri
UNCOR	[1]	3state	norm	tri
PSYNC	[0]	3state	norm	tri

BOUNDARY SCAN ELECTRICAL CHARACTERISTICS

Name	Description	Min	Max	Units
t_w	TCK clock period	25		nS
t_s	TDI and TMS set up time	0		nS
t_h	TDI and TMS hold time	4		nS
t_d	TDO delay time on 50pF		12	nS

FIGURE 15 : BOUNDARY SCAN TIMING DIAGRAM



FRAME SYNCHRONIZATION

Frame synchronization is performed at the output of the demodulator to both synchronize the Forney convolutional de-interleaver and to determine the boundaries of the Reed-Solomon blocks.

MPEG2 transport packets consist of 204 bytes: one sync byte (as the first byte of the packet), 187 data bytes, and 16 redundancy bytes. The sync byte is used in frame synchronization.

The frame synchronization state machine operates in two phases:

- Acquisition Phase. When α consecutive sync bytes (or $\overline{\text{sync}}$ bytes) are detected, the output signal FSYNC goes high and the state machine switches to the Tracking Phase.
- Tracking Phase. When β consecutive sync bytes (or $\overline{\text{sync}}$ bytes) are missed, the output signal FSYNC goes low and the state machine switches back to the Acquisition Phase.

(See FIGURE 16 page 35 for details of the state machine operation).

The parameters α and β are programmable via the I2C interface. The following table shows the value of the parameters as a function of C[1:0]:

C[1]	C[0]	α	β
0	0	5	6
0	1	5	8
1	0	6	10
1	1	6	15

➢ PERFORMANCE

The following table shows an example of frame synchronization algorithm performance. Computed values for maximum average re-frame time (TRF), the meanframe misalignment time (TMF) and the probability of false alignment (PF) are given as a function of the BER at the output of the demodulator output in the case of :
$\alpha = 5$ and $\beta = 8$.

BER	Acquisition Procedure ($\alpha = 5$)		Tracking Procedure($\beta = 8$)
	T_{RF}(frames)	P_F	T_{MF}(frames)
$5X10^{-2}$	69 .95	$1.15X10^{-8}$	$9.15X10^{3}$
10^{-2}	15 .97	$2.22X10^{-9}$	$8.54X10^{8}$
$5X10^{-3}$	13 .47	$1.81X10^{-9}$	$1.83X10^{11}$
10^{-3}	11 .78	$1.54X10^{-9}$	$6.18X10^{16}$
$5X10^{-4}$	11 .59	$1.51X10^{-9}$	$1.15X10^{19}$

FRAME SYNCRONIZATION (Con't)

➢ FORMULAS

The following formulas show frame synchronization parameter relationships.

$$T_{RF} = \frac{1}{P_d^{\alpha}}\left[1631\,\frac{P_S}{1 - P_S} + \frac{1 - P_d^{\alpha}}{1 - P_d}\right]$$

where, $P_d = (1 - BER)^8$ is the probability of detecting a sync word

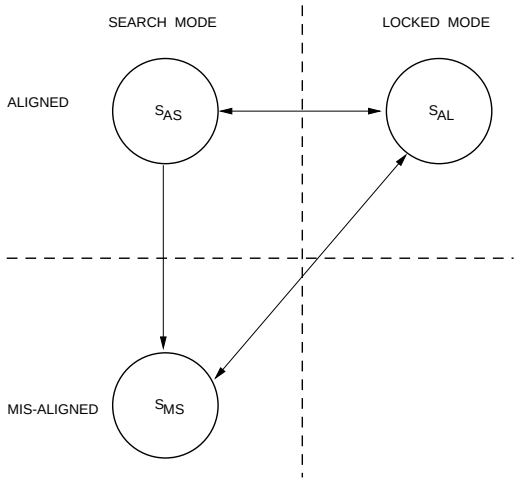
and $P_S = \frac{1}{256}$ is the probability to miss-detect the sync word.

$$P_F = \frac{1631\,P_S^{\alpha}}{P_d^{\alpha} + 1631\,P_S^{\alpha}}$$

$$T_{MF} = \frac{1}{q_d^{\beta}} \cdot \frac{1 - q_d^{\beta}}{1 - q_d}$$

where $q_d = 1 - P_d$ is the probability of failing to detect a sync word.

FIGURE 16 : FRAME SYNCHRONIZATION STATE MACHINE DIAGRAM



OUTPUT SIGNAL QUALITY MEASUREMENTS (BER)

The VES1820X provides an alternative signal quality measurement based on demodulator output Bit Error Rate computations (BER). This algorithm uses information provided by the Reed-Solomon decoder as shown in FIGURE 17. This information includes:

- The MFSTART signal which permits determining the number of bits. One Multi-Frame corresponds to 8 x 204 x 8 = 13,056 bits.

- The correction frame, CORR_FRAME, which corresponds to the number of erroneous bits in a frame at the Reed-Solomon decoder input (.ie the demodulator decoder output). The maximum value of CORR_FRAME is 64 (that is 8 bytes with 8 erroneous bits each).

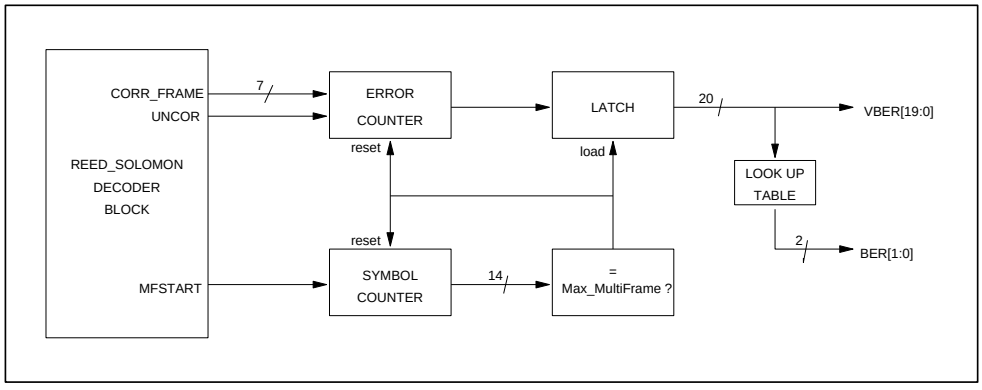
- The uncorrectable block flag, UNCOR which, when set, is counted as 27 erroneous bits (.ie, 9 erroneous bytes with three corrupted bits per byte).

The multi-frame counter is 14 bits wide and has a range of 0 to 16383. The maximum number of multiframes is programmable via I2C interface. The Error counter is 20 bits wide.
Depending on the programmation of PVBER, the BER is in the range from 10^{-2} to 10^{-5} (PVBER = 0_{16}) and can reach a precision of 10^{-8} (PVBER = 3_{16}).
The following table shows the number of bits of the sequence as a function of PVBER :

PVBER[1:0]	Number of bits
00	10^5
01	10^6
10	10^7
11	10^8

The error rate information may be obtained by reading the appropriate registers of the I2C interface (index 13, 14 & 15).

FIGURE 17 : OUTPUT SIGNAL QUALITY MEASUREMENT DETERMINATION



DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

NOTES

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