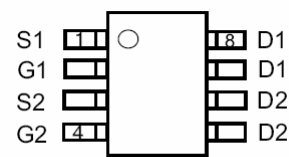


WPMD3002
Dual P-Channel, -30V, -4.9A, Power MOSFET
[Http://www.willsemi.com](http://www.willsemi.com)

V_{DS} (V)	$R_{ds(on)}$ (Ω)
-30	0.049@ $V_{GS}=-10V$
	0.070@ $V_{GS}=-4.5V$


SOP-8L


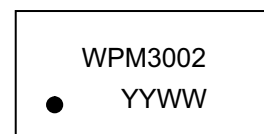
(Top View)

Pin configuration (Top view)
Descriptions

The WPMD3002 is the Dual P-Channel logic mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

Features

- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8L package design



WPM3002 = Device Code
 YY = Year
 WW = Week

Marking
Applications

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

Order information

Device	Package	Shipping
WPMD3002-8/TR	SOP-8L	4000/Reel&Tape

Absolute Maximum ratings

Parameter		Symbol	10 S	Steady State	Unit
Drain-Source Voltage		V_{DS}	-30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ^a	$T_A=25^\circ\text{C}$	I_D	-4.9	-3.8	A
	$T_A=70^\circ\text{C}$		-3.9	-3.0	
Maximum Power Dissipation ^a	$T_A=25^\circ\text{C}$	P_D	1.9	1.1	W
	$T_A=70^\circ\text{C}$		1.2	0.7	
Continuous Drain Current ^b	$T_A=25^\circ\text{C}$	I_D	-4.5	-3.6	A
	$T_A=70^\circ\text{C}$		-3.6	-2.9	
Maximum Power Dissipation ^b	$T_A=25^\circ\text{C}$	P_D	1.6	1.0	W
	$T_A=70^\circ\text{C}$		1.0	0.6	
Pulsed Drain Current ^c		I_{DM}	-30		A
Operating Junction Temperature		T_J	150		$^\circ\text{C}$
Lead Temperature		T_L	260		$^\circ\text{C}$
Storage Temperature Range		T_{stg}	-55 to 150		$^\circ\text{C}$

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ^a	$t \leq 10 \text{ s}$	$R_{\theta JA}$	56	65	$^\circ\text{C/W}$
	Steady State		87	105	
Junction-to-Ambient Thermal Resistance ^b	$t \leq 10 \text{ s}$	$R_{\theta JA}$	64	76	
	Steady State		96	115	
Junction-to-Case Thermal Resistance		$R_{\theta JC}$	32	40	
Dual Operation					
Junction-to-Ambient Thermal Resistance ^a	$t \leq 10 \text{ s}$	$R_{\theta JA}$	61	70	
	Steady State		92	112	
Junction-to-Ambient Thermal Resistance ^b	$t \leq 10 \text{ s}$	$R_{\theta JA}$	69	82	
	Steady State		102	120	
Junction-to-Case Thermal Resistance		$R_{\theta JC}$	36	45	

a Surface mounted on FR4 Board using 1 square inch pad size, 1oz copper

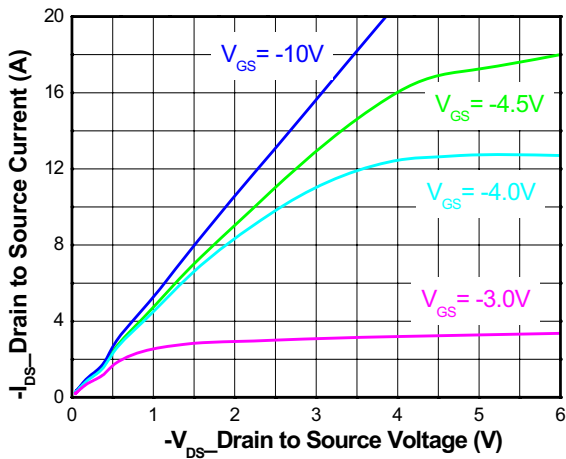
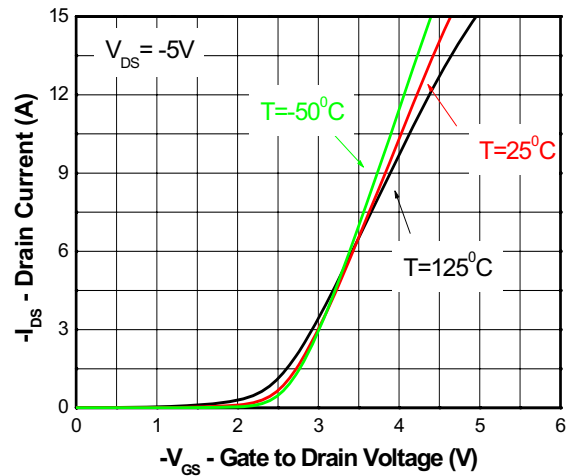
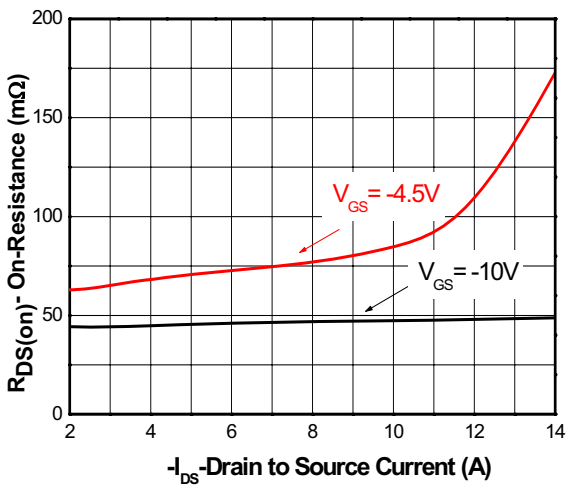
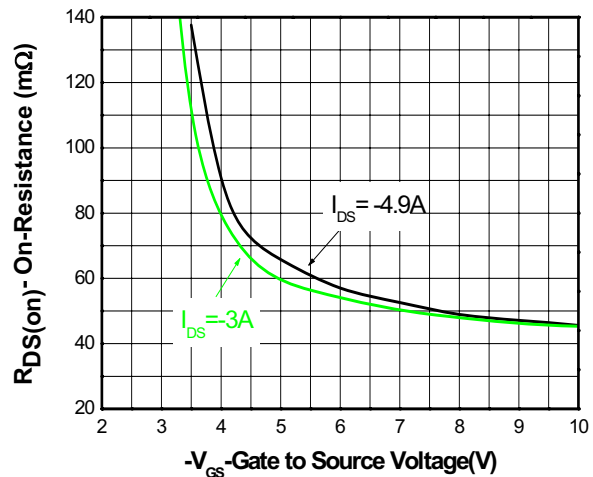
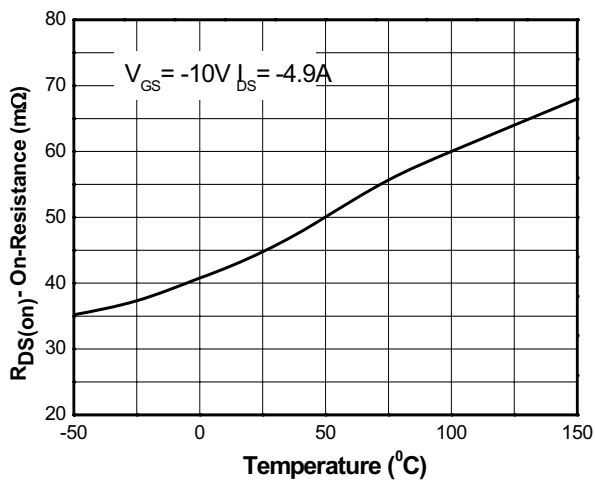
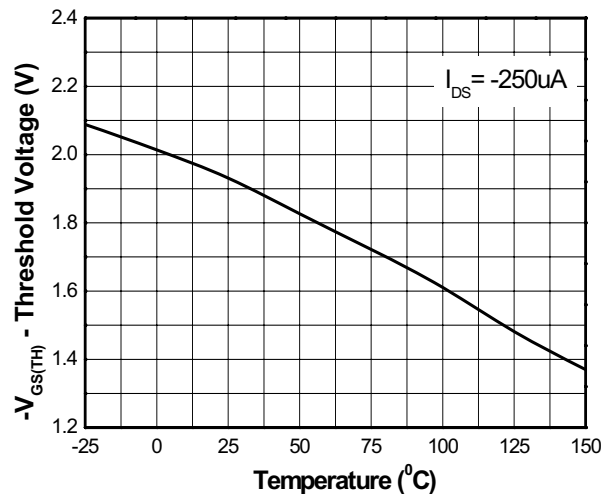
b Surface mounted on FR4 board using minimum pad size, 1oz copper

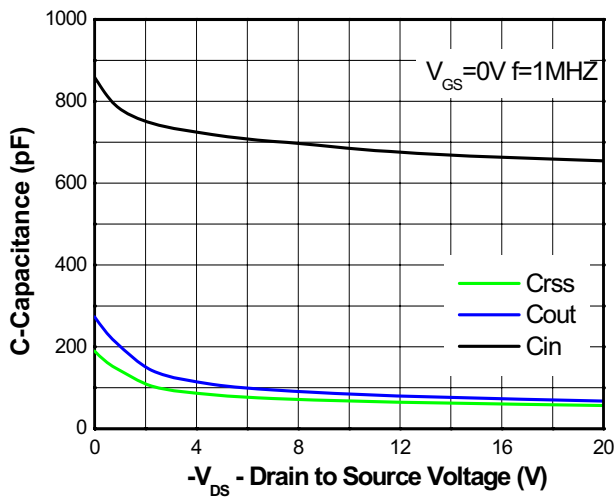
c Repetitive rating, pulse width limited by junction temperature, $t_p=10\mu\text{s}$, Duty Cycle=1%

d Repetitive rating, pulse width limited by junction temperature $T_J=150^\circ\text{C}$.

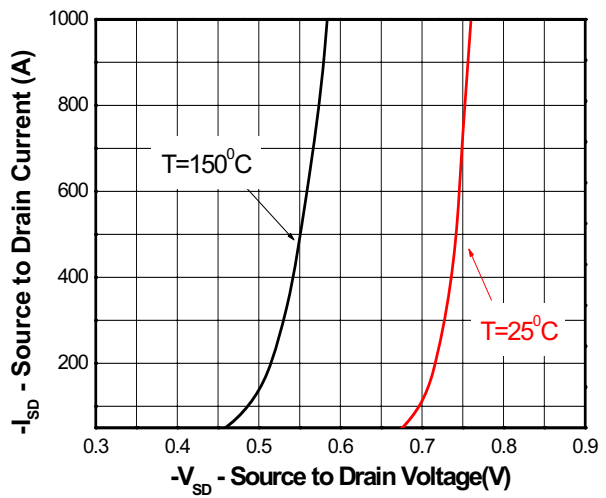
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = -250\mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
Gate-to-source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1.5	-1.9	-2.5	V
Drain-to-source On-resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -4.9\text{ A}$		49	60	m Ω
		$V_{GS} = -10\text{ V}, I_D = -3.0\text{ A}$		49	60	
		$V_{GS} = -4.5\text{ V}, I_D = -4.0\text{ A}$		70	90	
		$V_{GS} = -4.5\text{ V}, I_D = -3.0\text{ A}$		70	90	
Forward Transconductance	g_{FS}	$V_{DS} = -15\text{ V}, I_D = -3.0\text{ A}$		5.0		S
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -15\text{ V}$		670		pF
Output Capacitance	C_{OSS}			75		
Reverse Transfer Capacitance	C_{RSS}			62		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}, V_{DS} = -15\text{ V}, I_D = -4.9\text{ A}$		14.0		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.31		
Gate-to-Source Charge	Q_{GS}			1.80		
Gate-to-Drain Charge	Q_{GD}			1.60		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -10\text{ V}, V_{DS} = -15\text{ V}, R_L = 5.0\Omega, R_G = 15\Omega$		6.8		ns
Rise Time	t_r			3.2		
Turn-Off Delay Time	$t_{d(OFF)}$			25.2		
Fall Time	t_f			4.4		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}$	-0.55	-0.78	-1.50	V

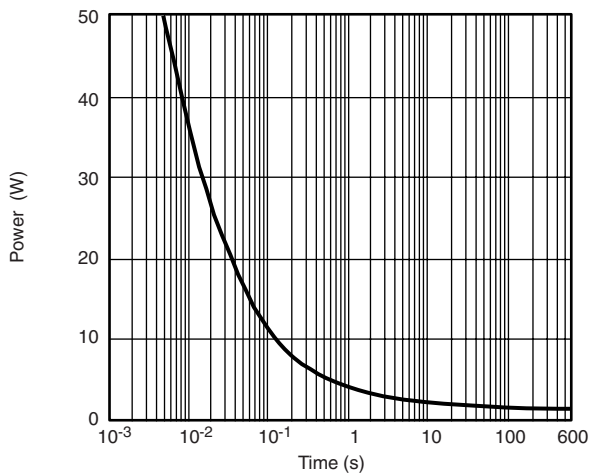
Typical Characteristics (Ta=25°C, unless otherwise noted)

Output characteristics

Transfer characteristics

On-Resistance vs. Drain current

On-Resistance vs. Gate-to-Source voltage

On-Resistance vs. Junction temperature

Threshold voltage vs. Temperature



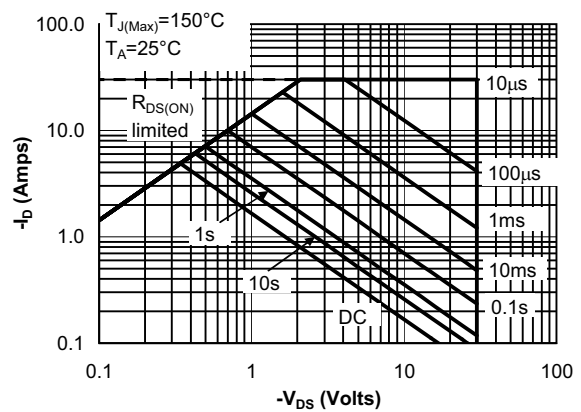
Capacitance



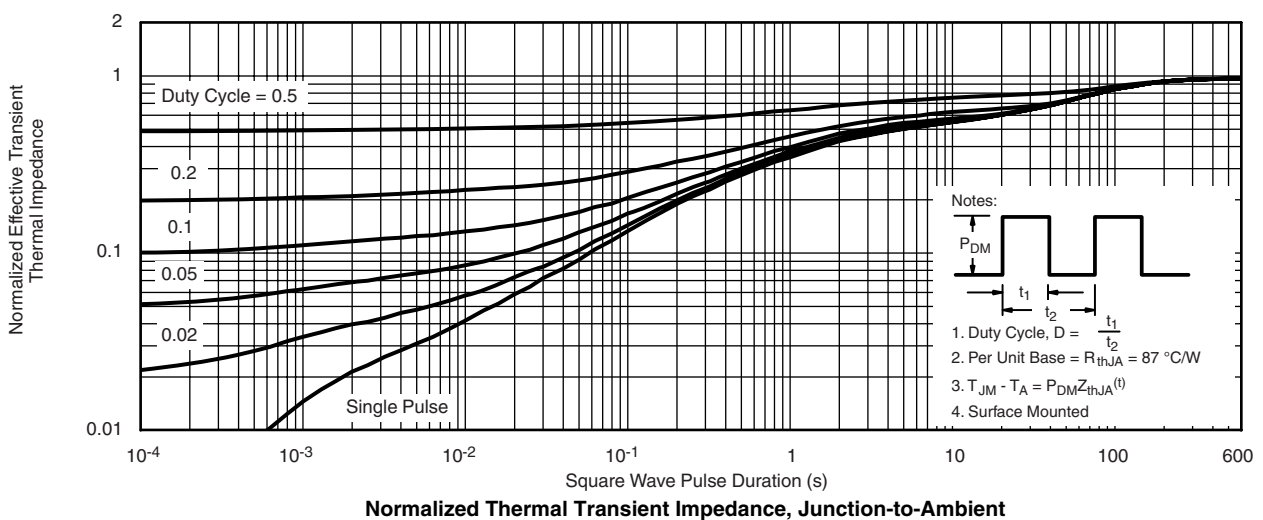
Body diode forward voltage



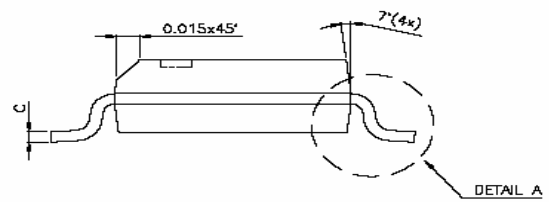
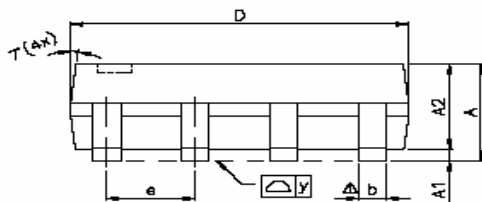
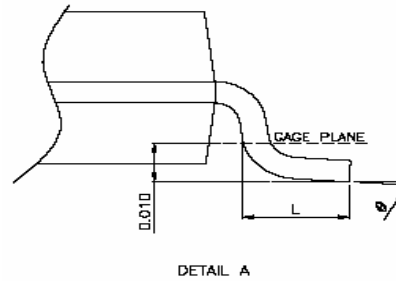
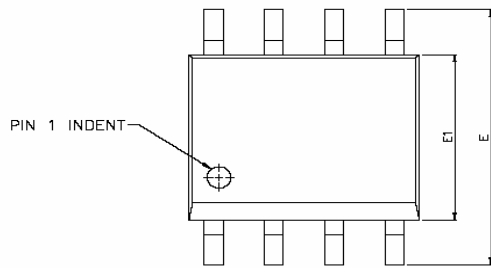
Single pulse power



Safe operating power



Normalized Thermal Transient Impedance, Junction-to-Ambient

Package outline dimensions
SOP-8L


Symbol	Dimensions in millimeter		
	Min.	Typ.	Max.
A	1.47	1.60	1.73
A1	0.10		0.25
A2		1.45	
b	0.33	0.41	0.51
C	0.19	0.20	0.25
D	4.80	4.85	4.95
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
L	0.38	0.71	1.27
y			0.076
θ	0°		8°