Z86C66

CMOS Z8®
16K ROM MICROCONTROLLER

FEATURES

Part	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z86C66	16	236	16

* General-Purpose

- 44-Pin QFP Package
- 4.5V to 5.5V Operating Range
- Low-Power Consumption
- –40°C to +105°C Operating Range
- 32 Input/Output Lines
- Vectored, Prioritized Interrupts
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86C66 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C66 is a member of the single-chip Z8® MCU family with 16 KB of ROM and 236 bytes of RAM.

The Z86C66 has been specifically designed for high-security operation. The device cannot be placed into ROMless mode, even by microprobing or simple chip alterations.

The Z86C66 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial, advanced scientific, and ***specifically high security applications.***

For applications which demand powerful I/O capabilities, the Z86C66 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports with eight lines each. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Data Memory, and 236 General-Purpose Registers.

To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C66 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (Figure 1).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION *(Continued)*

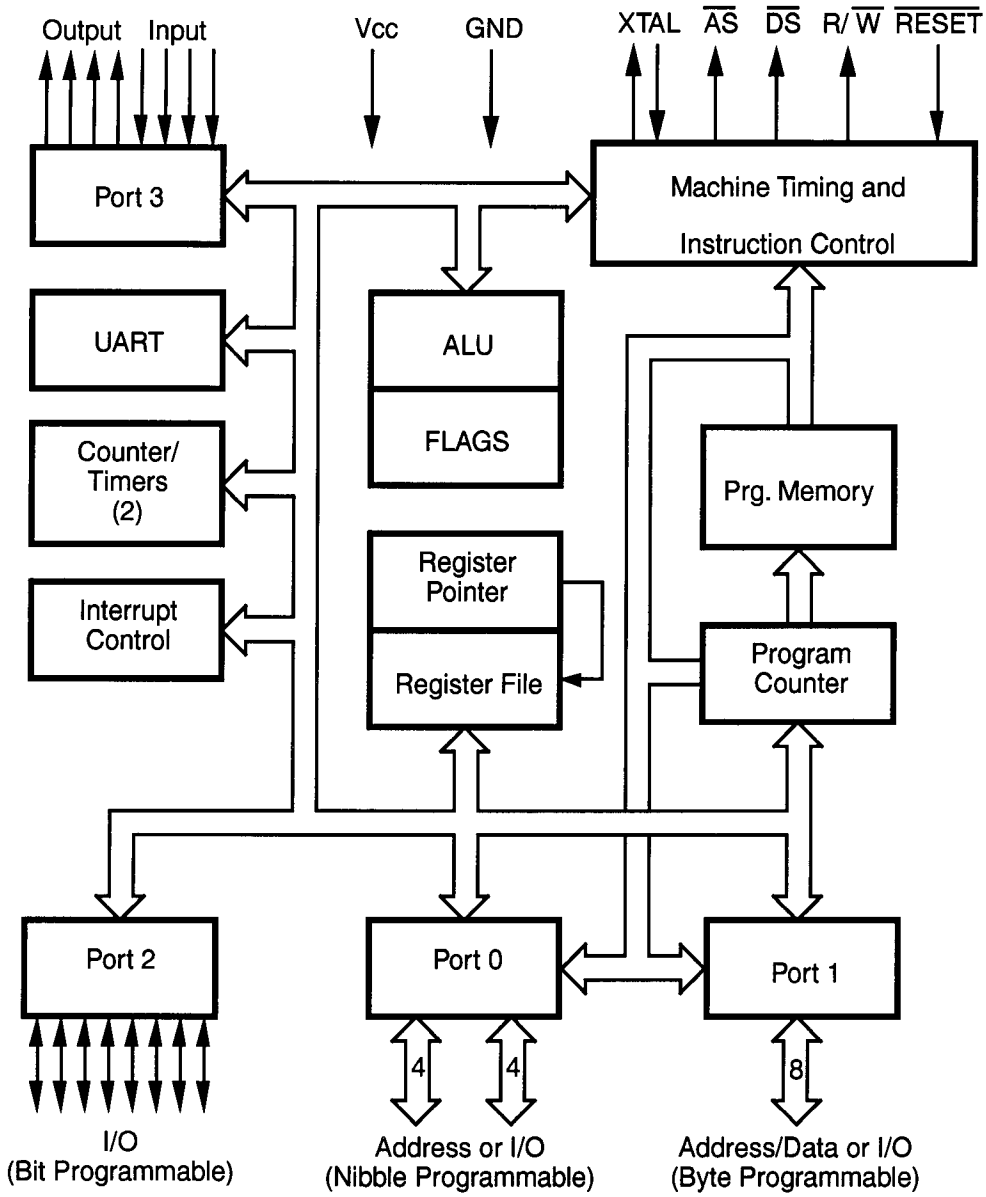

Figure 1. Z86C66 Functional Block Diagram

PIN DESCRIPTIONS

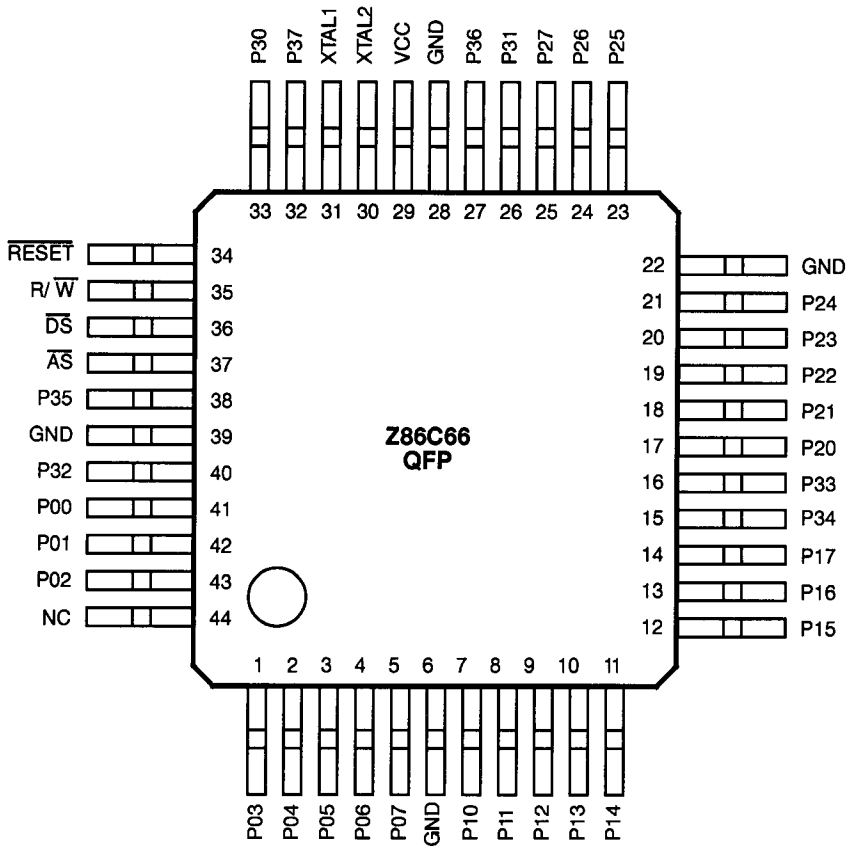

Figure 2. 44-Lead QFP Pin Assignments

Table 1. 44-Lead QFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0 Pins 3,4,5,6,7	In/Output
6	GND	Ground, GND	Input
7-14	P10-P17	Port 1 Pins 0,1,2,3,4,5,6,7	In/Output
15	P34	Port 3 Pin 4	Output
16	P33	Port 3 Pin 3	Input
17-21	P20-P24	Port 2 Pins 0,1,2,3,4	In/Output
22	GND	Ground, GND	Input
23-25	P25-P27	Port 2 Pins 5,6,7	In/Output
26	P31	Port 3 Pin 1	Input
27	P36	Port 3 Pin 6	Output
28	GND	Ground, GND	Input
29	V_{CC}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3 Pin 7	Output
33	P30	Port 3 Pin 0	Input
34	$\overline{\text{RESET}}$	Reset	Input
35	R/$\overline{\text{W}}$	Read/Write	Output
36	$\overline{\text{DS}}$	Data Strobe	Output
37	$\overline{\text{AS}}$	Address Strobe	Output
38	P35	Port 3 Pin 5	Output
39	GND	Ground, GND	Input
40	P32	Port 3 Pin 2	Input
41-43	P00-P02	Port 0 Pins 0,1,2	In/Output
44	NC	No Connect	

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†	†	

Notes:
* Voltages on all pins with respect to GND.
† See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 3).

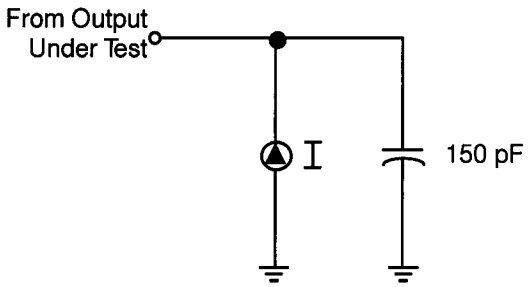

Figure 3. Test Load Diagram

APPLICATION PRECAUTION

External memory is addressable from 8000h to FFFFh.

DC ELECTRICAL CHARACTERISTICS
Z86C66

Sym	Parameter	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
	Max Input Voltage		7		7		V	[2] $I_{IN} < 250\ \mu A$
V_{CH}	Clock Input High Voltage	0.85 V_{CC}	$V_{CC}+0.3$	0.85 V_{CC}	$V_{CC}+0.3$		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	$V_{SS}-0.3$	0.8	$V_{SS}-0.3$	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	$V_{CC}+0.3$	2	$V_{CC}+0.3$		V	
V_{IL}	Input Low Voltage	$V_{SS}-0.3$	0.2 V_{CC}	$V_{SS}-0.3$	0.2 V_{CC}		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage		$V_{CC}-100$ mV		$V_{CC}-100$ mV		V	I_{OH} = –100 µA
V_{OH}	Output High Voltage (Low EMI)	2.4		2.4			V	I_{OH} = –0.5 mA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +5.0 mA
V_{OL}	Output Low Voltage (Low EMI)		0.4		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	0.85 V_{CC}	$V_{CC}+0.3$	0.85 V_{CC}	$V_{CC}+0.3$		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.2 V_{CC}	–0.3	0.2 V_{CC}		V	
I_{IL}	Input Leakage	–2	2	–2	2		µA	V_{IN} = 0 V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		µA	V_{IN} = 0 V, V_{CC}
I_{IR}	Reset Input Current		–180		–180		µA	V_{RL} = 0 V
I_{CC}	Supply Current (Standard Mode)		35		35	24	mA	[1] @ 16 MHz
I_{CC}	Supply Current (Low EMI)		6.0			4.0	mA	@ 4 MHz
I_{CC1}	Standby Current (Standard Mode)		15		15	4.5	mA	[1] HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC1}	Standby Current (Low EMI)		1.6			0.8	mA	@ 4 MHz
I_{CC2}	Standby Current		10		20	1	µA	[1] STOP Mode V_{IN} = 0 V, V_{CC}
I_{ALL}	Auto Latch Low Current	–14	14	–20	20		µA	

Notes:
[1] All inputs driven to either 0V or V_{CC}, outputs floating.
[2] $\overline{\text{Reset}}$ pin must be a maximum of V_{CC} + 0.3V.

AC CHARACTERISTICS

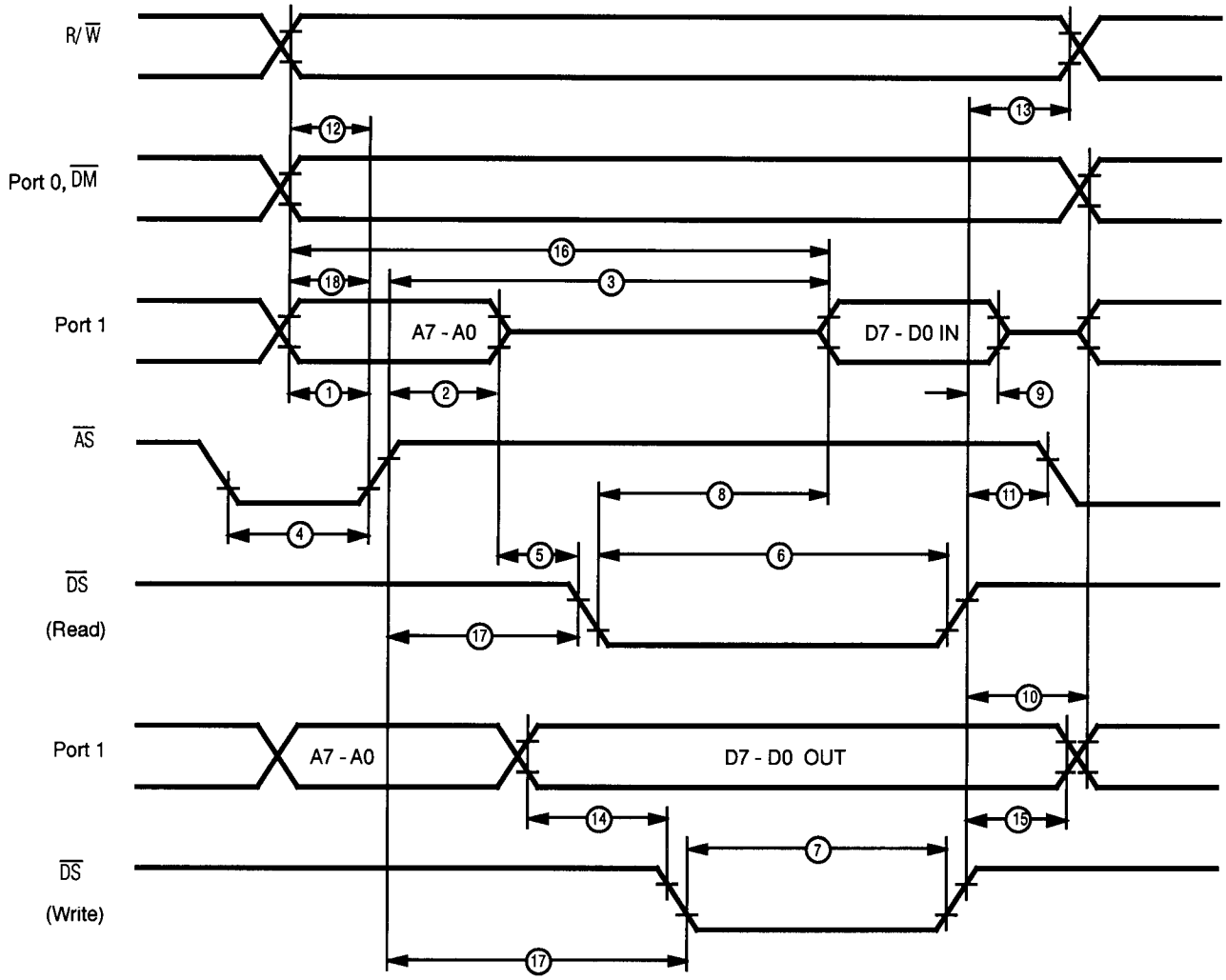

Figure 4. External I/O or Memory Read/Write

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C66 (16 MHz—Standard Mode Only[4])

No	Symbol	Parameter	T_A = 0°C to +70°C 16 MHz Min	Max	T_A = –40°C to +105°C 16 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ rise Delay	25		25		ns	[2,3]
2	TdAS(A)	$\overline{AS}$ rise to Address Float Delay	35		35		ns	[2,3]
3	TdAS(DR)	$\overline{AS}$ rise to Read Data Req'd Valid		150		150	ns	[1,2,3]
4	TwAS	$\overline{AS}$ Low Width	40		40		ns	[2,3]
5	TdAZ(DS)	Address Float to $\overline{DS}$ fall	0		0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width		135		135	ns	[1,2,3]
7	TwDSW	$\overline{DS}$ (Write) Low Width	80		80		ns	[1,2,3]
8	TdDSR(DR)	$\overline{DS}$ fall to Read Data Req'd Valid	75		75		ns	[1,2,3]
9	ThDR(DS)	Read Data to $\overline{DS}$ rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	$\overline{DS}$ rise to Address Active Delay	50		50		ns	[2,3]
11	TdDS(AS)	$\overline{DS}$ rise to $\overline{AS}$ fall Delay	35		35		ns	[2,3]
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ rise Delay	25		25		ns	[2,3]
13	TdDS(R/W)	$\overline{DS}$ rise to R/$\overline{W}$ Not Valid	35		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ fall (Write) Delay	25		25		ns	[2,3]
15	TdDS(DW)	$\overline{DS}$ rise to Write Data Not Valid Delay	35		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		210		210	ns	[1,2,3]
17	TdAS(DS)	$\overline{AS}$ rise to $\overline{DS}$ fall Delay	45		45		ns	[2,3]
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ rise Delay	25		25		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
[4] Low EMI is not selected.

Standard Test Load
All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	0.8 TpC – 15
14	TdDW(DSW)	0.4 TpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TdDM(AS)	0.9 TpC – 26.3

AC CHARACTERISTICS
Additional Timing Diagram

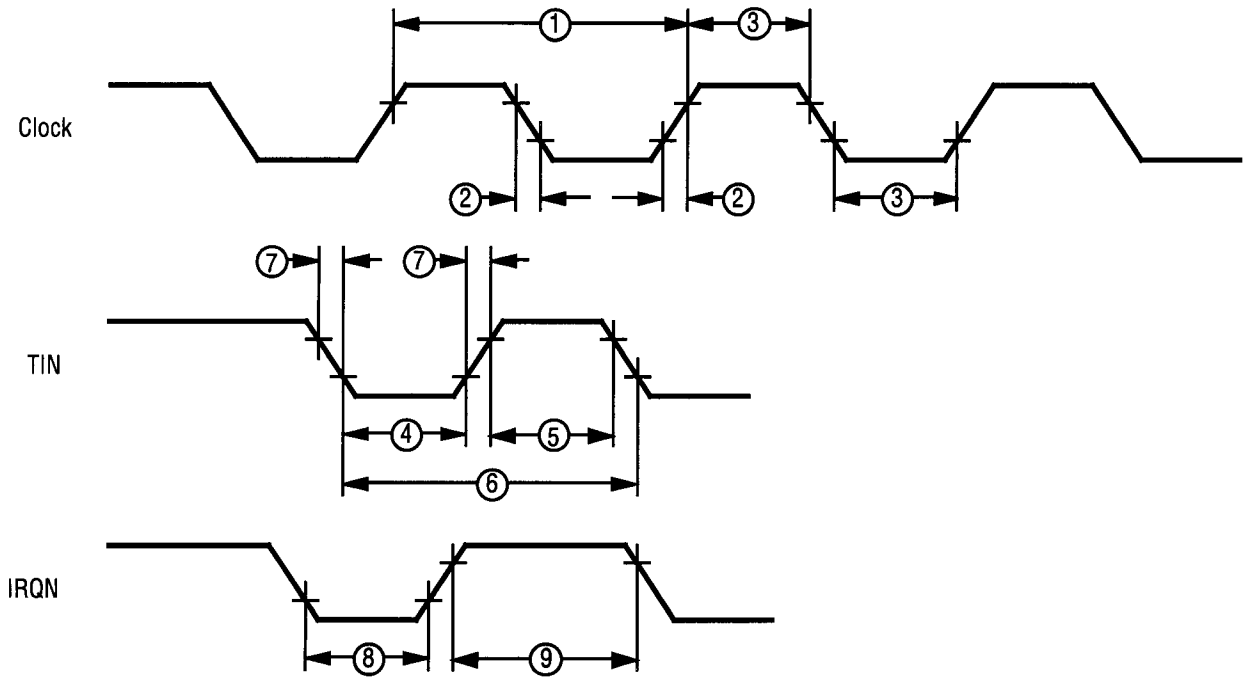

Figure 5. Additional Timing

AC CHARACTERISTICS
Additional Timing Table
Z86C66 (Standard Mode Only)

No	Symbol	Parameter	T_A = 0°C to +70°C 16 MHz Min	Max	T_A= –40°C to +105°C 16 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	62.5	1000	62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10		10	ns	[1]
3	TwC	Input Clock Width	31		31		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		ns	[2]
5	TwTinH	Timer Input High Width	5 TpC		5 TpC		ns	[2]
6	TpTin	Timer Input Period	8 TpC		8 TpC		ns	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	[2]
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		ns	[2,5]
9	TwIH	Interrupt Request Input High Times	5 TpC		5 TpC		ns	[2,3]

Notes:
[1] Clock timing references use $0.85V_{CC}$ for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS

Additional Timing Table
Z86C66 (Low EMI Mode Only)

No	Symbol	Parameter	T_A = 0°C to +70°C 4 MHz Min	Max	T_A = –40°C to +105°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	250	DC	250	DC	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10		10	ns	[1]
3	TwC	Input Clock Width	125		125		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		ns	[2]
5	TwTinH	Timer Input High Width	3 TpC		3 TpC		ns	[2]
6	TpTin	Timer Input Period	4 TpC		4 TpC		ns	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	[2]
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8b	TwIL	Interrupt Request Input Low Times	3 TpC		3 TpC		ns	[2,5]
9	TwIH	Interrupt Request Input High Times	3 TpC		3 TpC		ns	[2,3]

Notes:
[1] Clock timing references use $0.85V_{CC}$ for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com