Brief Description

The ZSSC3015 sensor signal conditioner IC is adjustable to nearly all piezo-resistive bridge sensors. Measured and corrected bridge values are provided at the Sig™ pin, which can be configured as an analog voltage output or as a one-wire serial digital output.

The ZACwire™ digital one-wire interface (OWI) can be used for a simple PC-controlled calibration procedure to program a set of calibration coefficients into an on-chip EEPROM. The calibrated ZSSC3015 and a specific sensor are mated digitally: fast, precise, and without the cost overhead associated with trimming by external devices or laser. Integrated diagnostics functions make the ZSSC3015 particularly well suited for automotive applications.

Features

- Digital compensation of sensor offset, sensitivity, temperature drift, and nonlinearity
- Programmable analog gain and digital gain; accommodates bridges with spans < 1mV/V and high offset
- Many diagnostic features on chip (e.g., EEPROM signature, bridge connection checks, bridge short detection, power loss detection)
- Independently programmable high and low clipping levels
- 24-bit customer ID field for module traceability
- Internal temperature compensation reference (no external components)
- Option for external temperature compensation with addition of single diode
- Output options: rail-to-rail ratiometric analog voltage (12-bit resolution), absolute analog voltage, ZACwire™ digital one-wire interface
- Fast power-up to data out response; output available 5ms after power-up
- Current consumption depends on programmed sample rate and mode: 1mA down to 300µA (typ.)
- Fast response time: 1.4ms typical
- High voltage protection: ≤ 30V with external JFET
- AEC-Q100 qualified

Benefits

- No external trimming components required
- PC-controlled configuration and calibration via ZACwire™ one-wire interface – simple, low cost
- High accuracy (as high as ±0.1% FSO @ -25 to 85°C; ±0.25% FSO @ -50 to 150°C)
- Single-pass calibration – quick and precise

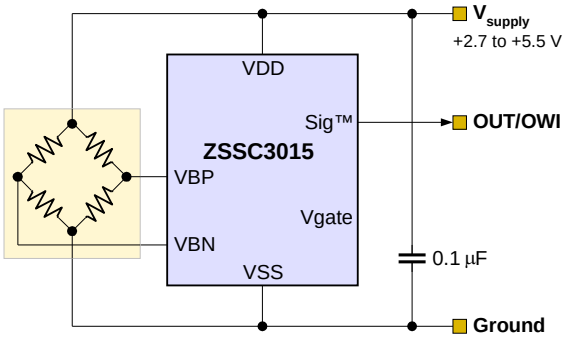
Available Support

- Evaluation Kit available
- Mass Calibration System available
- Support for industrial mass calibration available
- Quick circuit customization possible for large production volumes

Physical Characteristics

- Wide operation temperature: –50°C to +150°C
- Supply voltage 2.7 to 5.5V; with external JFET, 5.5 to 30V
- Small SOP8 package

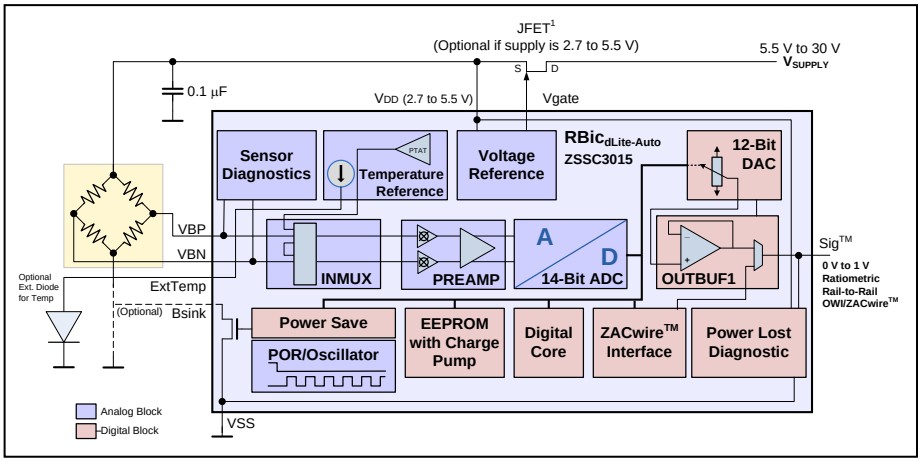
ZSSC3015 Application Circuit



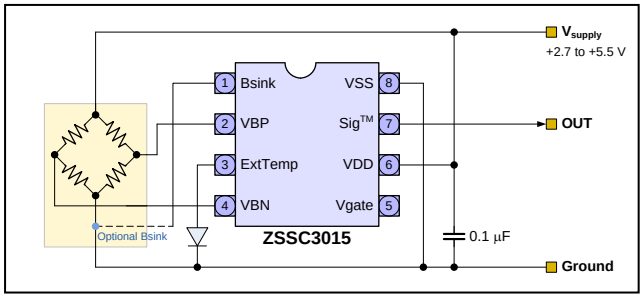
ZSSC3015 Block Diagram

Highly Versatile Applications in Many Markets Including

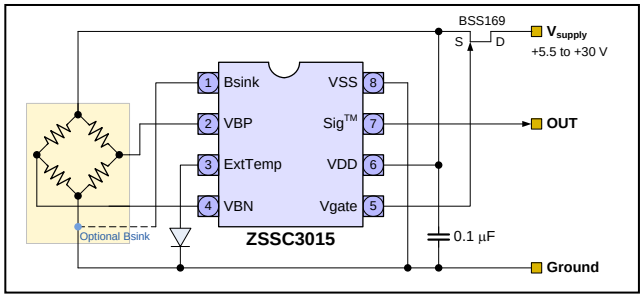
- ***Industrial***
- ***Building Automation***
- ***Office Automation***
- ***White Goods***
- ***Automotive***
- ***Portable Devices***
- ***Your Innovative Designs***



Rail-to-Rail Ratiometric Voltage Output Applications



Absolute Analog Voltage Output Applications



Part Ordering Examples *(See section 11 in the data sheet for additional options.)*

Sales Code	Description	Package
ZSSC3015NE1B	ZSSC3015 Die — Temperature range: -50°C to +150°C	Unsawn on Wafer
ZSSC3015NE1C	ZSSC3015 Die — Temperature range: -50°C to +150°C	Sawn on Wafer Frame
ZSSC3015NE2T(R)	ZSSC3015 SOP8 (150 mil) — Temperature range: -50°C to +150°C	Tube: add "-T" to sales code. Reel: add "-R"
ZSSC3015KIT	ZSSC3015 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB cable, 5 IC samples, instructions for downloading SSC Evaluation Software	Kit

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1 Electrical Characteristics

1.1. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. The ZSSC3015 might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

Parameter	Symbol	Min	Max	Unit
Analog Supply Voltage	V_{DD}	-0.3	6.0	V
Voltages at Analog I/O – In Pin	V_{INA}	-0.3	VDD+0.3	V
Voltages at Analog I/O – Out Pin	V_{OUTA}	-0.3	VDD+0.3	V
Electrostatic Discharge – Human Body Model (see section 7)		±4000		V
Storage Temperature Range (≥10 hours)	T_{STOR}	-50	150	°C
Storage Temperature Range (<10 hours)	$T_{STOR <10h}$	-50	170	°C

1.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Analog Supply Voltage to Ground	V_{DD}	2.7	5.0	5.5	V
Analog Supply Voltage (with external JFET Regulator)	V_{SUPP}	5.5	7	30	V
Common Mode Voltage	V_{CM}	1		V_{DDA} – 1.3	V
Ambient Temperature Range [1), 2)]	T_{AMB}	-50		150	°C
External Capacitance between V_{DD} and Ground	C_{VDD}	100	220	470	nF
Output Load Resistance to V_{SS} or V_{DD} [3)]	$R_{L,OUT}$	5			kΩ
Output Load Capacitance [4)]	$C_{L,OUT}$		10	15	nF
Bridge Resistance [5), 6)]	R_{BR}	0.3		100	kΩ
Power-On Rise Time	t_{PON}			100	ms

1) Note that the maximum EEPROM programming temperature is 85°C.

2) If buying die, designers should use caution not to exceed maximum junction temperature by proper package selection.

3) Only needed for Analog Output Mode; not needed for Digital Output Mode. When a pull-down resistor is used as load resistor, the power loss detection diagnostic for loss of VSS cannot be assured at RL=5k; RL=10k is recommended for this configuration.

4) Using the output for digital calibration, CL,OUT is limited by the maximum rise time tZAC,rise. See section 1.3.

5) Note: Minimum bridge resistance is only a factor if using the Bsink feature. The RDS(ON) of the Bsink transistor is 8 to 10Ω when operating at VDD=5V. This gives rise to a ratiometricity inaccuracy that becomes greater with low bridge resistances.

6) Note: Minimum bridge resistance is important if using certain diagnostic features. It must be at least 0.3kΩ at V_{DD}=2.7V and at least 0.6kΩ at V_{DD}=5V for the Sensor Short Check to function properly. For details, see section 2.6.3.

1.3. Electrical Parameters

Note: See important table notes at end of table. For parameters marked with an asterisk * there is no verification in mass production; the parameter is guaranteed by design and/or quality observation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	5.0	5.5	V
Supply Current (varies with update rate and output mode)	I_{DD}	At slowest update rate		0.3		mA
		At fastest update rate		1.0	1.4	
Temperature Coefficient – PTAT Source *	T_{CPTAT}			20	100	ppm/K
Power Supply Rejection Ratio*	PSRR		60			dB
Power-On Reset Level	POR		1.4		2.6	V
EEPROM						
Number Write Cycles	n_{WRI_EEP}	At 85°C			100k	Cycles
Data Retention	t_{WRI_EEP}	At 100°C			10	Years
Analog Front-End (AFE)						
Leakage Current—Pins VBP and VBN	I_{IN_LEAK}	Sensor connection and short check must be disabled. See sections 2.6.2 and 2.6.3.			±10	nA
Analog-to-Digital Converter (ADC)						
ADC Resolution	r_{ADC}				14	Bit
Integral Nonlinearity (INL) 1)	INL_{ADC}	Based on ideal slope.			±8	LSB
Differential Nonlinearity (DNL)*	DNL_{ADC}				±1	LSB
Digital-to-Analog Converter (DAC) and Buffer for Analog Output						
Maximum Output Current	I_{OUT}	Maximum current maintaining accuracy.	2.2			mA
Resolution	Res	Referenced to V_{DD}.			12	Bit
Absolute Error	E_{ABS}	DAC input to output.			±0.2%	V_{DD}
Differential Nonlinearity *	DNL	No missing codes.	-0.9		+3.0	LSB_{12Bit}
Upper Output Voltage Limit	V_{OUT}	R_L = 5 kΩ.	95%			V_{DD}
Lower Output Voltage Limit	V_{OUT}	With 5kΩ pull down, 0-1V output.			16.5mV	mV
Output Short Circuit Protection Limit	I_{SC}	Depends on operating conditions. Short circuit protection must be enabled via Diag_cfg (EEPROM word [102:100]). See section 2.4.2.	3		20	mA
Analog Output Noise Peak-to-Peak	$V_{NOISE,PP}$	Shorted input.			5±1LSB	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diagnostics						
Upper Diagnostic Output Level	$V_{DIA,H}$		97.5%			V_{DD}
Lower Diagnostic Output Level	$V_{DIA,L}$				2.5%	V_{DD}
Minimum Load Resistor for Power Loss	R_{L,OUT_PS}	Pull-up or pull-down[2] in Analog Output Mode	5			kΩ
External Temperature Measurement						
ExtTemp Signal Input Range	V_{TSE}		150		800	mV
Required External Temperature Diode Sensitivity	ST_{TSE}		1.9		3.25	mV/K
Temperature Span with External Temperature Diode	T_{TSE_SP}		-50		150	°C
ZACwire™ Serial Interface						
See section 3.3.1 for specifications related to the ZACwire™ serial interface.						
System Response						
Start-Up Time (Power-up to data output)	t_{STA}	Fast Startup	6		8	ms
Response Time – Analog Output	t_{RESP-A}	Update_rate = 0	0.88	1.4	3.2	ms
Response and Transmission Time for Digital Output	$t_{RES, DIG}$	Update_rate = 0	1.7	2.75	5.5	ms
Overall Linearity Error– Digital	E_{LIND}	Bridge input to output		0.025	0.04	%
Overall Linearity Error – Analog	E_{LINA}	Bridge input to output		0.1	0.2	%
Overall Ratiometricity Error	RE_{out}	±10%VDD; not using Bsink feature		0.025	0.1	%
Overall Accuracy – Digital (only IC, without sensor bridge)	AC_{outD}	-25°C to 85°C			±0.1%	%FSO
		-50°C to 150°C			±0.25%	
Overall Accuracy – Analog [3), 4)] (only IC, without sensor bridge)	AC_{outA}	-25°C to 85°C			±0.35%	%FSO
		-50°C to 150°C			±0.5%	

1) Note: This is ± 8 LSBs for the 14-bit analog-to-digital conversion. This results in absolute accuracy to 11-bits on the conversion result. Nonlinearity is typically better at temperatures less than 125°C.

2) When using a pull-down resistor as load resistor, the power loss detection diagnostic for loss of VSS cannot be assured at RL=5k; RL=10k is recommended for this configuration.

3) Not included is the quantization noise of the DAC. The 12-bit DAC has a quantization noise of ± ½ LSB = 0.61mV (@ 5V VDD) = 0.0125%.

4) Analog output range 2.5% to 95%.

1.4. Analog Inputs versus Output Resolution

The ZSSC3015 has a fully differential chopper-stabilized pre-amplifier with 4 programmable gain settings. The output of the pre-amplifier is input to a 14-bit charge-balanced ADC. Span, offset, temperature, and nonlinearity correction are performed in the digital domain. Then the resulting corrected bridge value can be output in analog form through a 12-bit DAC or as a 16-bit serial digital packet. The resolution of the output depends on the input span (bridge sensitivity) and the analog gain setting programmed. Digital gains can vary from [0,32). Analog gains available are 6, 24, 48, and 96.

Note: At higher analog gain settings, there will be higher output resolution, but the ability of the ZSSC3015 to handle large offsets decreases. This is expected because the offset is also amplified by the analog gain and can therefore saturate the ADC input.

The following tables outline the guaranteed minimum resolution for a given bridge sensitivity range.

Table 1.1 ADC Resolution Characteristics for an Analog Gain of 6

Analog Gain 6				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
57.8	80.0	105.8	38%	12.4
50.6	70.0	92.6	53%	12.2
43.4	60.0	79.4	73%	12.0
36.1	50.0	66.1	101%	11.7
28.9	40.0	52.9	142%	11.4
21.7	30.0	39.7	212%	11.4

1) In addition to Tco, Tcg.

Table 1.2 ADC Resolution Characteristics for an Analog Gain of 24

Analog Gain 24				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
18.1	25.0	33.1	17%	12.7
14.5	20.0	26.5	38%	12.4
7.2	10.0	13.2	142%	11.4
3.6	5.0	6.6	351%	10.4
1.8	2.5	3.3	767%	9.4
0.9	1.2	1.6	1670%	8.4

1) In addition to Tco, Tcg.

Important Note: The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

Table 1.3 ADC Resolution Characteristics for an Analog Gain of 48

Analog Gain 48				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
10.8	15.0	19.8	3%	13.0
7.2	10.0	13.2	38%	12.4
4.3	6.0	7.9	107%	11.7
2.9	4.0	5.3	194%	11.1
1.8	2.5	3.3	351%	10.4
1.0	1.4	1.85	678%	9.6
0.72	1.0	1.32	976%	9.1

1) In addition to Tco, Tcg.

Important Note: The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

Table 1.4 ADC Resolution Characteristics for an Analog Gain of 96

Analog Gain 96				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
4.3	6.0	7.9	21%	12.7
2.9	4.0	5.3	64%	12.1
1.8	2.5	3.3	142%	11.4
1.0	1.4	1.85	306%	10.6
0.72	1.0	1.32	455%	10.1

1) In addition to Tco, Tcg.

2 Circuit Description

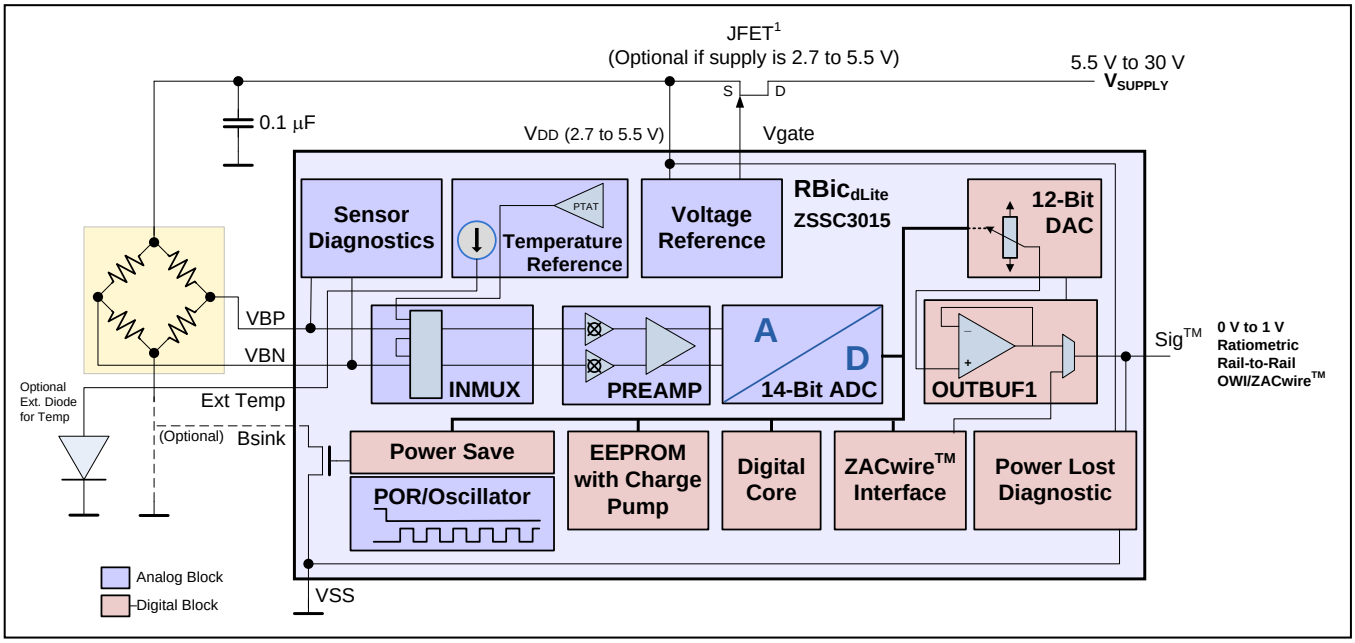
2.1. Signal Flow and Block Diagram

The ZSSC3015 resistive bridge sensor interface ICs were specifically designed as cost-effective solutions for sensing in building automation, automotive, industrial, office automation, and white goods applications. The ZSSC3015 employs IDT's high precision bandgap with proportional-to-absolute-temperature (PTAT) output; low-power 14-bit analog-to-digital converter (ADC, A2D, A-to-D); and an on-chip digital signal processor (DSP) core with EEPROM to precisely calibrate the bridge output signal.

Three selectable outputs, two analog and one digital, offer the ultimate in versatility across many applications. The ZSSC3015 rail-to-rail ratiometric analog V_{out} signal (0V to ~5 V V_{out} @ V_{DD}=5V) suits most building automation and automotive requirements (12-bit resolution). Typical office automation and white goods applications require the 0 to ~1V V_{out} signal, which in the ZSSC3015 is referenced to the internal bandgap. The ZSSC3015 is capable of running in high-voltage (5.5 to 30 V) systems when combined with an external JFET.

Direct interfacing to µP controllers is facilitated via IDT's single-wire serial ZACwire™ digital interface.

Figure 2.1 ZSSC3015 Block Diagram



2.2. Analog Front End

2.2.1. Bandgap/PTAT and PTAT Amplifier

The highly linear Bandgap/PTAT section provides the PTAT signal to the ADC, which allows accurate temperature conversion. In addition, the ultra-low ppm Bandgap section provides a stable voltage reference over temperature for the operation of the rest of the ZSSC3015. If the bridge is not near the ZSSC3015, an external diode can be used for temperature measurement/compensation.

The temperature signal (internal PTAT or external diode) is amplified through a path in the PREAMP block and fed to the ADC for conversion. The most significant 12-bits of this converted result are used for temperature measurement and temperature correction of bridge readings. When temperature is output in Digital Mode, only the most significant 8 bits are given.

When external temperature is selected, add a diode from the ExtTemp pin to ground. The diode is biased with approximately 50µA during temperature measurement cycles. The voltage level on ExtTemp is amplified through the PREAMP section and converted by the ADC. Ensure that the ExtTemp signal is in the range of 150mV to 800mV to prevent saturation of the ADC. If the selected diode has a sensitivity in the range of 1.9mV/^{o}C to 3.25mV/^{o}C, a corrected temperature output (in Digital Mode) can be achieved for a 200^{o}C temperature span (-50^{o}C to 150^{o}C).

2.2.2. Bridge Supply

The voltage-driven bridge is usually connected to V_{DD} and ground. As a power savings feature, the ZSSC3015 also includes a switched transistor to interrupt the bridge current via pin 1 (Bsink). The transistor switching is synchronized to the analog-to-digital conversion and released after finishing the conversion. To utilize this feature, the low supply of the bridge should be connected to Bsink instead of ground.

Depending on the programmable update rate, the average current consumption (including bridge current) can be reduced to approximately 20%, 5%, or 1%. Note this feature has no power savings benefit if using the fastest update rate mode.

2.2.3. PREAMP Block

The differential signal from the bridge is amplified through a chopper-stabilized instrumentation amplifier with very high input impedance designed for low noise and low drift. This pre-amp provides gain for the differential signal and re-centers its DC to V_{DD}/2. The output of the PREAMP section is fed into the ADC. The calibration sequence performed by the digital core includes an auto-zero sequence to null any drift in the pre-amp state over temperature.

The pre-amp can be set to a gain of 6, 24, 48, or 96 through EEPROM. See Pamp_Gain in section 3.6.

The inputs to the pre-amp from (VBN/VBP pins) can be reversed via an EEPROM configuration bit. See “flip polarity” under A2D_Offset in section 3.6.

2.2.4. Analog-to-Digital Converter (ADC)

A 14-bit 2nd order charge-balancing ADC is used to convert signals coming from the pre-amplifier. The converter, designed in full differential switched capacitor technique, is used for converting the various signals in the digital domain.

This principle offers the following advantages:

- High noise immunity because of the differential signal path and integrating behavior
- Independence from clock frequency drift and clock jitter
- Fast conversion time due to second order mode

Parameters of the ADC can be controlled with EEPROM settings given in section 3.6.

Four selectable values for the zero point of the input voltage allow conversion to adapt to the sensor's offset parameter. With the Flip Polarity Mode and the negative digital gain options, this results in seven possible zero point adjustments (not eight because the -1/2,1/2 offset setting is the same regardless of gain polarity).

The conversion rate varies with the programmed update rate. The fastest conversation rate is 1k samples/s. Based on a best fit, the integral nonlinearity (INL) is less than 4 LSB_{14Bit}.

2.3. Digital Signal Processor

A digital signal processor (DSP) is used for processing the converted bridge data as well as performing temperature correction and computing the temperature value for output on the digital channel.

The digital core reads correction coefficients from EEPROM and can correct for the following:

- Bridge Offset
- Bridge Gain
- Variation of Bridge Offset over Temperature (Tco)
- Variation of Bridge Gain over Temperature (Tcg)
- A single second-order effect (SOT) (Second Order Term)

The EEPROM contains a single SOT that can be applied to correct one and only one of the following:

- 2nd order behavior of bridge measurement
- 2nd order behavior of Tco
- 2nd order behavior of Tcg

If the SOT applies to correcting the bridge reading, then the correction formula for the bridge reading is represented as a two-step process as follows:

$$ZB = Gain\_B(1 + \Delta T * Tcg) * (BR\_Raw -/+ Offset\_B + \Delta T * Tco) \quad (1)$$

$$RB = ZB(1.25 + SOT * ZB) \quad (2)$$

Where:

BR = Corrected Bridge reading that is output as digital or analog on Sig™ pin

ZB = Intermediate result in the calculations

BR_Raw = Raw Bridge reading from ADC

T_Raw = Raw Temp reading converted from PTAT signal or external diode

Gain_B = Bridge Gain term

Offset_B = Bridge Offset term

Offset_B_sign = Sign bit for Bridge Offset term

Tcg = Temperature Coefficient Gain

Tco = Temperature Coefficient Offset

ΔT = ($T\_Raw - T_{SETL}$)

T_{SETL} = T_Raw reading at which low calibration was performed (typically 25°C)

SOT = Second Order Term

If the **SOT** applies to correcting the 2nd order behavior of **Tco**, then the formula for bridge correction is as follows:

$$BR = Gain\_B(1 + \Delta T * Tcg) * [BR\_Raw -/+ Offset\_B + \Delta T(SOT * \Delta T + Tco)] \quad (3)$$

If the **SOT** applies to correcting the 2nd order behavior of Tcg, then the formula for bridge correction is as follows:

$$BR = Gain\_B[1 + \Delta T(SOT * \Delta T + Tcg)] * [BR\_Raw -/+ Offset\_B + \Delta T * Tco] \quad (4)$$

The bandgap reference gives a very linear PTAT signal, so temperature correction can always simply be accomplished with a linear gain and offset term.

Corrected Temperature Reading:

$$T = Gain\_T(T\_Raw + Offset\_T) \quad (5)$$

Where:

T_Raw = Raw Temperature reading converted from PTAT signal or external diode

Offset_T = Offset Coefficient for Temperature

Gain_T = Gain Coefficient for Temperature

2.3.1. EEPROM

The EEPROM contains the calibration coefficients for gain and offset, etc., and the configuration bits, such as output mode, update rate, etc. The ZSSC3015 also offers 3 user-programmable storage bytes for module traceability. When programming the EEPROM, an internal charge pump voltage is used; therefore a high voltage supply is not needed. The EEPROM is implemented as a shift register. During an EEPROM read, the contents are shifted 8 bits before each transmission of one byte occurs. The charge pump is internally regulated to 12.5 V, and the programming time is 6ms.

See section 2.6.1 regarding EEPROM signatures for verifying EEPROM integrity.

Note: EEPROM writing can only be performed at temperatures lower than 85ºC.

2.3.2. One-Wire Interface – ZACwire™

The ZSSC3015 communicates via a one-wire serial interface. There are different commands available for the following:

- Reading the conversion result of the ADC (Get_BR_Raw, Get_T_Raw)
- Calibration commands
- Reading from the EEPROM (dump of entire contents)
- Writing to the EEPROM (trim setting, configuration, and coefficients)

2.4. Output Stage

2.4.1. Digital to Analog Converter (Output DAC) with Programmable Clipping Limits

A 12-bit DAC based on sub-ranging resistor strings is used for the digital-to-analog output conversion in the analog ratiometric and absolute analog voltage modes. Options during calibration configure the system to operate in either of these modes. The design allows for excellent testability as well as low power consumption.

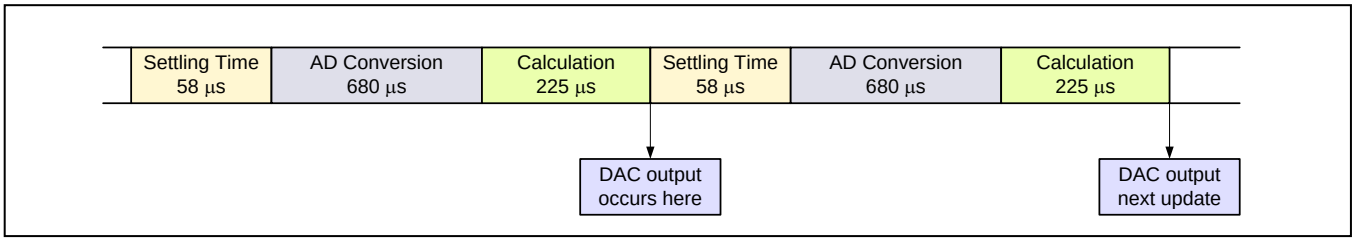
The DAC allows programming a lower and upper clipping limit for the output signal (analog and digital). See Up_Clip_Lim and Low_Clip_Lim in section 3.6. The internal 14-bit calculated bridge value is compared against the 14-bit value formed by {11,Up_Clip_Lim[6:0],11111} for the upper limit and {00,Low_Clip_Lim[6:0],00000} for the lower limit. If the calculated bridge value is higher than the upper limit or less than the lower limit, the analog output value is clipped to this value; otherwise it is output as is.

Example for the upper clipping level: If the Up_Clip_Lim[6:0] = 0000000, then the 14-bit value used for the clipping threshold is 11000000011111. This is 75.19% of full scale. Since there are 7 bits of upper clipping limit, there are 127 possible values between 75.19% and 100%. Therefore the resolution of the clipping limits 0.195%.

Example for the lower clipping level: If the Low_Clip_Lim[6:0] = 1111111, then the 14-bit value used for the clipping threshold is 00111111100000. This is 24.8% of full scale. Since there are 7 bits of lower clipping limit, there are 127 possible values between 0 and 24.8%. Therefore the resolution of the lower clipping limit is 0.195%.

Figure 2.2 shows the data timing of the DAC output for the update rate setting 00. Refer to the *ZSSC3015 Response Time Spreadsheet* for details.

Figure 2.2 DAC Output Timing for Highest Update Rate



2.4.2. Output Buffer and Output Short Circuit Protection

A rail-to-rail op amp configured as a unity gain buffer can drive resistive loads (whether pull-up or pull-down) as low as 5kΩ and capacitances up to 15nF (for pure analog output). In addition, to limit the error due to amplifier offset voltage, an error compensation circuit is included which tracks and reduces offset voltage to < 1mV.

The output of the ZSSC3015 output can be permanently shorted to VDD or VSS without damaging the device. The output driver contains a current-limiting block that detects a hard short and limits the current to a safe level. The output short circuit protection current can vary from a minimum of 3mA to a maximum of 20mA depending on operating conditions. Output short circuit protection can be enabled via Diag_cfg (EEPROM [102:100]). Enabling this protection is recommended when using the analog output. See Table 3.6 for settings.

2.4.3. Voltage Reference Block

A linear regulator control circuit is included in the Voltage Reference block to interface with an external JFET to allow operation in systems where the supply voltage exceeds 5.5V. This circuit can also be used for over-voltage protection. The regulator set point has a coarse adjustment controlled by the JFET_cfg EEPROM bits that can adjust the set point around 5.0 or 5.5V. (See Table 3.6 for bit locations and section 2.3.1 regarding writing to the EEPROM.). The 1V trim setting (see below) can also act as a fine adjust for the regulation set point. The 5V reference can be trimmed within +/-15mV.

Note: If using the external JFET for over-voltage protection purposes (i.e., 5V at JFET drain and expecting 5V at JFET source), there will be a voltage drop across the JFET; therefore ratiometricity will be slightly compromised depending on the rds(on) of the chosen JFET. A J107 is the best choice because it has only an 8mV drop worst case. If using as regulation instead of over-voltage, a MMBF4392 or BSS169 also works well.

The Voltage Reference block uses the absolute reference voltage provided by the bandgap to produce two regulated on-chip voltage references. A 1V reference is used for the output DAC high reference when the part is configured in 0-1V Analog Output Mode. For this reason, the 1V reference must be very accurate and includes trim so that its value can be trimmed within +/- 3mV of 1.00V. The 1V reference is also used as the on-chip reference for the JFET regulator. The regulation set point of the JFET regulator can be fine-tuned using the 1V trim.

The reference trim setting is selected with the 1V_Trim/JFET_Trim bits in EEPROM. See Table 3.6 for bit locations. Table 2.1 shows the order of trim codes with 0111 for the lowest reference voltage and 1000 for the highest reference voltage.

Important: Optimal reference trim is determined during wafer-level testing and final package testing. Back-up copies of these bits are stored in bits in the CUST_ID0 bits for applications requiring accurate references. In this case, see section 5 for important notes and instructions for verifying the integrity of the 1V_Trim/JFET_Trim bits and if necessary, restoring the value from the CUST_ID0 bits before calibration.

Table 2.1 1V Reference Trim (1V vs. Trim for Nominal Process Run)

Order	1Vref/ 5Vref_trim3	1Vref/ 5Vref_trim2	1Vref/ 5Vref_trim1	1Vref/ 5Vref_trim0
Highest Reference Voltage	1	0	0	0
…	1	0	0	1
…	1	0	1	0
…	1	0	1	1
…	1	1	0	0
…	1	1	0	1
…	1	1	1	0
…	1	1	1	1
…	0	0	0	0
…	0	0	0	1
…	0	0	1	0
…	0	0	1	1
…	0	1	0	0
…	0	1	0	1
…	0	1	1	0
Lowest Reference Voltage	0	1	1	1

2.5. Clock Generator / Power-On Reset (CLKPOR)

If the power supply exceeds 2.5V (maximum), the reset signal de-asserts and the clock generator starts operating at a frequency of approximately 570kHz (±10%). The exact value only influences the conversion cycle time and communication to the outside world but not the accuracy of signal processing.

2.6. Diagnostic Features

The ZSSC3015 offers a full suite of diagnostic features to ensure robust system operation in the most “mission-critical” applications. If the part is programmed in Analog Output Mode, then diagnostic states are indicated by an output below 2.5% of VDD or above 97.5% of VDD. If the part is programmed in Digital Output Mode, then diagnostic states will be indicated by a transmission with a generated parity error.

Table 2.2 gives a summary of the diagnostic features, which are explained in detail in the following sections. EEPROM settings that control diagnostic functions are given in section 3.6.

Table 2.2 Summary of Diagnostic Features

Detected Fault	Analog Diagnostic Level	ZACwire™ Diagnostic	Delay in Detection*
EEPROM signature	Lower	Generates parity error	11ms after power-on†
Loss of bridge positive	Upper	Generates parity error	2ms
Loss of bridge negative	Upper	Generates parity error	2ms
Open bridge connection	Upper	Generates parity error	2ms
Bridge input short	Upper	Generates parity error	2ms
ExtTemp pin open	Lower	Generates parity error	300ms
ExtTemp pin shorted to PWR/GND	Lower	Generates parity error	300ms
ExtTemp pin shorted to BP/BN‡	Upper	Generates parity error	3ms
Loss of VDD	Lower	Transmissions stop	Dependent on R_L and C_L
Loss of VSS	Upper	Transmissions stop	Dependent on R_L and C_L

2.6.1. EEPROM Integrity

The contents of the EEPROM are protected by an 8-bit LFSR signature (linear feedback shift register). This signature is regenerated and stored in EEPROM every time EEPROM contents are changed. This signature is generated and checked for a match after Power-On Reset prior to entering Normal Operation Mode. If the generated signature fails to match, the part will output a diagnostic state on the output.

In addition to an extensive temporal and code interlock mechanism used to prevent false writes to the EEPROM, the ZSSC3015 offers an EEPROM lock mechanism for high-security applications. When EEPROM bits 105:103 are programmed with “011” or “110,” this 3-bit field will disable the VPP charge pump and will not allow further writes to the EEPROM.

2.6.2. Sensor Connection Check

Four dedicated comparators permanently check the range of the bridge inputs (BP/BN) to ensure they are within the envelope of 0.8V to 0.85∗VDD during all conversions. The two sensor inputs have a switched ohmic path to ground and if left floating, would be discharged. If any of the wires connecting the bridge break, this mechanism will detect it and put the ZSSC3015 in a diagnostic state. This same diagnostic feature can also detect a short between BP/BN and the ExtTemp signal if an external diode is being used for temperature measurement. See Table 2.2 in section 2.6 for more information.

* All timings assume nominal operating frequency of 570kHz.
† Assumes standard command window. If fast startup is enabled, the delay is 4ms.
‡ A short from ExtTemp to BP/BN might not be detected in some circuit configurations.

2.6.3. Sensor Short Check

If a short occurs between BP/BN (bridge inputs), it would normally produce an in-range output signal and therefore would not be detected as a fault. This diagnostic mode, if enabled, will deliberately look for such a short. After the measurement cycle of the bridge, it will deliberately pull the BP bridge input to ground for 4µsec. At the end of this 4µsec window, it will check to see if the BN input "followed" it down below the 0.8V comparator checkpoint. If so, a short must exist between BP/BN, and the ZSSC3015 will output a diagnostic state. The bridge will have a minimum of 480µsec recovery time prior to the next measurement. See Table 2.2 in section 2.6 for more information.

The bridge resistance must be taken into account if the Sensor Short diagnostic feature is used. At V_{DD} = 2.7V, the minimum bridge resistance is 0.3KΩ, and at V_{DD} = 5V, the minimum bridge resistance is 0.6KΩ.

2.6.4. Power Loss Detection

If the power or GND connection to the module containing the sensor bridge and ZSSC3015 is lost, the ZSSC3015 will output a diagnostic state if a pull-up or pull-down terminating resistor greater than or equal to 5kΩ is connected in the final application. This diagnostic mode only functions when the part is configured in Analog Output Mode. For more information, see Table 2.2 in section 2.6.

2.6.5. ExtTemp Connection Checks

When external temperature is selected and connection checking is enabled, the part performs range checking on the converted temperature value. If the internal ADC reading of the temperature is less than 1/32 of full scale or greater than 63/64 of full scale then a diagnostic state is asserted. If the ExtTemp pin is shorted to ground, the ADC reads less than 1/32. Because 100µA is sourced onto the ExtTemp pin during conversions, it naturally pulls up during these times. If the ExtTemp pin is open, it produces an ADC reading greater than 63/64 of full scale. Both these bad connection conditions would be detected and result in a diagnostic output. If internal temperature is selected or sensor connection check is not enabled, then this diagnostic check is not enabled. See Table 2.2 in section 2.6 for more information.

3 Functional Description

3.1. General Working Mode

The command/data transfer takes place via the one-wire Sig™ pin using the ZACwire™ serial communication protocol.

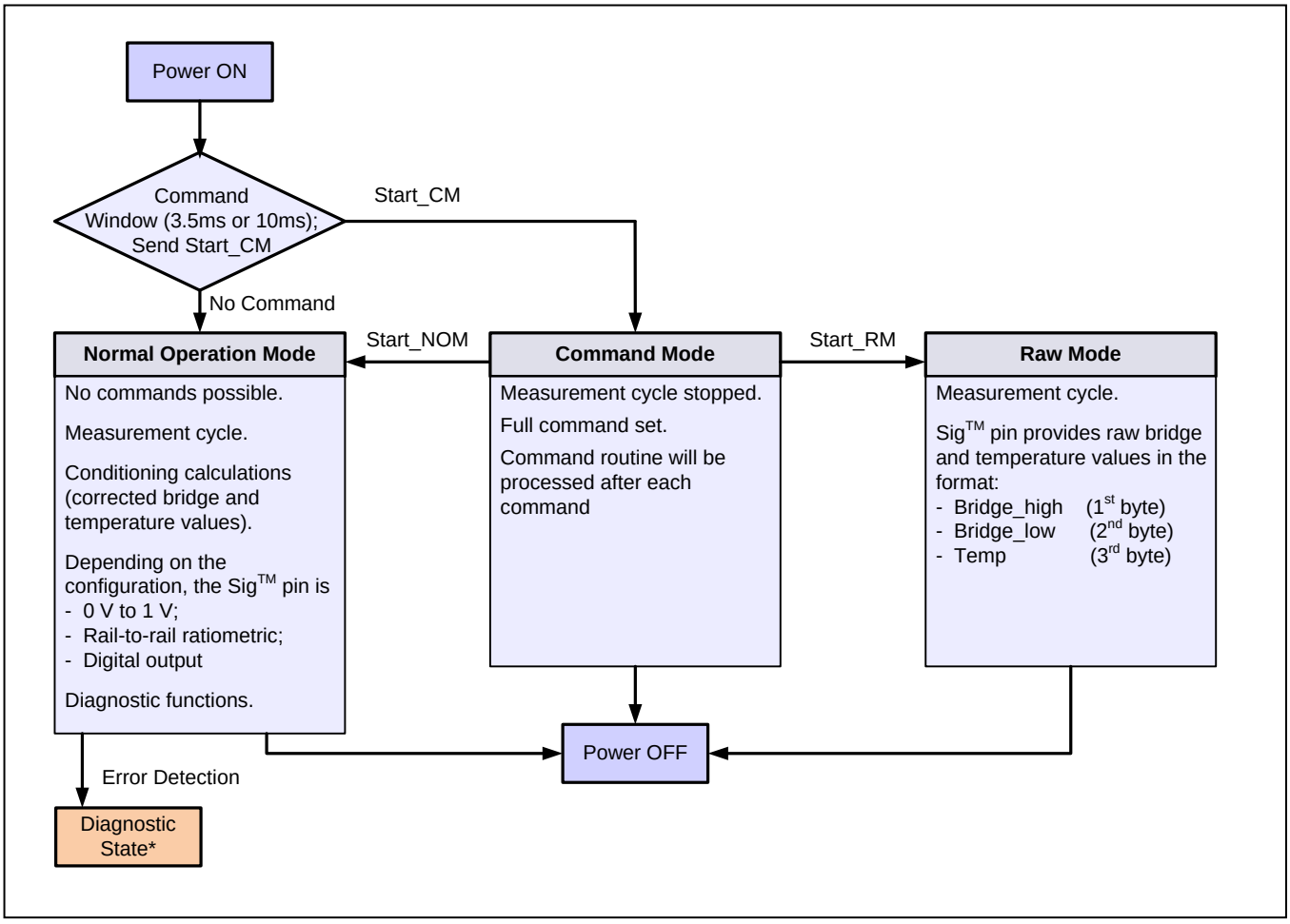
After power-on, the ZSSC3015 provides a command window for 3.5ms or 10ms. (The command window length depends on the setting of the Fast_Startup EEPROM bit; see section 3.6). During the command window, the ZSSC3015 is waiting for a Start_CM command. Without this command, the Normal Operation Mode (NOM) starts. In this mode, raw bridge values are converted and the corrected values are presented on the output in analog or digital format (depending on the configuration stored in EEPROM). If the ZSSC3015 receives the Start_CM command during the command window, it remains in Command Mode (CM). The CM allows changing to one of the other modes via command. (See section 3.4 for command encoding.) If the Start_RM command is sent, the ZSSC3015 enters the Raw Mode (RM). Without correction, the raw values are transmitted to the digital output in a predefined order. The RM can only be stopped by a power down. Raw Mode is used by the calibration software for collection of raw bridge and temperature data so the correction coefficients can be calculated.

If diagnostic features are enabled and a diagnostic fault is detected, diagnostic states are indicated as follows depending on the programmed mode:

- In Analog Output Mode:
  Diagnostic states are indicated by an output below 2.5% of VDD or above 97.5% of VDD.
- In Digital Output Mode:
  Diagnostic states will be indicated by a transmission with a generated parity error.

For more details, see section 2.6.

Figure 3.1 General Working Mode



* See section 2.6.

3.2. Normal Mode Sample Rate

When the ZSSC3015 is in Normal Operation Mode, the output rate depends mainly on the settings for the update rate and Output Mode. Table 3.1 shows the nominal sample rate for analog output across update rate settings for Analog Output Mode. See section 3.3.4 for information on reading the ZSSC3015 and the overall update and transmission time when in Digital Mode. The average response time shown in Table 3.1 accounts for 1.5 samples at nominal frequency and temperature. The worst-case response time accounts for process and temperature deviation on the oscillator. The worst case only occurs if the input changes immediately prior to a special measurement. See the *ZSSC3015 Response Time Spreadsheet* for details on the average and worst-case response time depending on the ZSSC3015 configuration.

Table 3.1 Update Rate for Analog Output

Update Rate Setting	Sample Rate	Average Response Time	Worst Case Response Time	Unit
00	0.96	1.44	3.3	ms
01	4.4	6.68	15.7	ms
10	20.2	31.58	72.4	ms
11	105.2	171.02	377.4	ms

3.3. ZACwire™ Communication Interface

3.3.1. Properties and Parameters

Table 3.2 ZACwire™ Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Comments
ZACwire™ frequency [1]	f_{ZAC}	30	36	40	kHz	Command Mode or Update Rate = 0 or 1
		7	9	10		Update Rate = 2 or 3
Pull-up resistor (on-chip)	$R_{ZAC,pu}$		30		kΩ	On-chip pull-up resistor switched on during Digital Output Mode and during Command Mode (first 3ms after power up)
Pull-up resistor (external)	R_{ZAC,pu_ext}	150			Ω	If the master communicates via a push-pull stage, no pull-up resistor is needed; otherwise, a pull-up resistor with a value of at least 150Ω must be connected.
ZACwire™ rise time	$t_{ZAC,rise}$			5	µs	Any user RC network included in Sig™ path must meet this rise time
ZACwire™ line resistance [2]	$R_{ZACload}$			3.9	kΩ	
ZACwire™ load capacitance [2]	$C_{ZAC,load}$	0	1	15	nF	
Voltage low level [3]	$V_{ZAC,low}$		0	0.2	V_{DD}	Rail-to-rail CMOS driver
Voltage high level [3]	$V_{ZAC,high}$	0.8	1		V_{DD}	Rail-to-rail CMOS driver

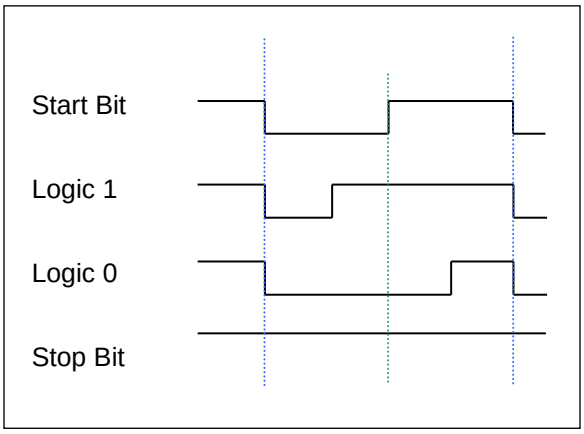
1) Output frequency only. The master should communicate with the ZSSC3015 at 20kHz to 52kHz when it is in Command Mode.

2) The rise time must be $t_{ZAC,rise} = 2 * R_{ZACload} * C_{ZACload} \leq 5\mu s$. If using a pull-up resistor instead of a line resistor, it must meet this specification. The absolute maximum for $C_{ZACload}$ is 15nF.

3) No verification in mass production; the parameter is guaranteed by design and/or quality observation.

3.3.2. Bit Encoding

Figure 3.2 Manchester Duty Cycle



Start bit = 50% duty cycle used to set up strobe time

Logic 1 = 75% duty cycle

Logic 0 = 25% duty cycle

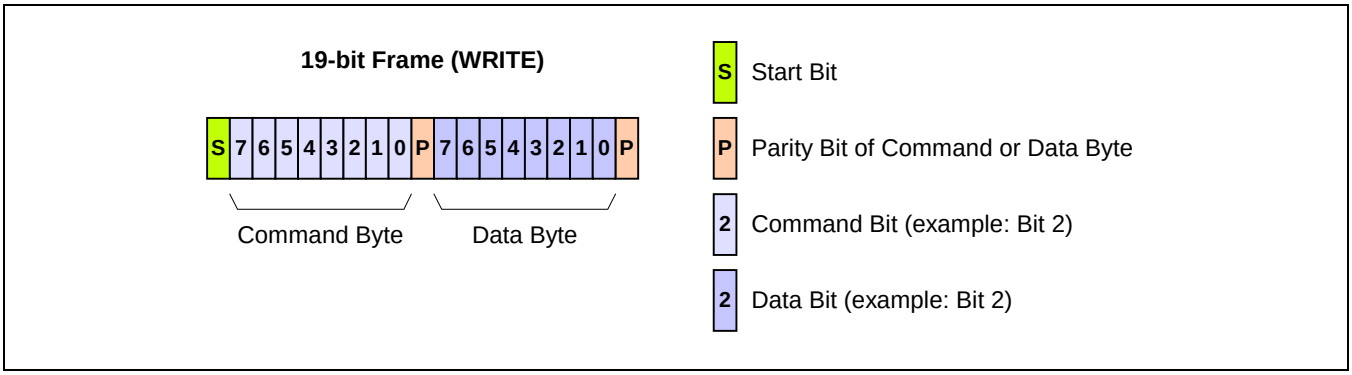
Stop Bit = The ZACwire™ bus will be held high for 1 bit length between consecutive data packets.

See *Technical Note – ZACwire™ Communication* for more details on the ZACwire™ protocol.

3.3.3. Write Operation from Master to ZSSC3015

The calibration master sends a 19-bit packet frame to the ZSSC3015.

Figure 3.3 19-Bit Write Frame



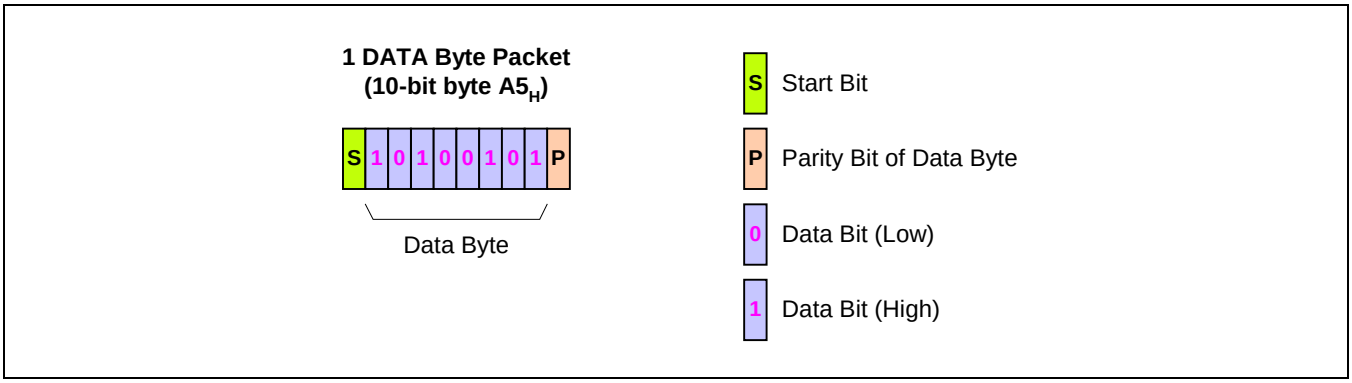
The incoming serial signal will be sampled at a 570kHz clock rate. This protocol is very tolerant to clock skew, and can easily tolerate a wide range of baud rates. The incoming baud rate should be in the 8kHz to 52kHz range (36kHz nominal).

3.3.4. ZSSC3015 Read Operations

The incoming frame will be checked for proper parity on both command and data bytes, as well as for any edge time-outs prior to a full frame being received.

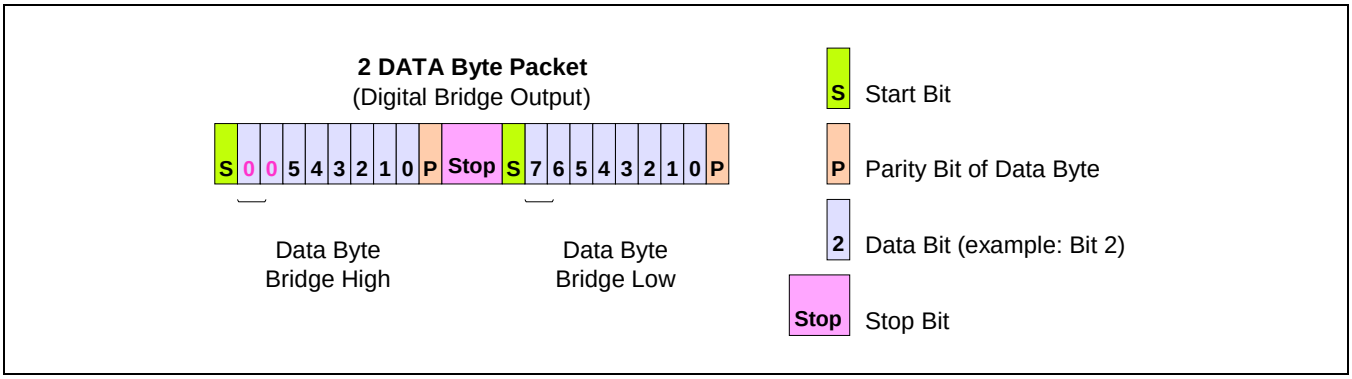
After a command/data pair is received, the ZSSC3015 will perform that command. After the command has been successfully executed by the ZSSC3015, it will acknowledge success by a transmission of an $A5_{HEX}$ byte back to the master. If the master does not receive an $A5_H$ transmission within 130ms of issuing the command, it must assume the command was either improperly received or could not be executed.

Figure 3.4 Read Acknowledge



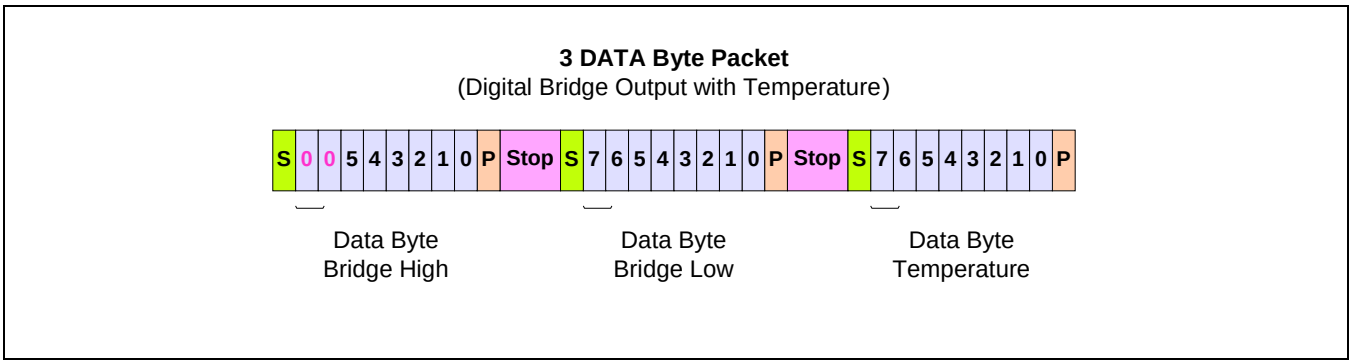
The ZSSC3015 transmits 10-bit bytes (1 start bit, 8 data bits, 1 parity bit). During calibration and configuration, transmissions are normally either $A5_{HEX}$ or data. $A5_{HEX}$ indicates successful completion of a command. There are two different digital output modes configurable (digital output with temperature and digital output with only bridge data). During Normal Operation Mode, if the part is configured for digital output of the bridge reading, it first transmits the high byte of bridge data, followed by the low byte. The bridge data is 14 bits in resolution, so the upper two bits of the high byte are always zero-padded. There is a stop bit time between bytes in a packet. This means that for the time of a bit width, the signal level is high.

Figure 3.5 Digital Output (NOM) Bridge Readings



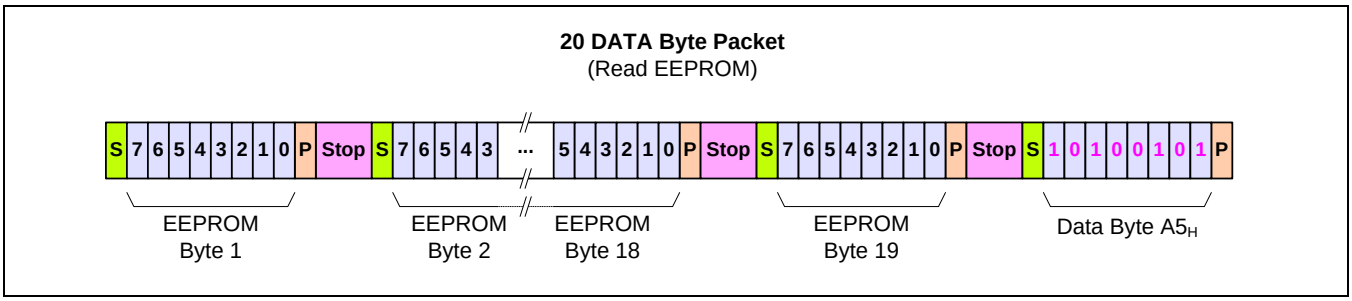
The second option for Digital Output Mode is digital output bridge reading with temperature. It will be transmitted as 3 data packets. The temperature byte represents an 8-bit temperature quantity spanning from -50 to 150°C.

Figure 3.6 Digital Output (NOM) Bridge Readings with Temperature



The EEPROM transmission occurs in a packet with 20 data bytes, as shown in Figure 3.7.

Figure 3.7 Read EEPROM Contents



There is a variable idle time between packets. This idle time varies with the update rate setting in EEPROM.

Figure 3.8 Transmission of a Number of Data Packets

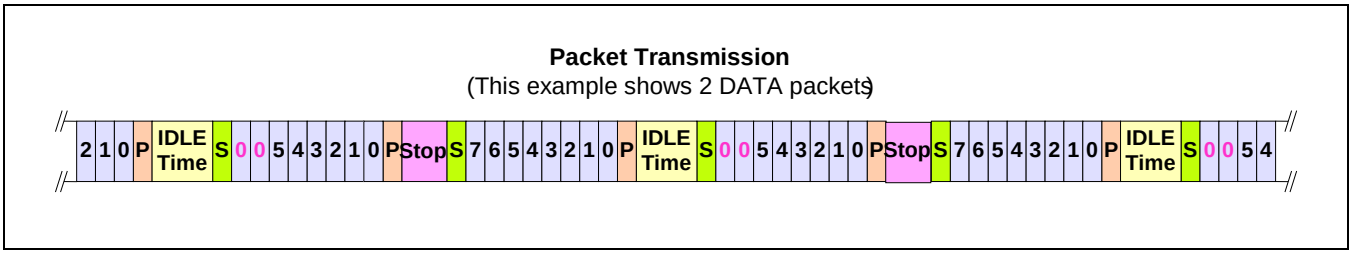


Table 3.3 shows the idle time between packets versus the update rate. This idle time can vary by nominal +/-15% between parts and over a temperature range of -50 to 150ºC. The idle time is extended by the time of one conversion at each special measurement.

Table 3.3 Idle Time between Packets versus Update Rate

Update Rate Setting	Idle Time between Packets	Idle Time at Special Measurements every (xx) Packets
00	1ms	1.83ms (128)
01	4.33ms	5.16ms (64)
10	20.3ms	21.1ms (16)
11	106ms	107ms (8)

Transmissions from the ZSSC3015 occur at one of two speeds depending on the update rate programmed in EEPROM. If the user chooses one of the two fastest update rates (00_{BIN} or 01_{BIN}) then the baud rate of the digital transmission will be 36kHz. However, if the user chooses one of the two slower update rates (10_{BIN} or 11_{BIN}), then the baud rate of the digital transmission will be 9kHz.

The total transmission time for both digital output configurations is shown in Table 3.4.

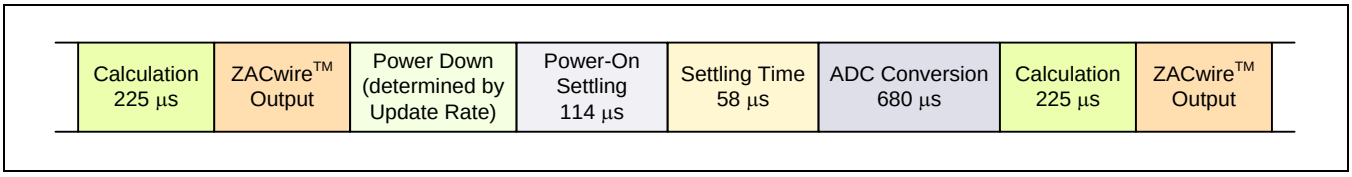
Table 3.4 Total Transmission Time for Different Update Rate and Output Configurations

Update Rate Setting	Baud Rate*	Idle Time	Transmission Time – Bridge Only Readings			Transmission Time – Bridge & Temperature Readings		
00	36 kHz	1.0 ms	21 bits	27.7 µs	1.6 ms	32 bits	27.7 µs	1.9 ms
01	36 kHz	4.33 ms	21 bits	27.7 µs	4.9 ms	32 bits	27.7 µs	5.2 ms
10	9 kHz	20.3 ms	21 bits	111.1 µs	22.6 ms	32 bits	111.1 µs	23.9 ms
11	9 kHz	106 ms	21 bits	111.1 µs	108.3 ms	32 bits	111.1 µs	109.6 ms

* Typical values. See Table 3.2 for details.

For lower update rates, the output is followed by a power-down as shown in Figure 3.9.

Figure 3.9 ZACwire™ Output Timing for Lower Update Rates



It is easy to program any standard microcontroller to communicate with the ZSSC3015. IDT can provide sample code for a MicroChip PIC® microcontroller.

3.3.5. High Level Protocol

The ZSSC3015 will listen for a command/data pair to be transmitted for the 3.5ms or 10ms (depending on the setting of the Fast_Startup EEPROM bit; see section 3.6) after the de-assertion of its internal Power-On Reset (POR). If a transmission is not received within this time frame, then it will transition to Normal Operation Mode (NOM). In the NOM, it will output bridge data in 0-1V analog, rail-to-rail ratiometric analog, or digital depending on how the part is currently configured.

If the ZSSC3015 receives a Start_CM command within the first 3.5ms or 10ms after the de-assertion of POR, then it will go into Command Mode (CM). In this mode, calibration/configuration commands will be executed. The ZSSC3015 will acknowledge successful execution of commands by transmission of $A5_{HEX}$. The calibrating /configuring master will know a command was not successfully executed if no response is received within 130ms after issuing the command. Once in command interpreting/executing mode, the ZSSC3015 will stay in this mode until power is removed or a Start_NOM (Start Normal Operation Mode) command is received. The Start_CM command is used as an interlock mechanism to prevent a spurious entry into Command Mode on power up. The first command received within the command window must be a Start_CM command to enter into command interpreting mode. Any other commands will be ignored.

3.4. Command/Data Bytes Encoding

The 2-byte command sent to the ZSSC3015 consists of 1 byte of command information and 1 byte of data information. Regardless of whether the command requires data or not, 2 bytes MUST be sent. Table 3.5 lists all the command/data pairings. (X=don't care.)

Table 3.5 Command/Data Bytes Encoding

Note: $_{HEX}$ = Hexadecimal

Command Byte	Data	Description		
00_{HEX}	XX_{HEX}	Read EEPROM command via Sig™ pin.[§]		
20_{HEX}	$5X_{HEX}$	DAC Ramp Test Mode. Gain_B[13:3] contains the starting point, and the increment is (Offset_B/8). The increment will be added every 125µsec.		
30_{HEX}	WD_{HEX} W = What D = Data	Trim/Configure: 3rd nibble determines what is trimmed/configured. The 4th nibble is data to be programmed.		
		3rd Nibble	4th Nibble Data	Description
		0_{HEX}	D_{HEX}	Program EEPROM bits [2:0] ZMDI_cfg[**]. Least significant 3 bits are used.
		1_{HEX}	D_{HEX}	Trim 1V reference. Least significant 4 bits of data used.
		2_{HEX}	D_{HEX}	Offset Mode. Least significant 4 bits of data used.
		3_{HEX}	D_{HEX}	Set output mode. Least significant 2 bits used.
		4_{HEX}	D_{HEX}	Set update rate. Least significant 2 bits used.
		5_{HEX}	D_{HEX}	Configure JFET regulation.
		6_{HEX}	D_{HEX}	Program the Tc_cfg register. Least significant 3 bits used. Most significant bit of data nibble should be 0.
		7_{HEX}	D_{HEX}	Program EEPROM bits [99:96] {SOT_cfg,Pamp_Gain}.
		D_{HEX}		Program EEPROM bits [105:103]:
			0x3	**EEPROM locked!** Int. PTAT used for temperature.
			0x0,0x1,0x2	EEPROM unlocked. Int. PTAT used for temperature.
			0x6	**EEPROM locked!** Ext. diode used for temperature.
			0x4,0x5,0x7	EEPROM unlocked. Ext. diode used for temperature.
		E_{HEX}	D_{HEX}	Program EEPROM bits [102:100] Diag_cfg [††]. Least significant 3 bits used.
40_{HEX}	00_{HEX}	Start_NOM => Ends Command Mode; transition to Normal Operation Mode.		
40_{HEX}	10_{HEX}	Start_RM = Start the Raw Mode (RM). In this mode, if Gain_B = 800_{HEX} and Gain_T = 80_{HEX}, then the digital output will simply be the raw values of the ADC for the Bridge reading and the PTAT conversion.		
50_{HEX}	90_{HEX}	Start_CM => Start the Command Mode; used to enter the command interpreting mode.		

[§] For more details, refer to section 3.8.
[**] For more details, refer to section 3.6.
[††] For more details, refer to section 3.6.

Command Byte	Data	Description
60_{HEX}	YY_{HEX}	Program SOT (Second Order Term).
70_{HEX}	YY_{HEX}	Program T_{SETL}. (Set the MSB to 0.)
80_{HEX}	YY_{HEX}	Program Gain_B upper 7-bits. (Set the MSB to 0.)
90_{HEX}	YY_{HEX}	Program Gain_B lower 8-bits.
$A0_{HEX}$	YY_{HEX}	Program Offset_B upper 6-bits. (Set the two MSBs to 0.)
$B0_{HEX}$	YY_{HEX}	Program Offset_B lower 8-bits.
$C0_{HEX}$	YY_{HEX}	Program Gain_T.
$D0_{HEX}$	YY_{HEX}	Program Offset_T.
$E0_{HEX}$	YY_{HEX}	Program Tco.
$E8_{HEX}$	YY_{HEX}	Disable EEPROM lock until next reset.
$F0_{HEX}$	YY_{HEX}	Program Tcg.
08_{HEX}	YY_{HEX}	Program Upper Clipping Limit. (Set the MSB to 0.)
18_{HEX}	YY_{HEX}	Program Lower Clipping Limit. (Set the MSB to 0.)
28_{HEX}	YY_{HEX}	Program Cust_ID0.
38_{HEX}	YY_{HEX}	Program Cust_ID1.
48_{HEX}	YY_{HEX}	Program Cust_ID2.

3.5. Calibration Sequence

Although the ZSSC3015 can work with many different types of resistive bridges, assume a pressure bridge is being used for the following discussion on calibration.

For this pressure sensing application, calibration essentially involves collecting raw bridge and temperature data from the ZSSC3015 for different known pressures and temperatures. This raw data can then be processed by the calibration master (typically a PC) to compute the coefficients, and the calculated coefficients can then be written to the ZSSC3015.

IDT can provide software and hardware with samples to perform the calibration.

There are three main steps to calibration:

1. Assigning a unique identification to the ZSSC3015. This identification is programmed in EEPROM and can be used as an index into the database stored on the calibration PC. This database will contain all the raw values of bridge readings and temperature readings for that part, as well as the known pressure (for this application) and temperature the bridge was exposed to. This unique identification can be stored in a concatenation of the following EEPROM registers: Cust_ID0, Cust_ID1, Cust_ID2. These registers can also form a permanent serial number.
2. Data collection. Data collection involves getting raw data from the bridge at different known pressures and temperatures. This data is then stored on the calibration PC using the unique identification of the ZSSC3015 as the index to the database.
3. Coefficient calculation and write. After enough data points have been collected to calculate all the desired coefficients then the coefficients can be calculated by the calibrating PC and written to the ZSSC3015.

Step 1 – Assigning Unique Identification

Assigning a unique identification number is as simple as using the commands Program Cust_ID0, Program Cust_ID1 and Program Cust_ID2. These three 8-bit registers allow for more than 16 million unique devices.

Step 2 – Data Collection

The number of unique (pressure, temperature) points that calibration must be performed at depends on the user's needs. The minimum is a 2-point calibration, and the maximum is a 5-point calibration. To acquire raw data from the part, set the ZSSC3015 to enter Raw Mode. This is done by issuing a Start_CM (Start Command Mode 5090_{HEX}) command/data pair to the ZSSC3015 followed by a Start_RM (Start Raw Mode 4010_{HEX}) command/data pair. Now if the Gain_B term has been set to unity (800_{HEX}) and the Gain_T term has been set to unity (80_{HEX}), then the part will be in the Raw Mode and will output raw data on its Sig™ pin instead of corrected bridge and temperature. Capture several of these data points with the user's calibration system (capturing 16 each of bridge and temperature raw measurements is recommended) and average them. For highest accuracy, start gathering calibration data after the first special measurement has been completed. Store these raw bridge and temperature settings in the database along with the known pressure and temperature. The output format during Raw Mode is Bridge_High, Bridge_Low, Temp. Each of these is an 8-bit quantity. The upper 2-bits of Bridge_High are zero-filled. The Temp data (8 bits only) would not be enough information for accurate temperature calibration. Therefore the upper three bits of temperature information are not given, but rather assumed known. Therefore effectively 11-bits of temperature information are provided in this mode.

Step 3 – Coefficient Calculations

The math to perform the coefficient calculation is very complicated and will not be discussed in detail. There is a rough overview in the "Calibration Math" section. IDT will provide software to perform the coefficient calculation. After the coefficients are calculated, the final step is to write them to the EEPROM of the ZSSC3015.

The number of calibration points required can be as few as two or as many as five. This depends on the precision desired and the behavior of the resistive bridge in use.

1. 2-point calibration can be used if only a gain and offset term are needed for a bridge with no temperature compensation for either term.
2. 3-point calibration would be used to obtain 1st order compensation for either a Tco or Tcg term but not both.
3. 3-point calibration could also be used to obtain 2nd order correction for the bridge but no temperature compensation of the bridge output.
4. 4-point calibration would be used to obtain 1st order compensation for both Tco and Tcg.
5. 4-point calibration could also be used to obtain 1st order compensation for Tco and a 2nd order correction for the bridge measurement.
6. 5-point calibration would be used to obtain both 1st order Tco correction and 1st order Tcg correction, plus a 2nd order correction that could be applied to one and only one of the following: 2nd order Tco, 2nd order Tcg, or 2nd order bridge.

3.6. EEPROM Bits

Table 3.6 shows the bit order and default settings for the EEPROM, which are programmed through the serial interface. See section 5 for important information for die/wafer customers.

Table 3.6 ZSSC3015 EEPROM Bits

EEPROM Range	Description	Default Settings	Notes
2:0	ZMDI_cfg	0_{HEX}	ZMDI_cfg[0] = Oscillator Frequency – Program to 0. ZMDI_cfg[1] = Offset_B_sign. Flip the sign of the Offset_B coefficient to be negative. ZMDI_cfg[2] = Fast_Startup. Change the command window to be 3.5ms instead of 10ms.
6:3	1V_Trim/JFET_Trim	$ssss_{BIN}$ where “s” is the part-specific factory bit setting for the reference voltage trim value. (Back-up copies are stored in CUST_ID0 for applications requiring accurate references. See section 5 for important notes.)	See Table 2.1 in section 2.4.3.
10:7	A2D_Offset	3_{HEX} (Normal polarity, positive gain; ADC offset = [-1/2,1/2])	The upper two bits are flip polarity and invert bridge input (negative gain) respectively. If both are used in conjunction, negative offset modes can be achieved. 00_{BIN} => Normal polarity, positive gain 01_{BIN} => Normal polarity, negative gain 10_{BIN} => Flip polarity, positive gain 11_{BIN} => Flip polarity, negative gain The lower two bits form the ADC offset selection. Offset selection: 11_{BIN} => [-1/2,1/2] mode bridge inputs 10_{BIN} => [-1/4,3/4] mode bridge inputs 01_{BIN} => [-1/8,7/8] mode bridge inputs 00_{BIN} => [-1/16,15/16] mode bridge inputs

EEPROM Range	Description	Default Settings	Notes
12:11	Output_Select	2_{HEX} (Rail-to-Rail Ratiometric Output Mode)	00_{BIN} => Digital (3 bytes with parity) Bridge High {00,[5:0]} Bridge Low [7:0] Temp [7:0] 01_{BIN} => 0-1V Analog 10_{BIN} => Rail-to-Rail Ratiometric 11_{BIN} => Digital (2 bytes with parity) (No Temp) Bridge High {00,[5:0]} Bridge Low [7:0]
14:13	Update_Rate	2_{HEX} (20ms (50Hz))	00_{BIN} => 1ms (1kHz) 01_{BIN} => 4ms (250Hz) 10_{BIN} => 20ms (50Hz) 11_{BIN} => 100ms (10Hz)
16:15	JFET_cfg	3_{HEX} (Over-voltage protection)	00_{BIN} => No JFET regulation (lower power) 01_{BIN} => No JFET regulation (lower power) 10_{BIN} => JFET regulation centered around 5.0V 11_{BIN} => JFET regulation centered around 5.5V (i.e., over-voltage protection)
31:17	Gain_B	800_{HEX}	Bridge Gain (also see bits 10:7): Gain_B[14] => multiply x 8 Gain_B[13:0] => 14-bit unsigned number representing a number in the range [0,8)
45:32	Offset_B	0_{HEX}	Unsigned 14-bit offset for bridge correction.
53:46	Gain_T	80_{HEX}	Temperature gain coefficient used to correct PTAT or ExtTemp reading.
61:54	Offset_T	0_{HEX}	Temperature offset coefficient used to correct PTAT or ExtTemp reading.
68:62	T_{SETL}	0_{HEX}	Stores Raw PTAT or ExtTemp reading at temperature in which low calibration points were taken.
76:69	Tcg	0_{HEX}	Coefficient for temperature correction of bridge gain term: Tcg = 8-bit magnitude of Tcg term. Sign is determined by Tc_cfg (bits 87:85).
84:77	Tco	0_{HEX}	Coefficient for temperature correction of bridge offset term. Tco = 8-bit magnitude of Tco term. Sign and scaling are determined by Tc_cfg (bits 87:85).
87:85	Tc_cfg	0_{HEX}	This 3-bit term determines options for temperature compensation of the bridge. Tc_cfg[2] => If set, Tcg is negative Tc_cfg[1] => Scale magnitude of Tco term by 8, and if SOT applies to Tco, scale SOT by 8 Tc_cfg[0] => If set, Tco is negative

EEPROM Range	Description	Default Settings	Notes
95:88	SOT	0_{HEX}	2^{nd} Order Term. This term is a 7-bit magnitude with sign. SOT[7] = 1 ➔ negative SOT[7] = 0 ➔ positive SOT[6:0] = magnitude [0-127] This term can apply to a 2^{nd} order Tcg, Tco, or bridge correction. (See SOT_cfg below.)
99:96	{SOT_cfg, Pamp_Gain}	5_{HEX} (SOT applies to Tcg; Pre-Amp Gain = 24)	Bits [99:98] = SOT_cfg 00_{BIN} = SOT applies to Bridge 01_{BIN} = SOT applies to Tcg 10_{BIN} = SOT applies to Tco 11_{BIN} = Prohibited Bits [97:96] = Pre-Amp Gain 00_{BIN} => 6 01_{BIN} => 24 (default setting) 10_{BIN} => 48 11_{BIN} => 96
102:100	Diag_cfg	7_{HEX} (Output short circuit protection, sensor short checking, and sensor connection checking enabled)	This 3-bit term applies to diagnostic features: Diag_cfg[2] → Enable output short circuit protection Diag _cfg[1] → Enable sensor short checking Diag_cfg[0] → Enable sensor connection checking
105:103	Lock_ExtTemp	0_{HEX} (Unlocked; internal PTAT used for temperature)	EEPROM lock: 011_{BIN} or 110_{BIN} => locked All other => unlocked **Important:** When EEPROM is locked, the internal charge pump is disabled and the EEPROM cannot be programmed. Bit 105 (the MSB of this field) is also used for selecting external temperature measurement. 000,001,010,011=>Internal PTAT used for temp 100,101,110,111=>External diode used for temp
112:106	Up_Clip_Lim	$7F_{HEX}$	7-bit value used to select an upper clipping limit for the output. It affects both analog and digital output. The 14-bit upper clipping limit value is {11,Up_Clip_Lim[6:0],11111}. 127 different clipping levels are selectable between 75.19% and 100% of VDD.
119:113	Low_Clip_Lim	0_{HEX}	7-bit value used to select a lower clipping limit for the output. It affects both analog and digital output. The 14-bit lower clipping limit value is {00,Low_Clip_Lim[6:0],00000}. 127 different clipping levels are selectable between 0% and 24.8% of VDD.

EEPROM Range	Description	Default Settings	Notes
127:120	Cust_ID0	SS_{HEX} where “s” is a part-specific factory bit setting. During factory testing, two back-up copies of the optimal setting for the 1V_Trim/JFET_Trim bits are stored in [123:120] and in [127:124]. See important notes in section 5.	Customer ID byte 0. Can be used to store a customer part identification number. Caution: If the application requires accurate voltage references, do not overwrite this byte until completing the procedures in section 5.
135:128	Cust_ID1	0	Customer ID byte 1. Can be used to store a customer part identification number.
143:136	Cust_ID2	0	Customer ID byte 2. Can be used to store a customer part identification number.
151:144	Signature		8-bit EEPROM signature. Generated through a LFSR[‡‡]. This signature is checked on power-on to ensure integrity of EEPROM contents.

3.7. Calibration Math

3.7.1. Correction Coefficients

All terms are calculated external to the ZSSC3015 and then programmed to its EEPROM through the serial interface.

Table 3.7 Correction Coefficients

Coefficient	Description
Offset_B_sign	A sign bit to allow for positive and negative Offset_B terms.
Gain_B	Gain term used to compensate span of Bridge reading.
Offset_B	Offset term used to compensate offset of Bridge reading.
Gain_T	Gain term used to compensate span of Temp reading.
Offset_T	Offset term used to compensate offset of Temp reading.

[‡‡] Linear feedback shift register.

Coefficient	Description
SOT	Second Order Term. The SOT can be applied as a second-order correction term for one of the following: • Bridge measurement • Temperature coefficient of offset (Tco) • Temperature coefficient of gain (Tcg) The EEPROM bits 99:98 determine which term SOT corrects.
T_{SETL}	RAW_PTAT or ExtTemp reading (upper 7-bits) at low temperature at which calibration was performed (typically room temperature).
Tcg	Temperature correction coefficient of bridge gain term. **Note:** This term has an 8-bit magnitude and a sign bit (Tc_cfg[2]).
Tco	Temperature correction coefficient of bridge offset term. **Note:** This term has an 8-bit magnitude, a sign bit (Tc_cfg[0]), and a scaling bit (Tc_cfg[1]), which can multiply its magnitude by 8.

3.7.2. Interpretation of Binary Numbers for Correction Coefficients

BR_Raw should be interpreted as an unsigned number in the set [0, 16383] with a resolution of 1.

T_Raw should be interpreted as an unsigned number in the set [0, 16383], with a resolution of 4.

3.7.2.1. Gain_B Interpretation

Gain_B should be interpreted as a value in the set [0, 64]. The MSB (bit 14) is a scaling bit that will multiply the effect of the Gain_B[13:0] term by 8. The remaining bits Gain_B[13:0] represent a number in the range of [0,8) with Gain_B[13] having a weighting of 4, and each subsequent bit has a weighting of ½ the previous bit.

Table 3.8 Gain_B [13:0] Weightings

Bit Position	Weighting
13	$2^2 = 4$
12	$2^1 = 2$
11	$2^0 = 1$
10	2^{-1}
…	…
3	2^{-8}
2	2^{-9}
1	2^{-10}
0	2^{-11}

Examples:

The binary number: 010010100110001_{BIN} = 4.6489; Gain_B[14] is 0, so the number represented by Gain_B[13:0] is not multiplied by 8.

The binary number: 101100010010110_{BIN} = 24.586; Gain_B[14] is 1, so the number represented by Gain_B[13:0] is multiplied by 8.

3.7.2.2. Offset_B Interpretation

Offset_B is a 14-bit unsigned binary number, the Offset_B_sign bit is pre-pended to the number to create a 15-bit 2's complement signed value. The bit weightings of {Offset_B_sign, Offset_B[13:0]} are shown in Table 3.9.

Table 3.9 Offset_B Weightings

Bit Position	Weighting
Offset_B_sign	-16384
13	8192
12	4096
11	2048
.	
.	
.	
1	$2^1 = 2$
0	$2^0 = 1$

For example, the binary number 0 1111 1111 1100_{BIN} = 4092.
However, with the Offset_B_sign bit set, the binary number 1 1111 1111 1100_{BIN} = -4.

3.7.2.3. Gain_T Interpretation

Gain_T should be interpreted as a number in the set [0,2]. Gain_T[7] has a weighting of 1, and each subsequent bit has a weighting of ½ the previous bit.

Table 3.10 Gain_T Weightings

Bit Position	Weighting
7	$2^0 = 1$
6	$2^{-1} = 0.5$
5	$2^{-2} = 0.25$
4	2^{-3}
3	2^{-4}
2	2^{-5}
1	2^{-6}
0	2^{-7}

3.7.2.4. Offset_T Interpretation

Offset_T is an 8-bit signed binary number in two's complement form. The MSB has a weighting of -128. The following bits then have a weighting of 64, 32, 16 …

Table 3.11 Offset_T Weightings

Bit Position	Weighting
7	-128
6	$2^6 = 64$
5	$2^5 = 32$
4	$2^4 = 16$
3	$2^3 = 8$
2	$2^2 = 4$
1	$2^1 = 2$
0	$2^0 = 1$

For example, the binary number $00101001_{BIN} = 41_{DEC}$.

3.7.2.5. Tco Interpretation

Tco is specified as having an 8-bit magnitude with an additional sign bit and a scalar bit (Tc_cfg). When the scalar bit is set, the signed Tco is multiplied by 8.

- Tco Resolution: 0.175 µV/V/^{o}C (referenced to input)
- Tco Range: ± 44.6 µV/V/^{o}C (referenced to input)

If the scaling bit is used, then the above resolution and range are scaled by 8 to give the following results:

- Tco Scaled Resolution: 1.40 µV/V/^{o}C (referenced to input)
- Tco Scaled Range: ± 357 µV/V/^{o}C (referenced to input)

3.7.2.6. Tcg Interpretation

Tcg is specified as an 8-bit magnitude with an additional sign bit (Tc_cfg).

- Tcg Resolution: 17.0 ppm/^{o}C
- Tcg Range: ±4335 ppm/^{o}C

3.7.2.7. SOT Interpretation

SOT is a 2nd order term that can apply to one and only one of the following: bridge nonlinearity correction, Tco nonlinearity correction, or Tcg nonlinearity correction.

As it applies to bridge nonlinearity correction:

- Resolution: 0.25% @ Full Scale
- Range: +25% @ Full Scale to -25% @ Full Scale
  (Saturation in internal arithmetic will occur at greater negative nonlinearities.)

As it applies to Tcg:

- Resolution: 0.3 ppm/(^oC)^2
- Range: +/- 38ppm/(^oC)^2

As it applies to Tco:

2 settings are possible. It is possible to scale the effect of SOT by 8. If Tc_cfg[1] is set, then both Tco and SOT's contribution to Tco are multiplied by 8.

- Resolution at unity scaling: 1.51nV/V/(^oC)^2 (referenced to input)
- Range: +/- 0.192µV/V/(^oC)^2 (referenced to input)
- Resolution at 8x scaling: 12.1nV/V/(oC)2 (referenced to input)
- Range: +/- 1.54µV/V/(oC)^2 (referenced to input)

3.8. Reading EEPROM Contents

The contents of the entire EEPROM memory can be read out using the Read EEPROM command (00_{HEX}). This command causes the ZSSC3015 to output consecutive bytes on the ZACwire™ interface. After each transmission, the EEPROM contents are shifted by 8 bits. The bit order of these bytes is given in Table 3.12.

Table 3.12 EEPROM Read Order

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1	Offset_B[7:0]							
Byte 2	Gain_T[1:0]		Offset_B[13:8]					
Byte 3	Offset_T[1:0]		Gain_T[7:2]					
Byte 4	T_{SETL}[1:0]		Offset_T[7:2]					
Byte 5	Tcg[2:0]			T_{SETL}[6:2]				
Byte 6	Tco[2:0]			Tcg[7:3]				
Byte 7	Tc_cfg[2:0]			Tco[7:3]				
Byte 8	SOT[7:0]							
Byte 9	Lock[0]	Diag_cfg[2:0]			SOT_cfg/Pamp_Gain[3:0]			
Byte 10	Up_Clip_Lim[5:0]						Lock[2:1]	
Byte 11	Low_Clip_Lim[6:0]							Up_Clip_Lim[6]
Byte 12	Cust_ID0[7:0]							
Byte 13	Cust_ID1[7:0]							
Byte 14	Cust_ID2[7:0]							
Byte 15	Signature[7:0]							
Byte 16	A2D_Offset[0]	1V_Trim/JFET_Trim[3:0]				ZMDI_cfg[2:0]		
Byte 17	JFET_cfg[0]	Update_Rate[1:0]		Output Select[1:0]		A2D_Offset[3:1]		
Byte 18	Gain_B[6:0]							JFET_cfg[1]
Byte 19	Gain_B[14:7]							
Byte 20	$A5_{HEX}$							

4 Application Circuit Examples

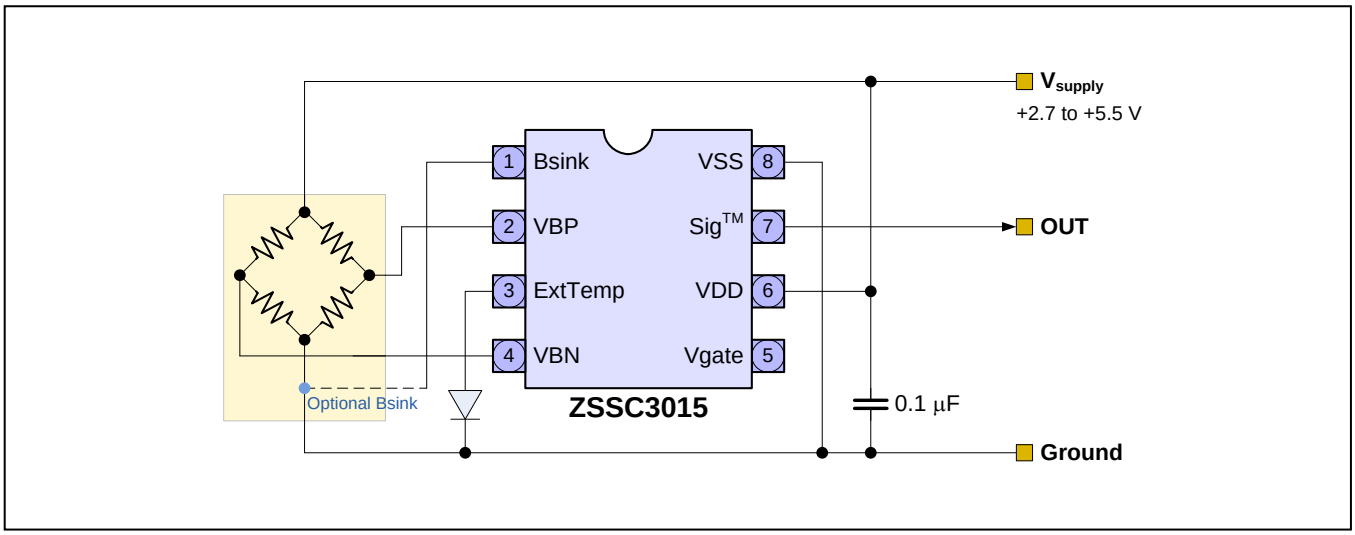
The minimum output analog load resistor is R_L= 5kΩ. This optional load resistor can be configured as a pull-up or pull-down. If it is configured as a pull-down, it cannot be part of the module to be calibrated because this would prevent proper operation of the ZACwire™. If a pull-down load is desired, it must be added to system after module calibration.

There is no output load capacitance needed.

4.1. Three-Wire Rail-to-Rail Ratiometric Output

This example shows an application circuit for rail-to-rail ratiometric voltage output configuration with temperature compensation via an external diode.

Figure 4.1 Rail-to-Rail Ratiometric Voltage Output – Temperature Compensation via External Diode



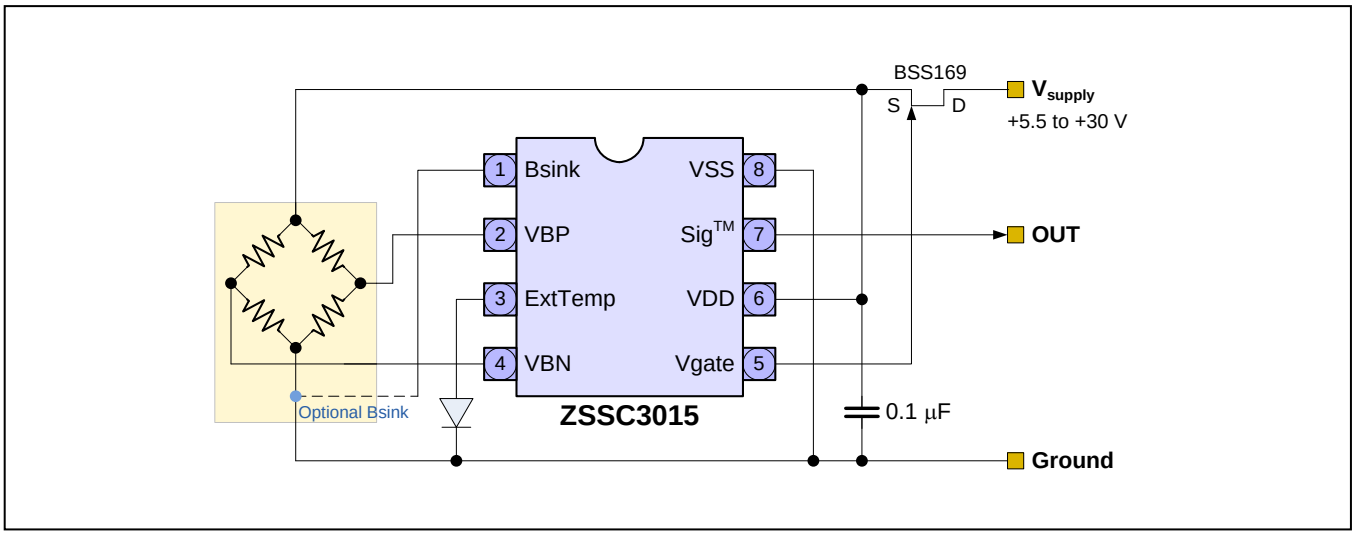
The optional bridge sink allows a power savings of bridge current. The output voltage can be either

- Rail-to-rail ratiometric analog output (ratiometric to VDD = Vsupply).
- 0 to 1V analog output. The absolute voltage output reference is trimmable 1V (+/-2mV) in the 1V Output Mode via a 4-bit EEPROM field. See section 2.4.3.

4.2. Absolute Analog Voltage Output

The figure below shows an application circuit for an absolute voltage output configuration with temperature compensation via external diode and external JFET regulation for all industry standard applications.

Figure 4.2 Absolute Analog Voltage Output – Temperature Compensation via External Diode with External JFET Regulation



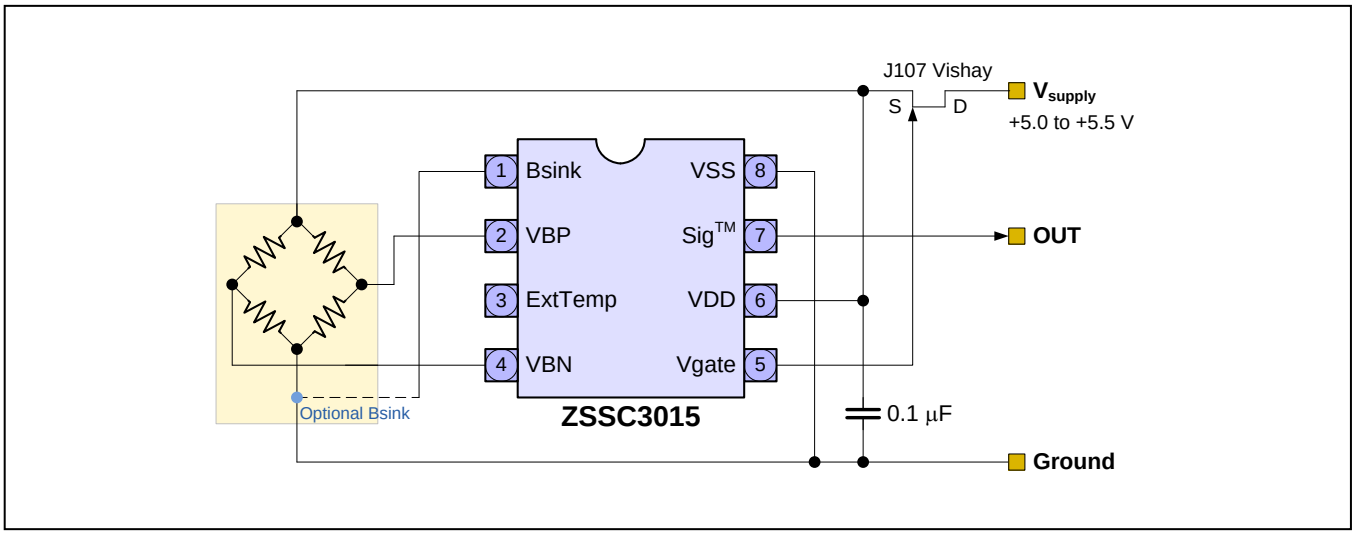
The output signal range can be one of the following options:

- 0 to 1 V analog output. The absolute voltage output reference is trimmable: 1V (+/-2 mV) in the 1V Output Mode via a 4-bit EEPROM field (see section 2.4.3).
- Rail-to-rail analog output. The on-chip reference for the JFET regulator block is trimmable: 5 V (±~10 mV) in the Ratiometric Output Mode via a 4-bit EEPROM field. (See section 2.4.3).

4.3. Three-Wire Ratiometric Output with Over-Voltage Protection

The figure below shows an application circuit for a ratiometric output configuration with temperature compensation via the internal PTAT. In this application, the JFET is used for voltage protection. JFET_cfg (16:15) in the EEPROM is configured to 5.5V. There is an additional maximum error of 8mV caused by the non-zero r_{ON} of the limiter JFET.

Figure 4.3 Ratiometric Output, Temperature Compensation via Internal PTAT



4.4. Digital Output

For all three circuits, the output signal can also be digital. Depending on the output select bits, the bridge signal or the bridge signal and temperature signal are sent. For the digital output, no load resistor or load capacity is necessary. No pull-down resistor is allowed. If a line resistor or pull-up resistor is used, the requirement for the rise time must be met (< 5µs). The ZSSC3015 output includes an internal pull-up resistor of about 30kΩ. The digital output can easily be read by firmware from a microcontroller, and IDT can provide the customer with software for developing the interface.

4.5. Output Resistor/Capacitor Limits

The limits for external components depend on the programmed output mode:

- Pure Analog Output Mode (calibration is done before): The only limit is the minimum load resistance of 5kΩ.
- Pure Digital Output Mode with end-of-line calibration: The RC time constant of the ZACwire™ line must have a rise time ≤ 5µs.
- Analog output with digital communication during calibration: The RC time constant of the ZACwire™ line must have a rise time ≤ 5µs.

Warning: Any series line resistance forms a voltage divider in conjunction with the pull-up load device. If a series line resistance is needed, choose a low value relative to the pull-up load device.

5 EEPROM Restoration

If needed, the default settings for the ZSSC3015 (see Table 3.6) can be reprogrammed as described in section 3. The following sections describe EEPROM content validation and handling during and/or after system assembly.

Important: During the sawing and dicing process, there is a possibility of the EEPROM contents flipping, and prevention cannot be guaranteed. This is primarily a concern for the factory trim settings, which are customized to each part. **If purchasing packaged parts, the EEPROM contents have already been returned to their default values and this section can be ignored.**

The EEPROM default values programmed during the different test levels have been selected so that customer has the option to refresh/reprogram trim bits that might have flipped during sawing or dicing.

Important: The EEPROM lock is stored in the bit range 105:103. A value of 6_{HEX} or 3_{HEX} will lock the EEPROM, disabling the charge pump needed for EEPROM writing. The lock may be temporarily ignored by using the EEPROM Force Unlock command ($E800_{HEX}$) in Command Mode. This will re-enable the charge pump until the next reset. Alternatively, the EEPROM Force Unlock command could be issued in Command Mode and the lock itself may be reprogrammed in EEPROM at this time. The complete contents can also be validated using the EEPROM signature stored in bits [151:144], (see “Signature” in Table 3.6).

5.1. Default EEPROM Contents

During the wafer level test (wafer/dice delivery) and during final test for SOP8 packaged parts, the EEPROM is programmed with the default values listed in the Table 3.6.

During the wafer level test, the trim bits in 1V_Trim/JFET_Trim [6:3] are set to die-specific values.

5.1.1. 1V_Trim/JFET_Trim

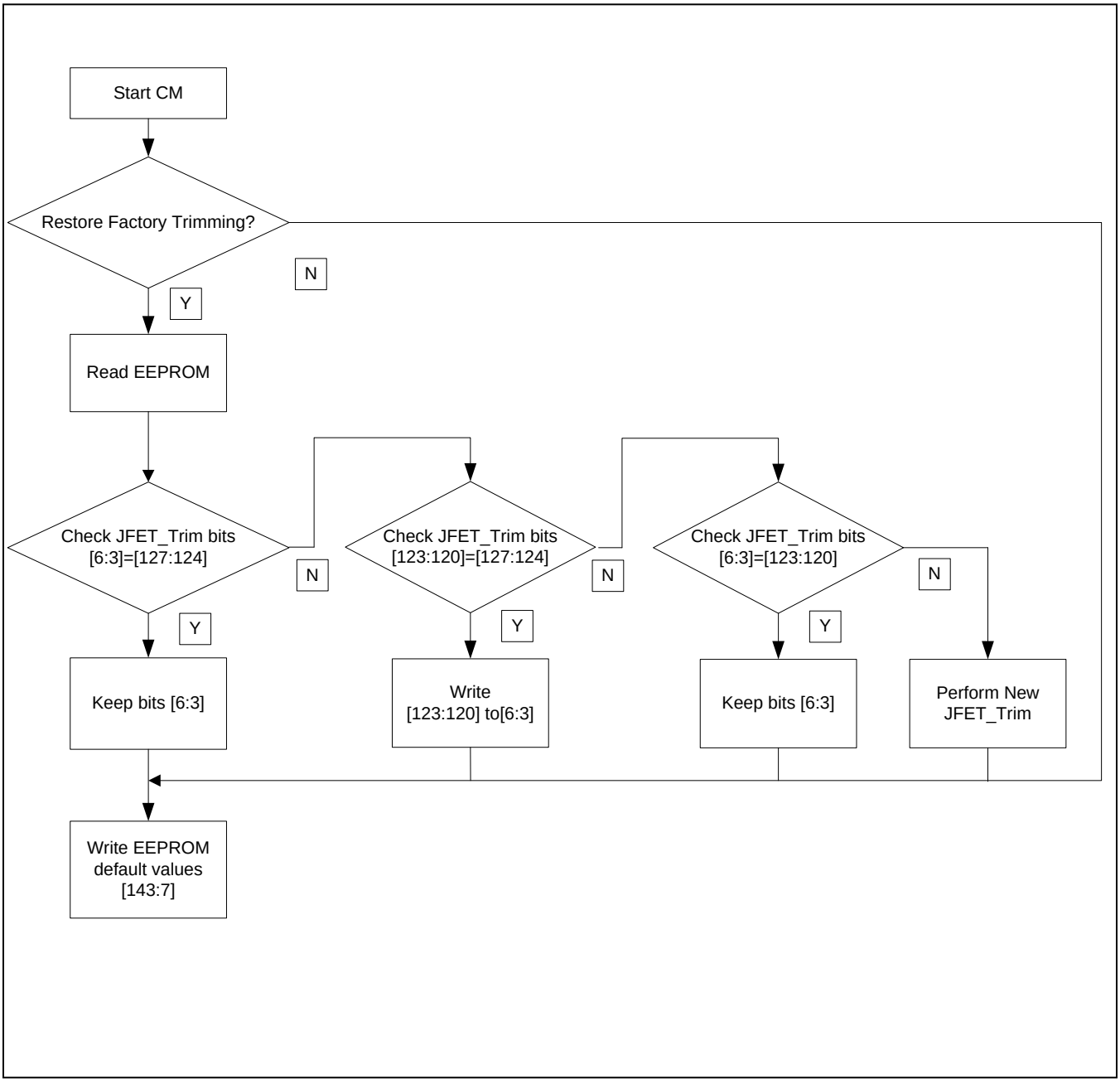
The 5V reference for the JFET regulation is factory trimmed during the final test to 5V±15mV using the 1V_Trim/JFET_Trim bit setting. The 4-bit setting stored in EEPROM bits [6:3] is copied twice to the Cust_ID0 bits [127:124] and [123:120] to ensure the factory settings are retained so that the customer can reprogram these values in the 1V_Trim/JFET_Trim bits if needed.

5.2. EEPROM Restoration Procedure

After module assembly, the EEPROM content should be refreshed. If JFET regulation is not used for the customer’s application, write the default values shown in Table 3.6 to the EEPROM bit range [143:7] and retain the existing values in the bit range [6:0]. If JFET regulation is required, the bit restoration procedure shown in the flow chart in Figure 5.1 must be used to keep the factory settings that were programmed during the testing.

Note: The EEPROM signature is re-calculated and updated after every EEPROM writing.

Figure 5.1 EEPROM Validation and Restoration Procedure



6 Pin Configuration and Package

The standard package of the ZSSC3015 is an SOP-8 (3.81mm / 150mil body) with a lead-pitch 1.27mm / 50mil.

Figure 6.1 ZSSC3015 Pin-Out Diagram

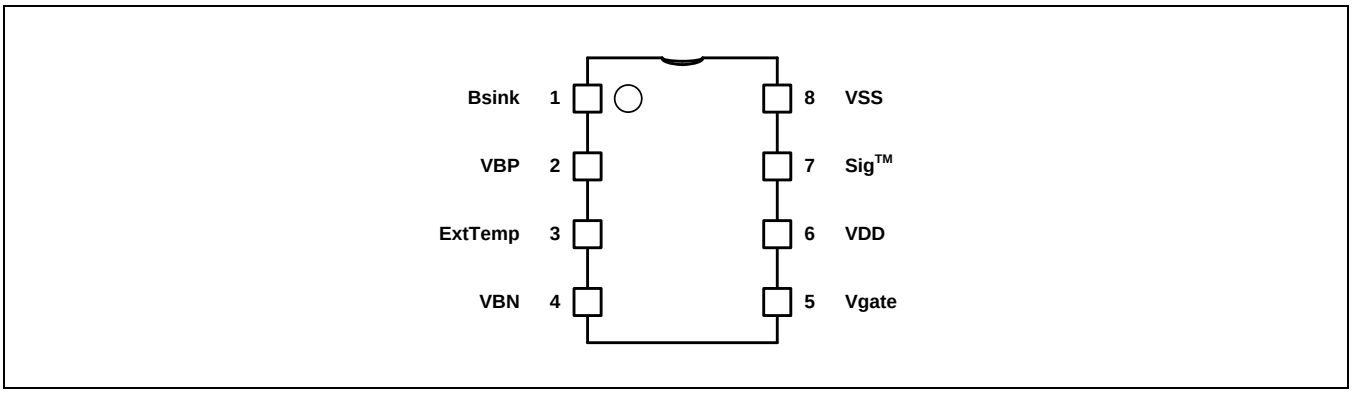


Table 6.1 ZSSC3015 Pin Configuration

Pin No.	Name	Description
1	Bsink	Optional ground connection for bridge ground. Used for power savings.
2	VBP	Positive bridge connection
3	ExtTemp	External diode connection
4	VBN	Negative bridge connection
5	Vgate	Gate control for external JFET regulation/over-voltage protection
6	VDD	Supply voltage (2.7 to 5.5 V)
7	Sig™	ZACwire™ interface (analog out, digital out, calibration interface)
8	VSS	Ground supply

7 ESD/Latch-Up-Protection

All pins have an ESD protection of ≥4000V and a latch-up protection of ±100 mA or of +8V/ –4V (to VSS/VSSA). ESD protection referenced to the Human Body Model is tested with devices in SOP-8 packages during product qualification. The ESD test follows the Human Body Model with 1.5kΩ/100pF based on MIL 883, Method 3015.7.

8 Test

The test program is based on this datasheet. The final parameters that will be tested during series production are listed in the tables of section 1.

The digital part of the ZSSC3015 includes IDDQ and a scan chain with a boundary scan, which can be activated and controlled during wafer test. Further test support for testing of the analog parts on wafer level is included in the DSP.

9 Quality and Reliability

The ZSSC3015 is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate <5fit (temp=55°C, S=60%) is guaranteed. A typical fit rate of the C7A-technology, which is used for ZSSC3015, is 2.7fit.

10 Customization

For high-volume applications that require an upgraded or downgraded functionality compared to the ZSSC3015, IDT can customize the circuit design by adding or removing certain functional blocks.

For this customization, IDT has a considerable library of sensor-dedicated circuitry blocks, which enable IDT to provide a custom solution quickly. Please contact IDT for further information.

11 Ordering Sales Codes

Sales Code	Description	Package
ZSSC3015NE1B	ZSSC3015 Die — Temperature range: -50°C to +150°C	Unsawn on Wafer
ZSSC3015NE1C	ZSSC3015 Die — Temperature range: -50°C to +150°C	Sawn on Wafer Frame
ZSSC3015NE2T(R)	ZSSC3015 SOP8 (150 mil) — Temperature range: -50°C to +150°C	Tube: add "-T" to sales code Reel: add "-R"
ZSSC3015NA1B	ZSSC3015 Die — Temperature range: -40°C to +125°C	Unsawn on Wafer
ZSSC3015NA1C	ZSSC3015 Die — Temperature range: -40°C to +125°C	Sawn on Wafer Frame
ZSSC3015NA2T(R)	ZSSC3015 SOP8 (150 mil) — Temperature range: -40°C to +125°C	Tube: add "-T" to sales code Reel: add "-R"
ZSSC3015KIT	ZSSC3015 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB cable, 5 IC samples, instructions for downloading SSC Evaluation Software from www.IDT.com	Kit

Contact IDT Sales for support and sales of IDT's ZSSC3015 Mass Calibration System.

12 Related Documents

Documents marked with two asterisks (**) require a login account for access on the web.

Documents marked with three asterisks (***) are only available on request.

Document
ZSSC3015 Feature Sheet
ZACwire™ SSC Evaluation Kit Documentation
SSC Evaluation Kits Feature Sheet (includes ordering codes)
ZSSC3015 Technical Note – IDT Wafer Dicing Guidelines
*ZSC31010, ZSC31015, and ZSSC3015 Technical Note – ZACWire™ SSC Calibration Sequence, DLL and EXE***
*ZSSC3015 Technical Note – Die Dimensions and Pad Coordinates ****
*ZSSC3015 Response Time Spreadsheet ****
*Technical Note – ZACwire™ Communication ****

Visit the ZSSC3015 product page (www.IDT.com/ZSSC3015) or contact your nearest sales office for the latest version of these documents.

13 Definitions of Acronyms

Term	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
BUF	Buffer
CM	Command Mode
CMC	Calibration Microcontroller
DAC	Digital-to-Digital Converter
DNL	Differential Nonlinearity
DSP	Digital Signal Processor
DUT	Device Under Test
ESD	Electrostatic Discharge
FSO	Full-Scale Output
INL	Integrated Nonlinearity
LSB	Least Significant Bit
MUX	Multiplexer
NOM	Normal Operation Mode
OWI	One-Wire Interface
POR	Power-On Reset Level
PSRR	Power Supply Rejection Ratio
PTAT	Proportional To Absolute Temperature
RM	Raw Mode
SOT	Second Order Term

14 Document Revision History

Revision	Date	Description
1.00	January 28, 2013	First release.
1.01-1.02	March 25, 2013	Edits for timing diagrams. Revision to block diagram. Updates for part numbers, contact information, and imagery for cover and headers. Minor edits.
1.10	May 6, 2013	Addition of specifications for EEPROM retention and cycles in section 1.3. Update for cover image.
1.11	July 3, 2014	Update to section 1.2 regarding minimum bridge resistance values. Update to section 2.6.3 regarding minimum bridge resistance values. Updates for order table, product references, “Related Documents” section, and IDT contact information.
1.12	December 26, 2014	Correction for default definition for EEPROM bits 99:96 in Table 3.6. Update for contact information.
	January 20, 2016	Changed to IDT branding.

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