

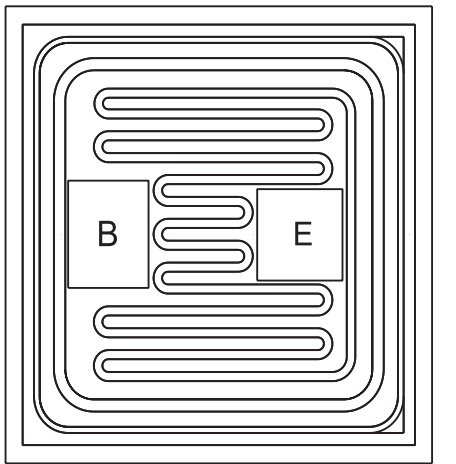
**PROCESS CP310**  
**Small Signal Transistor**  
NPN - High Voltage Transistor Chip

**Central**<sup>TM</sup>  
**Semiconductor Corp.**

**PROCESS DETAILS**

Process	EPITAXIAL PLANAR
Die Size	26 x 26 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	6.1 x 4.9 MILS
Emitter Bonding Pad Area	5.2 x 5.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

**GEOMETRY**



BACKSIDE COLLECTOR <sup>R1</sup>

**GROSS DIE PER 4 INCH WAFER**

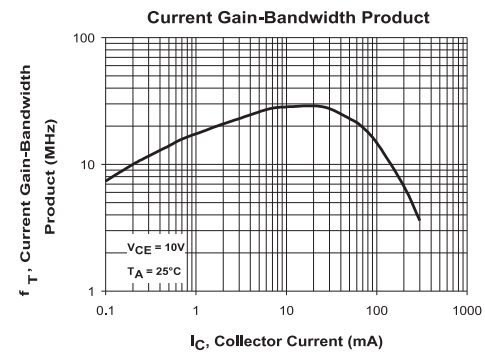
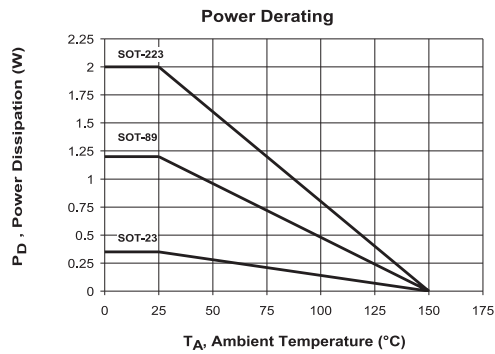
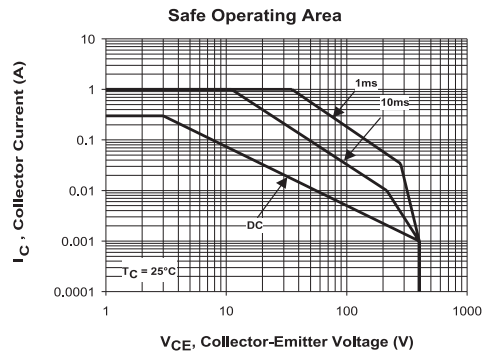
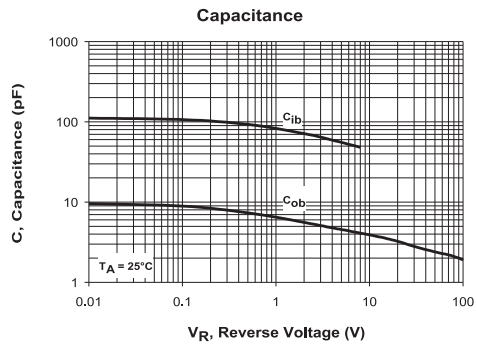
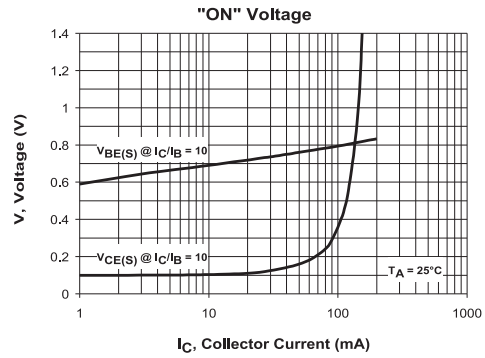
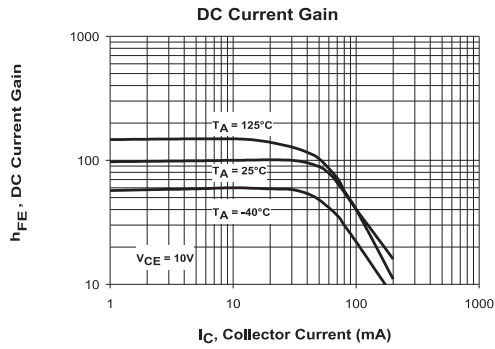
16,880

**PRINCIPAL DEVICE TYPES**

2N3439  
2N3440  
CMPTA42  
CMPTA44  
CMPT6517  
CXTA44  
CZTA42  
CZTA44  
MPSA42  
MPSA44

145 Adams Avenue  
Hauppauge, NY 11788 USA  
Tel: (631) 435-1110  
Fax: (631) 435-1824  
www.centrasemi.com

R2 (1-August 2002)



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