

ESD9L, SESD9L Series

Transient Voltage Suppressors

ESD Protection Diodes with Ultra-Low Capacitance

The ESD9L Series is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

Specification Features:

- Ultra Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
0.039" x 0.024" (1.00 mm x 0.60 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand-off Voltage: 3.3 V, 5 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000-4-2 Level 4 ESD Protection
- S and SZ Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V-0

LEAD FINISH: 100% Matte Sn (Tin)

MOUNTING POSITION: Any

QUALIFIED MAX REFLOW TEMPERATURE: 260°C

Device Meets MSL 1 Requirements

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|------------------|-------------|------|
| IEC 61000-4-2 (ESD) Contact Air | | ±10 ±15 | kV |
| Total Power Dissipation on FR-5 Board (Note 1) @ T _A = 25°C | P _D | 150 | mW |
| Storage Temperature Range | T _{stg} | -55 to +150 | °C |
| Junction Temperature Range | T _J | -55 to +150 | °C |
| Lead Solder Temperature – Maximum (10 Second Duration) | T _L | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

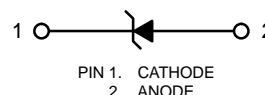
1. FR-5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.

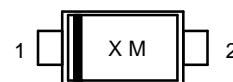


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MARKING DIAGRAM



X = Specific Device Code
M = Date Code

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|----------------------|------------------|
| ESD9LxxxST5G | SOD-923 (Pb-Free) | 8000/Tape & Reel |
| SESD9LxxxST5G | SOD-923 (Pb-Free) | 8000/Tape & Reel |
| SZESD9LxxxST5G | SOD-923 (Pb-Free) | 8000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

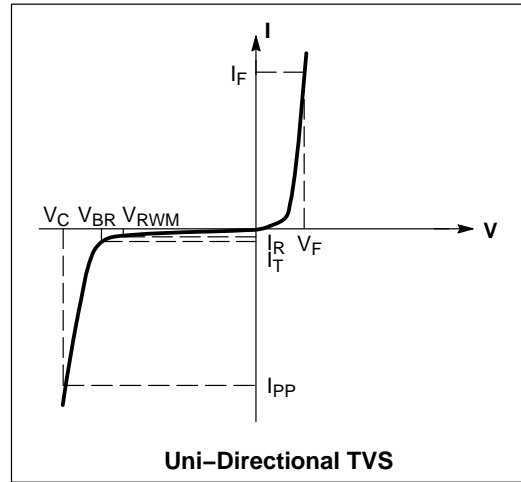
See specific marking information in the device marking column of the Electrical Characteristics tables starting on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter |
|-----------|--|
| I_{PP} | Maximum Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| V_{RWM} | Working Peak Reverse Voltage |
| I_R | Maximum Reverse Leakage Current @ V_{RWM} |
| V_{BR} | Breakdown Voltage @ I_T |
| I_T | Test Current |
| I_F | Forward Current |
| V_F | Forward Voltage @ I_F |
| P_{pk} | Peak Power Dissipation |
| C | Max. Capacitance @ $V_R = 0$ and $f = 1.0$ MHz |



*See Application Note AND8308/D for detailed explanations of datasheet parameters.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, $V_F = 1.0$ V Max. @ $I_F = 10$ mA for all types)

| Device* | Device Marking | V_{RWM} (V) | I_R (μA) @ V_{RWM} | V_{BR} (V) @ I_T (Note 2) | I_T | C (pF) | | V_C (V) @ $I_{PP} = 1$ A | V_C |
|--------------|----------------|---------------|-------------------------------------|-------------------------------|-------|--------|-----|----------------------------|------------------------------|
| | | Max | Max | Min | mA | Typ | Max | Max | Per IEC61000-4-2 (Note 4) |
| ESD9L3.3ST5G | 6** | 3.3 | 1.0 | 4.8 | 1.0 | 0.5 | 0.9 | 9.0 | Figures 1 and 2 See Below |
| ESD9L5.0ST5G | D | 5.0 | 1.0 | 5.4 | 1.0 | 0.5 | 0.9 | 9.8 | Figures 1 and 2 See Below |

* Includes S and SZ-prefix devices where applicable.

**Rotated 180°.

- V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C .
- Surge current waveform per Figure 5.
- For test procedure see Figures 3 and 4 and Application Note AND8307/D.

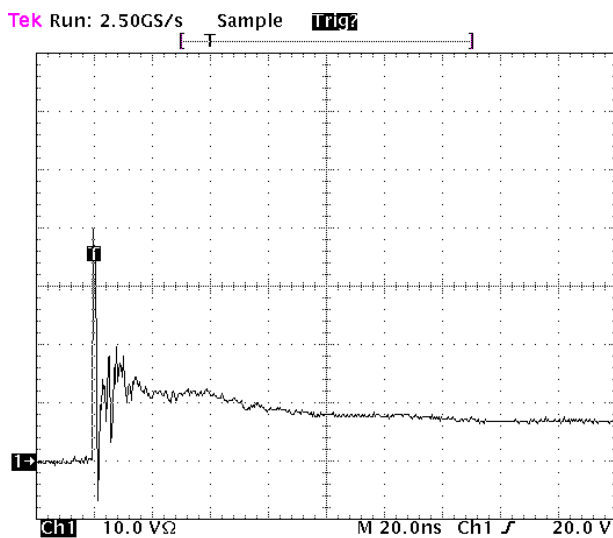


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

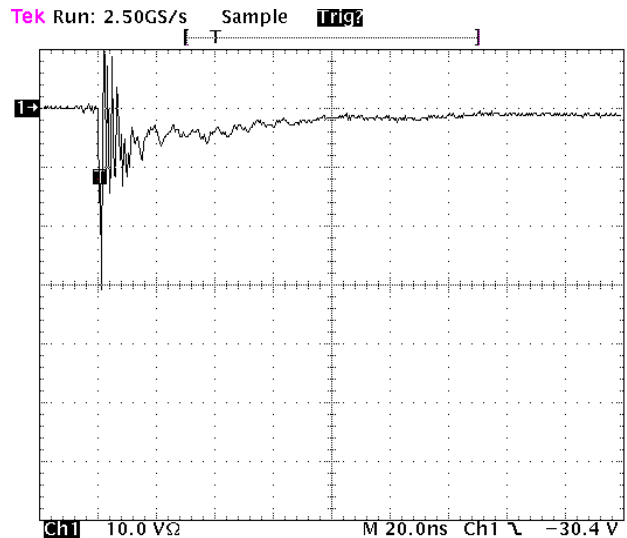


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

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IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |



Figure 3. IEC61000-4-2 Spec

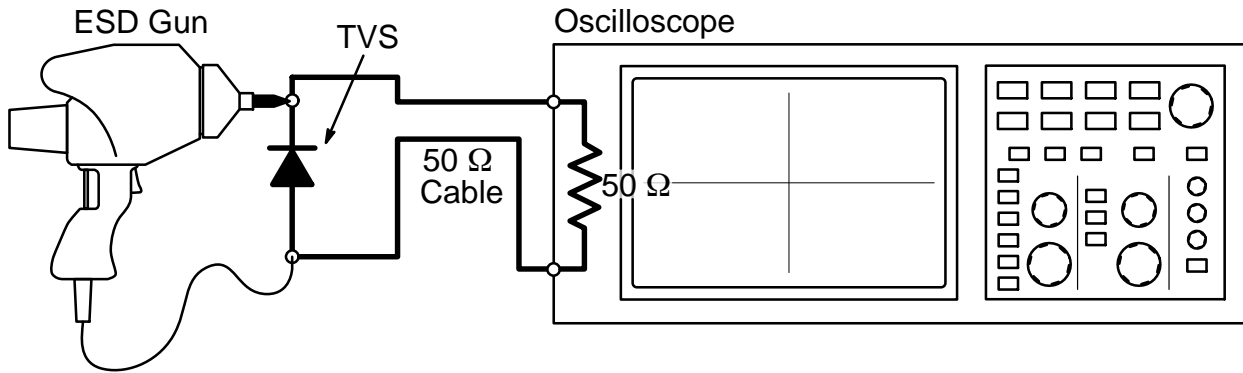


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

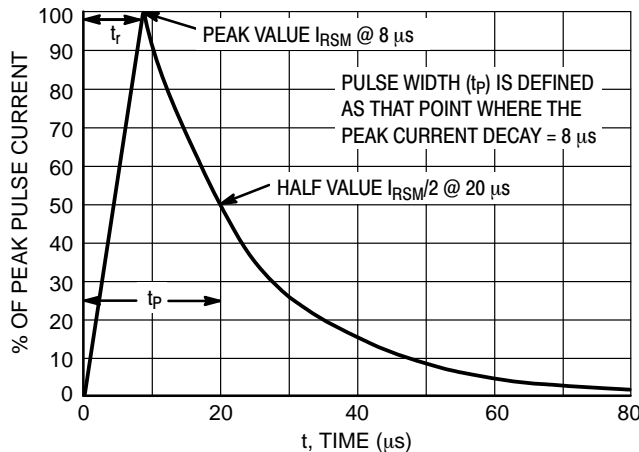
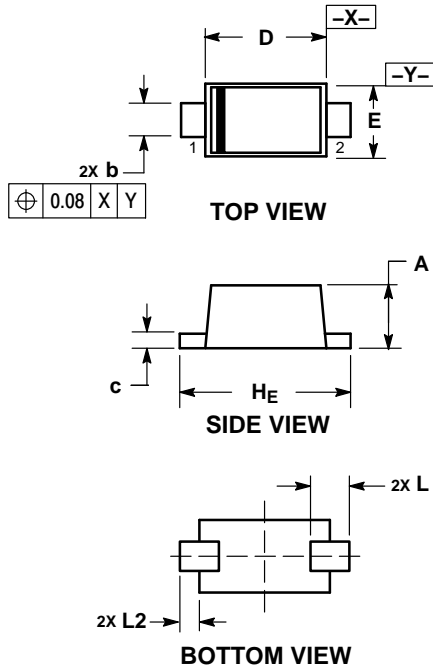


Figure 5. 8 X 20 μs Pulse Waveform

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PACKAGE DIMENSIONS

SOD-923
CASE 514AB
ISSUE C

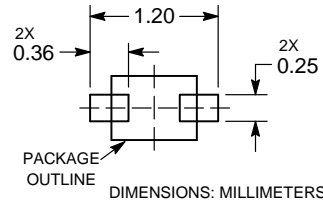


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | MILLIMETERS | | | INCHES | | |
|----------------|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.34 | 0.37 | 0.40 | 0.013 | 0.015 | 0.016 |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| c | 0.07 | 0.12 | 0.17 | 0.003 | 0.005 | 0.007 |
| D | 0.75 | 0.80 | 0.85 | 0.030 | 0.031 | 0.033 |
| E | 0.55 | 0.60 | 0.65 | 0.022 | 0.024 | 0.026 |
| H _E | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| L | 0.19 REF | | | 0.007 REF | | |
| L ₂ | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |

SOLDERING FOOTPRINT*



See Application Note AND8455/D for more mounting details

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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