

Small Signal Product

## Bi-directional ESD Protection Diode

### FEATURES

- Meet IEC61000-4-2 (ESD)  $\pm 15\text{kV}$  (air),  $\pm 8\text{kV}$  (contact)
- Meet IEC61000-4-4 (EFT) rating, 40A (5/50ns)
- Protects one Bi-directional I/O line
- Working Voltage : 5V
- Pb free version and RoHS compliant
- Packing code with suffix "G" means green compound (halogen-free)

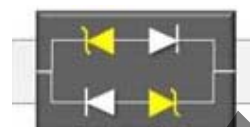


SOD-323



### MECHANICAL DATA

- Case: SOD-323 small outline plastic package
- Terminal: Matte tin plated, lead free., solderable per MIL-STD-202, Method 208 guaranteed
- High temperature soldering guaranteed :  $260^{\circ}\text{C}/10\text{s}$
- Weight:  $4.85 \pm 0.5 \text{ mg}$
- Marking code: AC



### APPLICATIONS

- Cell Phone Handsets and Accessories
- Notebooks, Desktops, and Servers
- Keypads, Side Keys, USB 2.0, LCD Displays
- Portable Instrumentation
- Microprocessor Based Equipment

### MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

| PARAMETER   | SYMBOL         | VALUE       | UNIT               |
|---|----------------|-------------|--------------------|
| Peak Pulse Power (tp=8/20 $\mu\text{s}$ waveform) | $P_{PP}$       | 350         | W                  |
| ESD per IEC 61000-4-2 (Air)                       | $V_{ESD}$      | $\pm 15$    | KV                 |
| ESD per IEC 61000-4-2 (Contact)                   |                | $\pm 8$     |                    |
| Junction and Storage Temperature Range            | $T_J, T_{STG}$ | -55 to +150 | $^{\circ}\text{C}$ |

| PARAMETER                 | SYMBOL     | MIN | MAX  | UNIT          |
|---------------------------|------------|-----|------|---------------|
| Reverse Stand-Off Voltage | $V_{RWM}$  | -   | 5    | V             |
| Reverse Breakdown Voltage | $V_{(BR)}$ | 6   | -    | V             |
| Reverse Leakage Current   | $I_R$      | -   | 5    | $\mu\text{A}$ |
| Clamping Voltage          | $V_C$      | -   | 9.8  | V             |
|                           |            | -   | 18.3 |               |
| Junction Capacitance      | $C_J$      | 1.2 |      | pF            |

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RATINGS AND CHARACTERISTICS CURVES

( $T_A=25^\circ\text{C}$  unless otherwise noted)

Fig. 1 Non-Repetitive Peak Pulse Power VS. Pulse Time

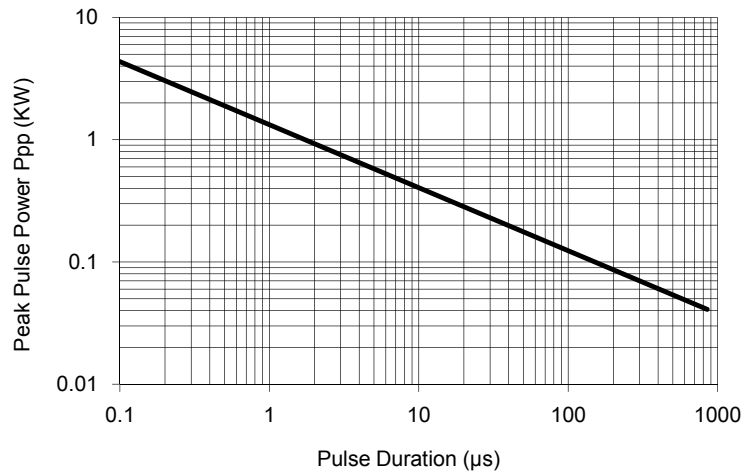


Fig. 2 Pulse Waveform

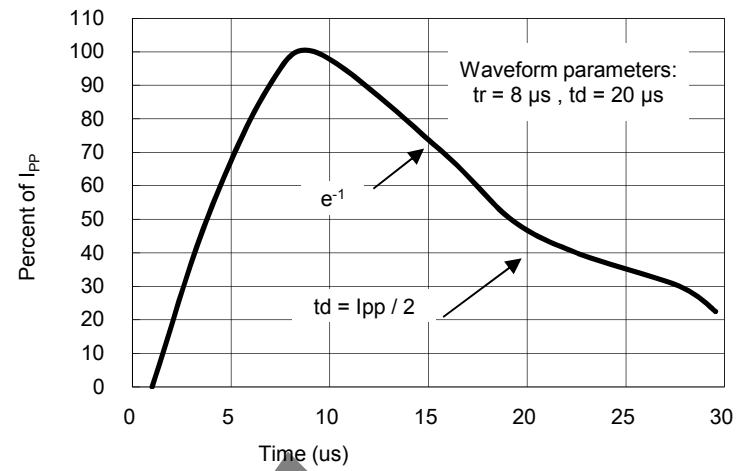


Fig. 3 Admissible Power Dissipation Curve

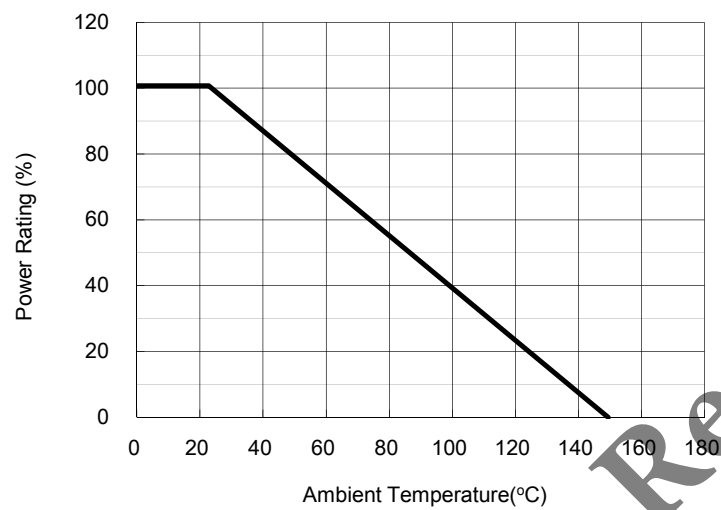


Fig. 4 Typical Junction Capacitance

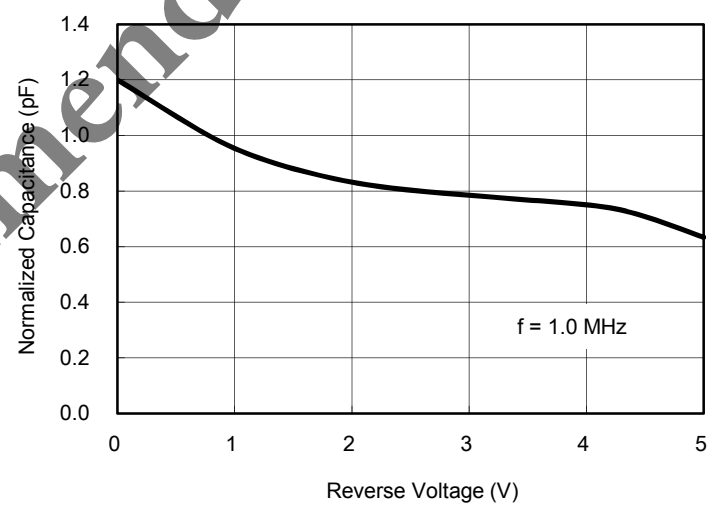
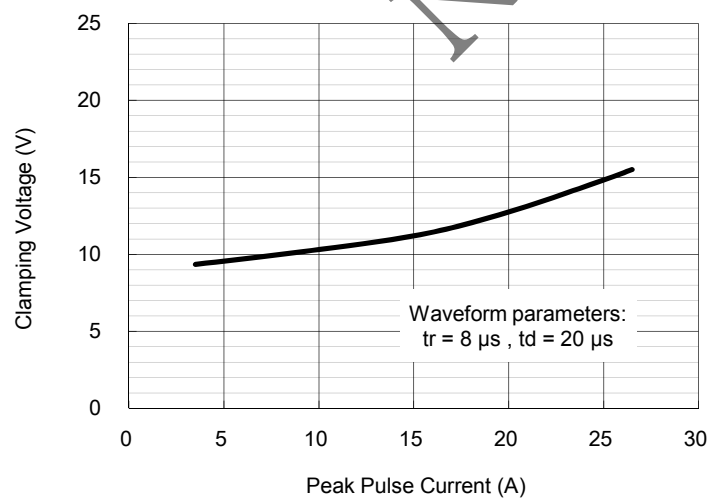


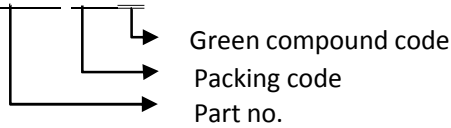
Fig. 5 Clamping Voltage VS. Peak Pulse Current



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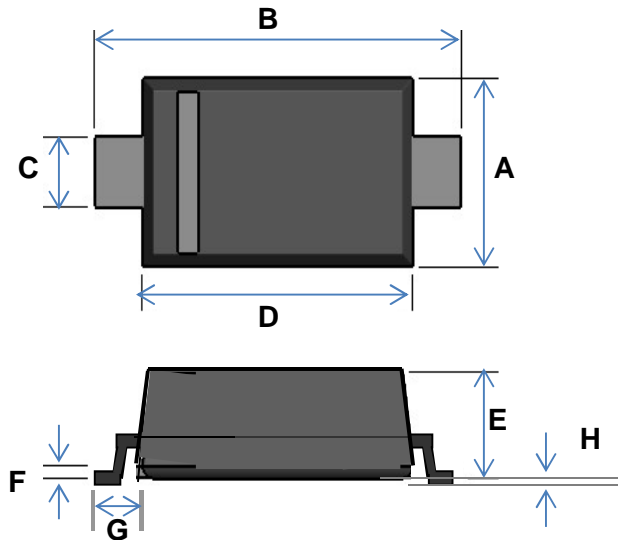
ORDER INFORMATION (EXAMPLE)

TESDC5V0LC RRG



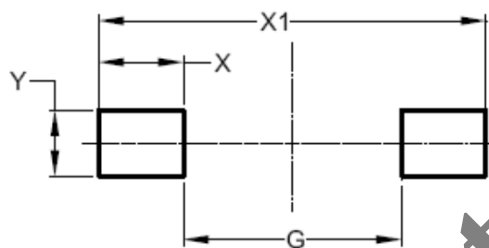
PACKAGE OUTLINE DIMENSIONS

**SOD-323**



| DIM. | Unit (mm) |       | Unit (inch) |       |
|------|-----------|-------|-------------|-------|
|      | Min       | Max   | Min         | Max   |
| A    | 1.150     | 1.400 | 0.045       | 0.055 |
| B    | 2.300     | 2.700 | 0.091       | 0.106 |
| C    | 0.250     | 0.450 | 0.010       | 0.018 |
| D    | 1.600     | 1.800 | 0.063       | 0.071 |
| E    | 0.800     | 1.000 | 0.031       | 0.039 |
| F    | 0.050     | 0.177 | 0.002       | 0.007 |
| G    | 0.475 REF |       | 0.019 REF   |       |
| H    | -         | 0.100 | -           | 0.004 |

SUGGEST PAD LAYOUT



| DIM. | Unit (mm) |     | Unit (inch) |     |
|------|-----------|-----|-------------|-----|
|      | Min       | Min | Min         | Min |
| G    | 1.52      |     | 0.060       |     |
| X    | 0.59      |     | 0.023       |     |
| X1   | 2.70      |     | 0.106       |     |
| Y    | 0.45      |     | 0.018       |     |

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

APPLICATION INFORMATION

- Designed to protect one data, I/O, or power supply line
- Designed to protect sensitive electronics from damage or latch-up due to ESD
- Designed to replace multilayer varistors (MLVs) in portable applications
- Offers superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs
- The combination of small size and high ESD surge capability makes them ideal for use in portable applications

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

- Good circuit board layout is critical for the suppression of ESD induced transients
- Place the ESD Protection Diode near the input terminals or connectors to restrict transient coupling
- Minimize the path length between the ESD Protection Diode and the protected line
- Minimize all conductive loops including power and ground loops
- The ESD transient return path to ground should be kept as short as possible

**Not Recommended**

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