# VS-VSKCS203/100

**Vishay Semiconductors** 





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AAP Gen 7 (TO-240AA)

PRIMARY CHARACTERISTICS			
I <sub>F(AV)</sub>	200 A		
V <sub>R</sub>	100 V		
Package	AAP Gen 7 (TO-240AA)		
Circuit configuration	Two diodes common cathode		

### **MECHANICAL DESCRIPTION**

The AAP Gen 7, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

## FEATURES

- 175 °C T<sub>J</sub> operation
- Low forward voltage drop
- High frequency operation
- Low thermal resistance
- UL approved file E78996
- · Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

### BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- High surge capability
- Easy mounting on heatsink

## **ELECTRICAL DESCRIPTION / APPLICATIONS**

The VS-VSKCS203.. Schottky rectifier common cathode has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature.

Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	VALUES	UNITS		
I <sub>F(AV)</sub>	Rectangular waveform	200	А		
V <sub>RRM</sub>		100	V		
I <sub>FSM</sub>	t <sub>p</sub> = 5 μs sine	12 800	А		
V <sub>F</sub>	100 A <sub>pk</sub> , T <sub>J</sub> = 125 °C	0.87	V		
TJ	Range	-55 to +175	۵°		

VOLTAGE RATINGS				
PARAMETER	SYMBOL	VS-VSKCS203/100	UNITS	
Maximum DC reverse voltage	V <sub>R</sub>	100	V	
Maximum working peak reverse voltage	V <sub>RWM</sub>	100	v	

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ABSOLUTE MAXIMUM RATINGS						
PARAMETER		SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average	per module		50 % duty cycle at $T_{\rm C}$ = 121 °C, rectangular waveform		200	
forward current	per leg		$30\%$ duty cycle at $1_{\rm C} = 121$ C	, rectarigular wavelonn	100	
Maximum peak one cycle		I <sub>FSM</sub>	5 µs sine or 3 µs rect. pulse	Following any rated load condition and with rated V <sub>RRM</sub> applied	12 800	A
non-repetitive surge current	on-repetitive surge current		10 ms sine or 6 ms rect. pulse		1700	
Non-repetitive avalanche energ	у	E <sub>AS</sub>	T <sub>J</sub> = 25 °C, I <sub>AS</sub> = 5.5 A, L = 1 mH		15	mJ
Repetitive avalanche current		I <sub>AR</sub>	Current decaying linearly to zero in 1 $\mu$ s Frequency limited by T <sub>J</sub> maximum V <sub>A</sub> = 1.5 x V <sub>R</sub> typical 1		А	

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	L TEST CONDITIONS VALU		VALUES	UNITS
Maximum forward voltage drop	V <sub>FM</sub>	100 A	T <sub>J</sub> = 25 °C	0.99	V
		200 A		1.34	
		100 A	- T <sub>J</sub> = 125 °C	0.87	
		200 A		1.09	
	I <sub>RM</sub>	T <sub>J</sub> = 25 °C	V <sub>R</sub> = Rated V <sub>R</sub>	3	mA
Maximum reverse leakage current		T <sub>J</sub> = 125 °C		65	
Maximum junction capacitance	CT	$V_{R} = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz), 25 °C		2750	pF
Typical series inductance	L <sub>S</sub>	Measured lead to lead 5 mm from package body		7.0	nH
Maximum voltage rate of change	dV/dt	Rated V <sub>R</sub>		10 000	V/µs
Maximum RMS insulation voltage	V <sub>INS</sub>	50 Hz		3000 (1 min) 3600 (1 s)	V

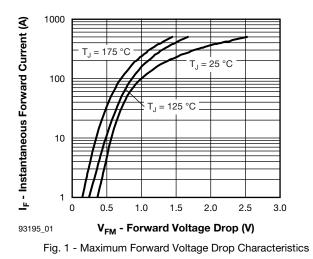
THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	)	T <sub>J</sub> , T <sub>Stg</sub>		-55 to +175	°C
Maximum thermal resistance, junction to case per leg		R <sub>thJC</sub>	DC operation	0.52	°C/W
Typical thermal resistance, case to heatsink per module		R <sub>thCS</sub>		0.1	
Approximate weight				75	g
Approximate weight				2.7	oz.
Mounting torque ± 10 %		A mounting compound is recommended and the torque should be rechecked after a period of 3 h to allow for the	4	Nm	
	busbar		spread of the compound.	3	
Case style			JEDEC®	TO-240AA co	mpatible

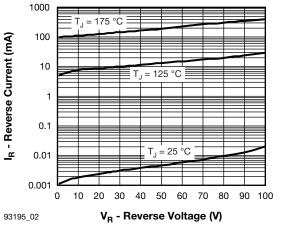
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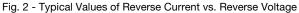


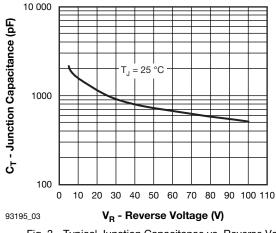
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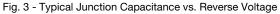
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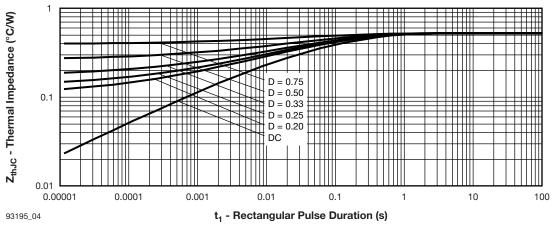
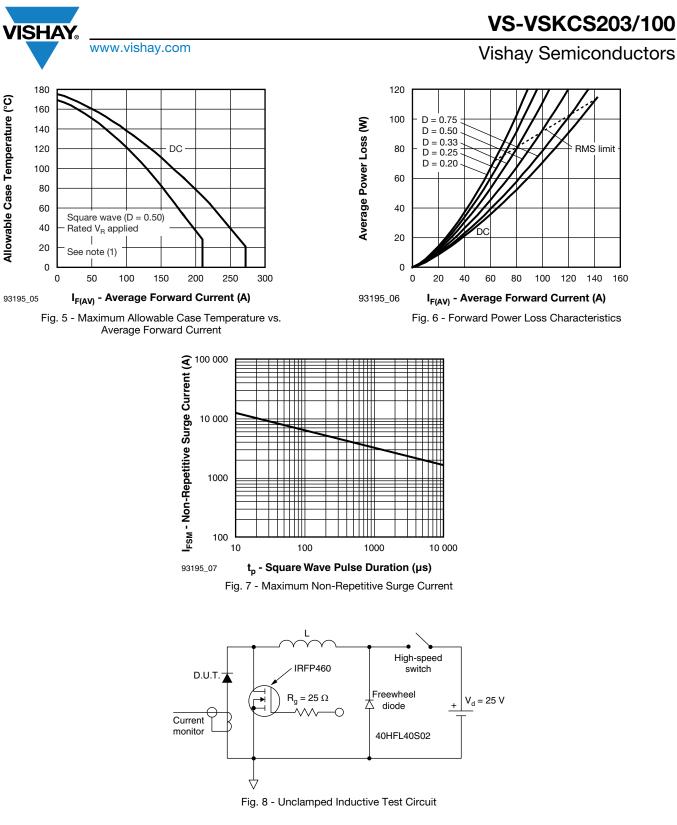


Fig. 4 - Maximum Thermal Impedance Z<sub>thJC</sub> Characteristics

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#### Note

- <sup>(1)</sup> Formula used:  $T_C = T_J (Pd + Pd_{REV}) \times R_{thJC}$ ;
- Pd = forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 6);
- $Pd_{REV}$  = inverse power loss =  $V_{R1} \times I_R (1 D)$ ;  $I_R$  at  $V_{R1}$  = 80 % rated  $V_R$

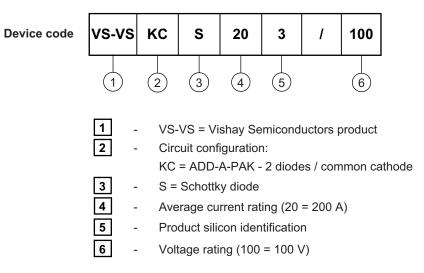
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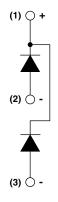
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### **ORDERING INFORMATION TABLE**



### **CIRCUIT CONFIGURATION**



LINKS TO RELATED DOCUMENTS			
Dimensions	www.vishay.com/doc?95369		

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## **ADD-A-PAK Generation VII - Diode**

### **DIMENSIONS** in millimeters (inches)





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