MX23L6422

3.3 Volt 64M-BIT (4M x 16 / 2M x 32) Mask ROM with Page Mode

FEATURES

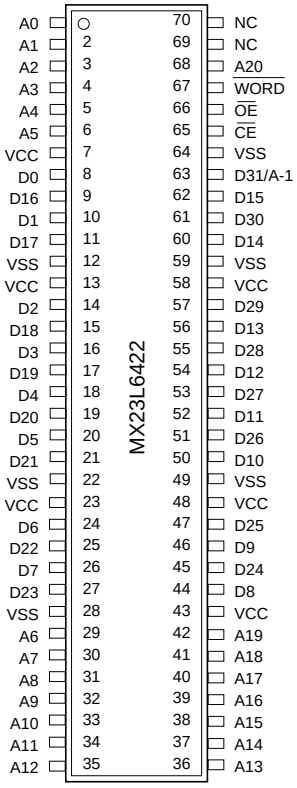
- Bit organization
  - 4M x 16 (byte mode)
  - 2M x 32 (double word mode)
- Fast access time
  - Random access: 110ns (max.) for 3.15~3.6V
    120ns (max.) for 3.0~3.6V
  - Page access: 30ns (max.)
- Page Size
  - 8 double words per page
- Current
  - Operating: 60mA (max.)
  - Standby: 20uA (max.)
- Supply voltage
  - 3.3V±10%
- Package
  - 70 pin SSOP
  - 86 pin TSOP(2)

ORDER INFORMATION

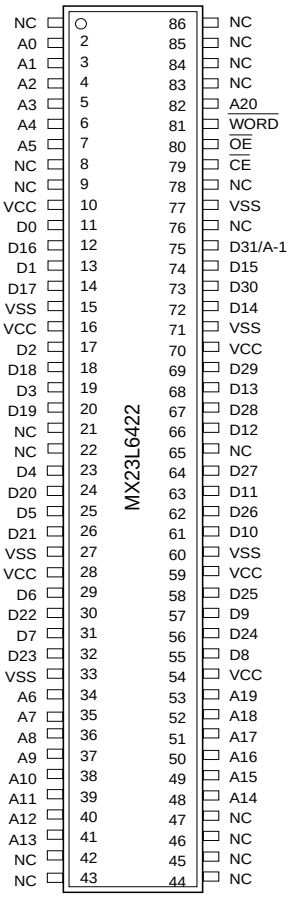
Part No.	Access Time	Page Access Time	Package
MX23L6422MC-11	110ns	30ns	70 pin SSOP
MX23L6422MC-12	120ns	50ns	70 pin SSOP
MX23L6422YC-12	120ns	50ns	86 pin TSOP

PIN CONFIGURATION

70 SSOP



86 TSOP(2)



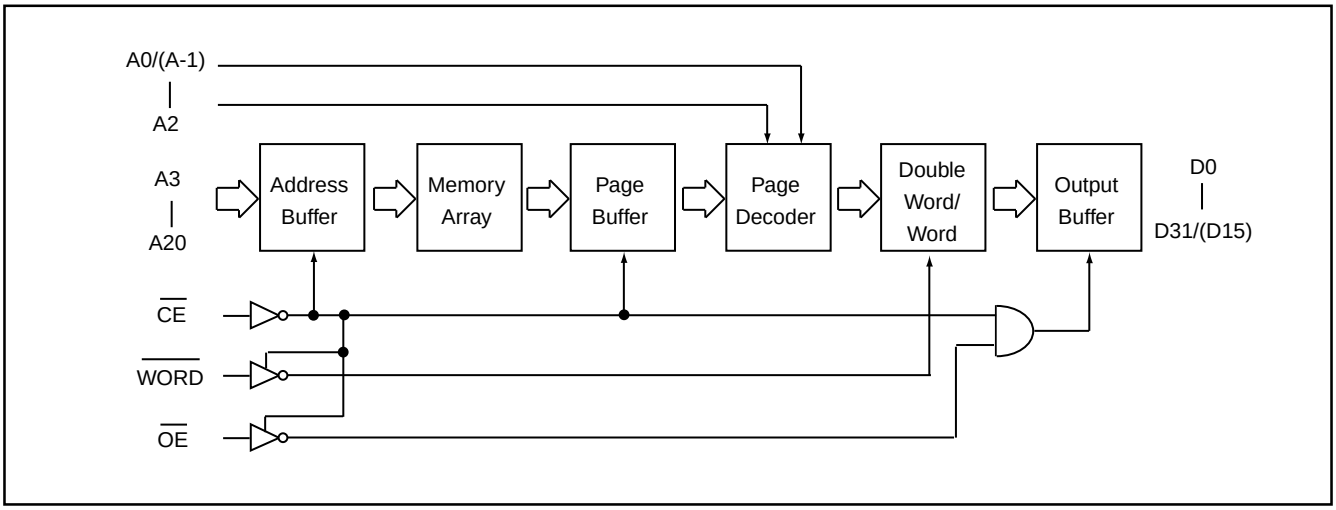
PIN DESCRIPTION

Symbol	Pin Function
A0~A20	Address Inputs
D0~D30	Data Outputs
D31/A-1	D31 (Double Word Mode)/ LSB Address (Word Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WORD}$	Double Word/ Word Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WORD}$	D31/A-1	D0~D15	D16~D31	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D15	D16~D31	Double Word	Active
L	L	L	Input	D0~D15	High Z	Word	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to 4.1V
Ambient Operating Temperature	Topr	0℃ to 70℃
Storage Temperature	Tstg	-65℃ to 125℃

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 3.3V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	10uA	0V, VCC
Output Leakage Current	ILO	-	10uA	0V, VCC
Operating Current	ICC1	-	60mA	tRC = 110ns, all output open, with normal sequential access testing pattern
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$ = VIH
Standby Current (CMOS)	ISTB2	-	20uA	$\overline{CE}$>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25℃, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25℃, f = 1MHZ

AC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 3.3V±10%)

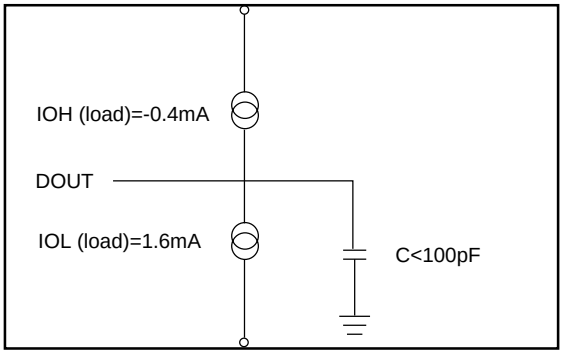
Item	Symbol	23L6422-11*		23L6422-12	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	110ns	-	120ns	-
Address Access Time	tAA	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	110ns	-	120ns
Page Mode Access Time	tPA	-	30ns	-	50ns
Output Enable Time	tOE	-	30ns	-	50ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

* 110ns for 3.15~3.6V

AC Test Conditions

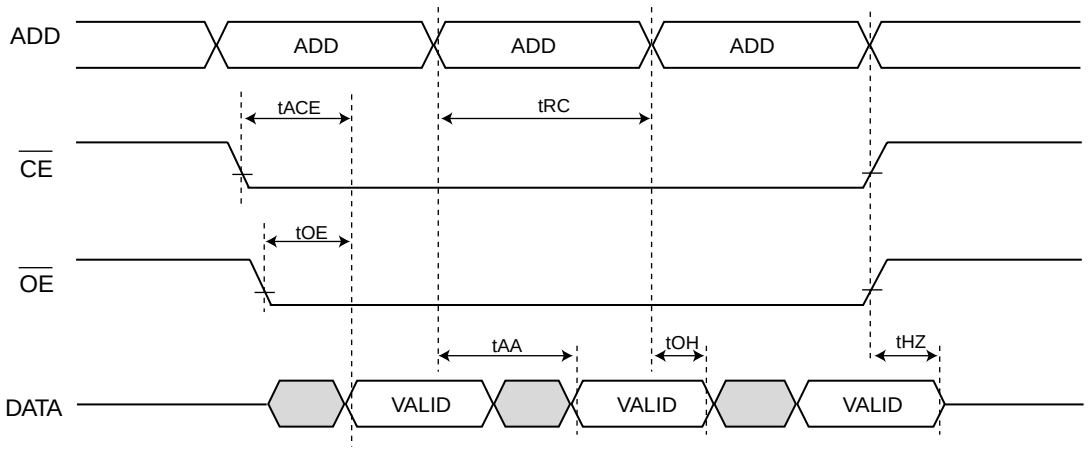
Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



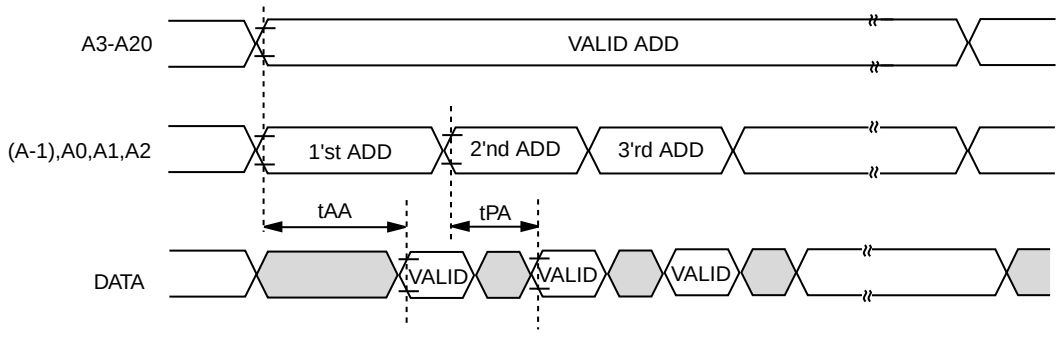
Note:No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

RANDOM READ



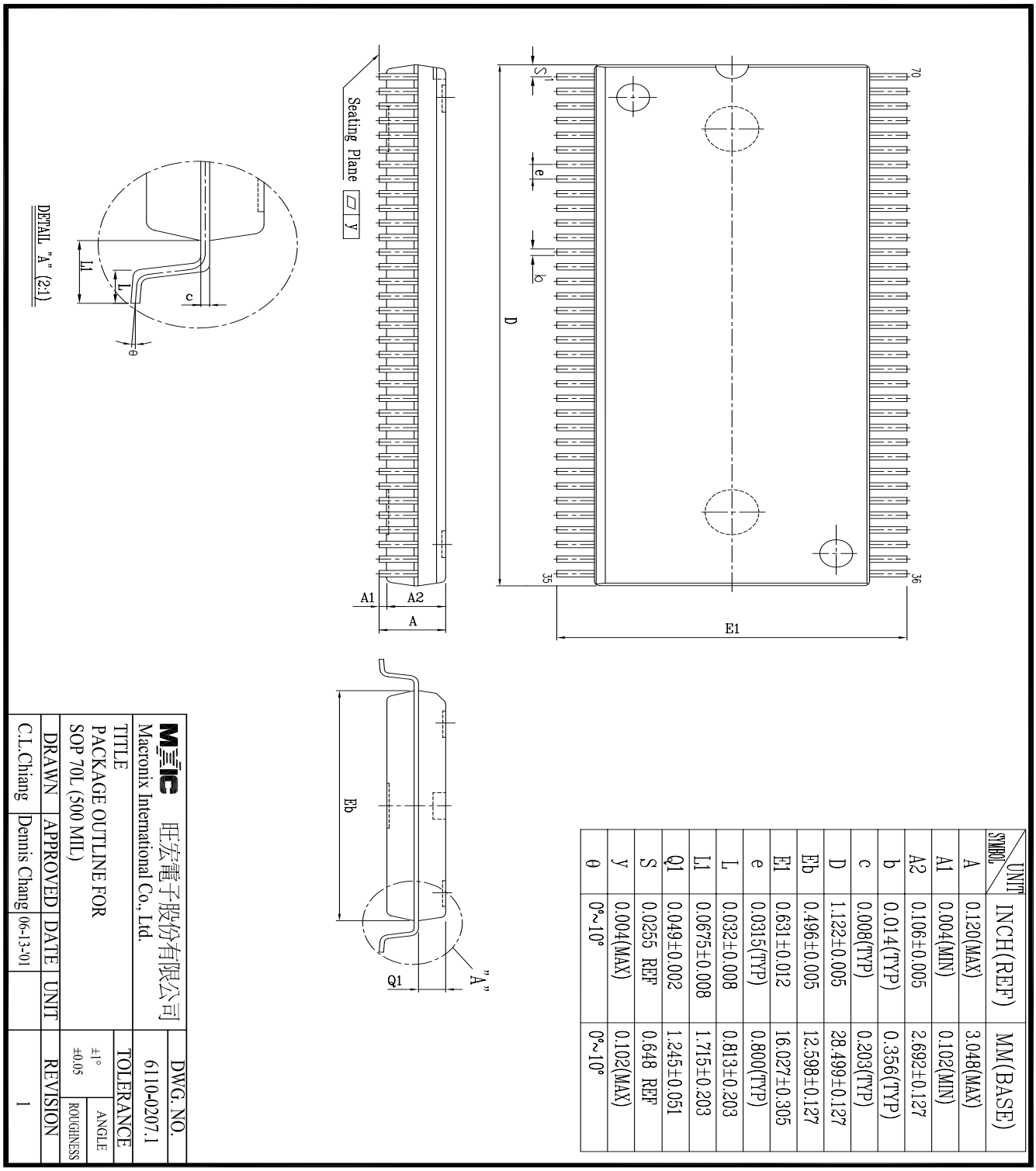
PAGE READ



Note: CE, OE are enable.
Page size is 8 double words in 32-bit mode, 16 words in 16-bit mode.

PACKAGE INFORMATION

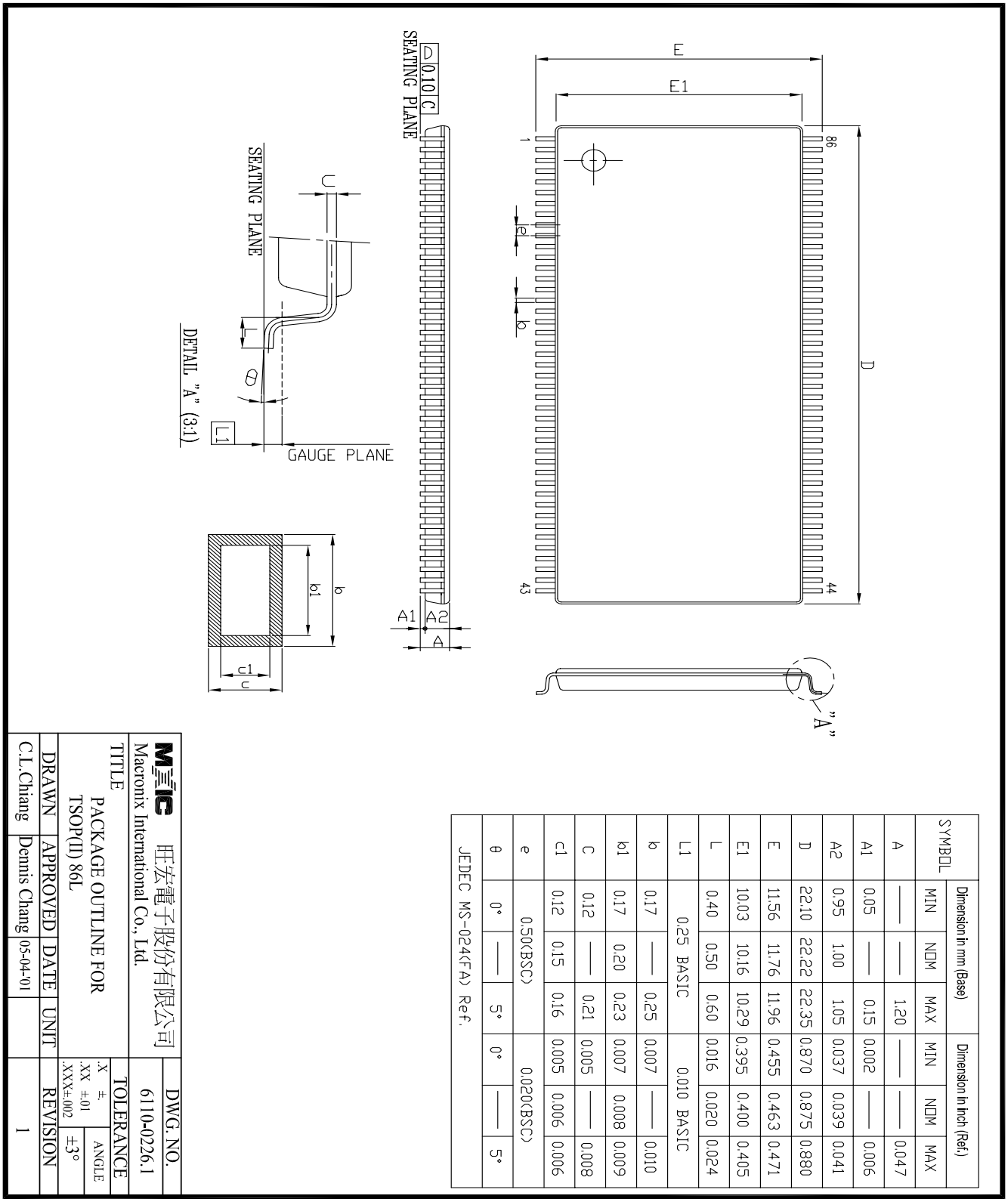
70 SSOP



SYMBOL / UNIT	INCH(REF)	MM(BASE)
A	0.120(MAX)	3.048(MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.106±0.005	2.692±0.127
b	0.014(TYP)	0.356(TYP)
c	0.008(TYP)	0.203(TYP)
D	1.122±0.005	28.499±0.127
Eb	0.496±0.005	12.598±0.127
E1	0.631±0.012	16.027±0.305
e	0.0315(TYP)	0.800(TYP)
L	0.032±0.008	0.813±0.203
L1	0.0675±0.008	1.715±0.203
Q1	0.049±0.002	1.245±0.051
S	0.0255 REF	0.648 REF
y	0.004(MAX)	0.102(MAX)
θ	0°~10°	0°~10°

MXIC 旺宏電子股份有限公司			DWG. NO.
Macronix International Co., Ltd.			6110-0207.1
TITLE			TOLERANCE
PACKAGE OUTLINE FOR			ANGLE ±1°
SOP 70L (500 MIL)			ROUGHNESS ±0.05
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Dennis Chang	06-13-01	
			REVISION
			1

86 TSOP



SYMBOL	Dimension in mm (Base)			Dimension in inch (Ref.)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	——	——	1.20	——	——	0.047
A1	0.05	——	0.15	0.002	——	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	22.10	22.22	22.35	0.870	0.875	0.880
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BASIC			0.010 BASIC		
b	0.17	——	0.25	0.007	——	0.010
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.12	——	0.21	0.005	——	0.008
c1	0.12	0.15	0.16	0.005	0.006	0.006
e	0.50(BSC)			0.020(BSC)		
θ	0°	——	5°	0°	——	5°

JEDEC MS-024(FA) Ref.

MIC	旺宏電子股份有限公司		DWG. NO.
Macronix International Co., Ltd.			6110-0226.1
TITLE			TOLERANCE
PACKAGE OUTLINE FOR TSOP(II) 86L			.X ± ANGLE
			.XX ±.01
			.XXX±.002 ±3°
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Dennis Chang	05-04-'01	
			REVISION
			1

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
2.1	AC CHARACTERISTICS tOH 10ns-->0ns	P4	JAN/29/1999
2.2	Add new 86pin TSOP(2) package	P1	APR/09/1999
	Add 100ns speed grade	P1,2	
	Delete 115ns speed grade	P4	
2.3	Change 100ns speed grade to 110ns	P4	SEP/14/1999
2.4	Add 110ns(max.) for 3.15~3.6V ; 120ns(max.) for 3.0~3.6V	P1	DEC/29/1999
2.5	Modify Operating Current : 40mA-->60mA	P1,3	JAN/13/2000
2.6	Modify Pin Configuration--100 TQFP D31-->D31/A-1; 86 TSOP NC-->D31/A-1	P2	DEC/26/2000
2.7	Delete package:100 pin TQFP	P1,2	OCT/19/2001
2.8	Add Package Information	P5,6	MAY/31/2002

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