AMERICAN MICROSYSTEMS, INC.

FS6372

ROM-Based 3-PLL Clock Generator IC

May 2000

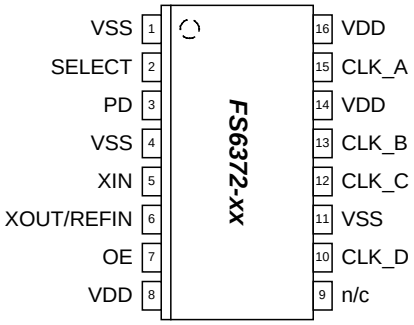
1.0 Features

- Fully compatible with FS6370 (EEPROM-based) and FS6377 (register-based) devices.
- Three on-chip PLLs with Reference and Feedback Dividers set by internal ROM look-up table
- Four independently programmable muxes and post dividers
- Selectable power-down of PLLs and shutdown of output clock drivers
- Tristate outputs for board testing
- Can be optimized for reference clock (instead of crystal) input
- 5V to 3.3V operation
- Commercial (FS6372) and industrial (FS6372i) temperature ranges

2.0 Description

The FS6372 is a CMOS clock generator IC designed to minimize cost and component count in a variety of electronic systems. Three phase-locked loops feeding four muxes and post dividers provide a high degree of flexibility.

Figure 1: Pin Configuration



16-pin (0.150") SOIC

Figure 2: Block Diagram

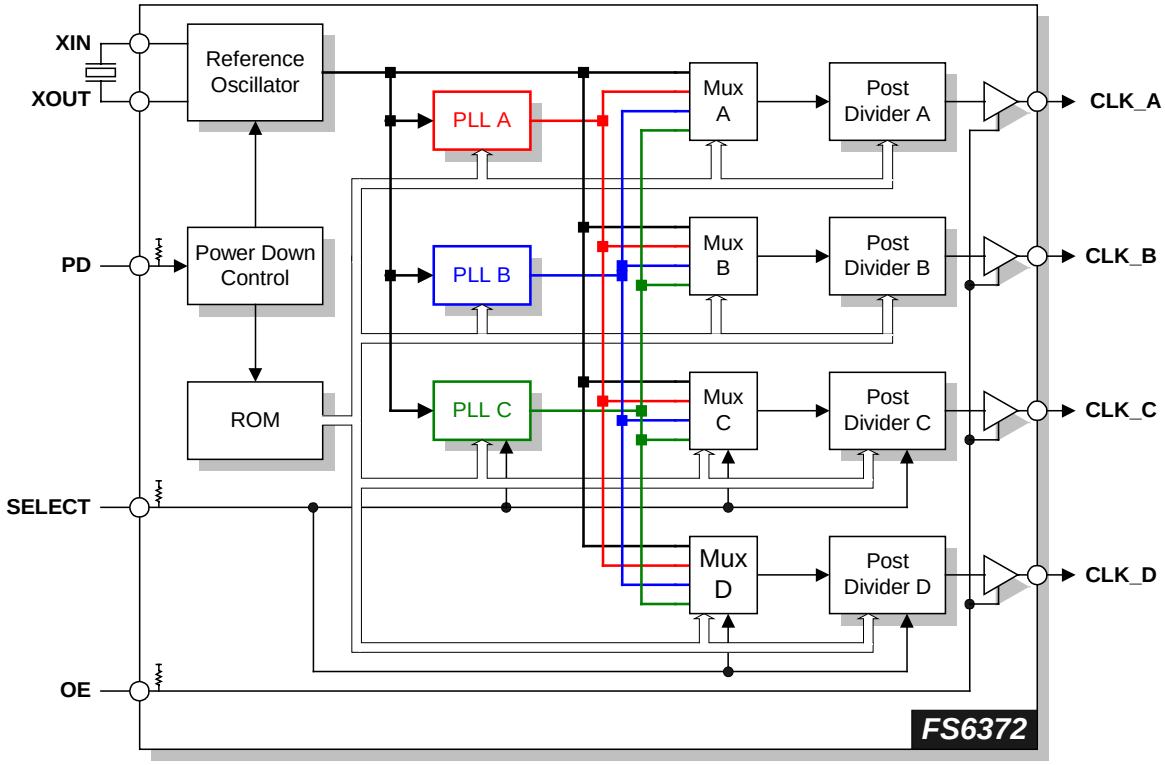


Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	P	VSS	Ground
2	DI^U	SELECT	Selects different device function (refer to specific variation of FS6372-xx for details)
3	DI^U	PD	Power-Down Input
4	P	VSS	Ground
5	AI	XIN	Crystal Oscillator Input
6	AO	XOUT / REFIN	Crystal Oscillator Output / Reference Clock Input
7	DI^U	OE	Output Enable Input
8	P	VDD	Power Supply (5V to 3.3V)
9	-	N/C	No Connect
10	DO	CLK_D	D Clock Output
11	P	VSS	Ground
12	DO	CLK_C	C Clock Output
13	DO	CLK_B	B Clock Output
14	P	VDD	Power Supply (5V to 3.3V)
15	DO	CLK_A	A Clock Output
16	P	VDD	Power Supply (5V to 3.3V)

May 2000

3.0 Electrical Specifications

Table 2: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage, dc (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		150	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 3: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	5V ± 10%	4.5	5	5.5	V
		3.3V ± 10%	3	3.3	3.6	
Ambient Operating Temperature Range	T_A	Commercial	0		70	°C
		Industrial	-40		85	
Crystal Resonator Frequency	f_{XIN}		5		27	MHz
Crystal Resonator Load Capacitance	C_{XL}	Parallel resonant, AT cut		18		pF
Output Driver Load Capacitance	C_L				15	pF

Table 4: DC Electrical Specifications

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σfrom typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	V_{DD} = 5.5V, f_{CLK} = 50MHz, C_L = 15pF		43		mA
Supply Current, Static	I_{DDL}	V_{DD} = 5.5V, device powered down		0.3		mA
Power-Down, Output Enable Pins (PD, OE)						
High-Level Input Voltage	V_{IH}	V_{DD} = 5.5V	3.85		V_{DD}+0.3	V
		V_{DD} = 3.6V	2.52		V_{DD}+0.3	
Low-Level Input Voltage	V_{IL}	V_{DD} = 5.5V	V_{SS}-0.3		1.65	V
		V_{DD} = 3.6V	V_{SS}-0.3		1.08	
Hysteresis Voltage	V_{hys}	V_{DD} = 5.5V		2.20		V
		V_{DD} = 3.6V		1.44		
High-Level Input Current	I_{IH}		-1		1	µA
Low-Level Input Current (pull-up)	I_{IL}	V_{IL} = 0V	-20	-36	-80	µA
Select (SELECT)						
High-Level Input Voltage	V_{IH}	V_{DD} = 5.5V	2.4		V_{DD}+0.3	V
		V_{DD} = 3.6V	2.0		V_{DD}+0.3	
Low-Level Input Voltage	V_{IL}	V_{DD} = 5.5V	V_{SS}-0.3		0.8	V
		V_{DD} = 3.6V	V_{SS}-0.3		0.8	
High-Level Input Current	I_{IH}		-1		1	µA
Low-Level Input Current (pull-up)	I_{IL}		-20	-36	-80	µA
Crystal Oscillator Feedback (XIN)						
Threshold Bias Voltage	V_{TH}	V_{DD} = 5.5V		2.9		V
		V_{DD} = 3.6V		1.7		
High-Level Input Current	I_{IH}	V_{DD} = 5.5V		54		µA
		V_{DD} = 5.5V, oscillator powered down	5		15	mA
Low-Level Input Current	I_{IL}	V_{DD} = 5.5V	-25	-54	-75	µA
Crystal Loading Capacitance *	$C_{L(xtal)}$	As seen by an external crystal connected to XIN and XOUT		18		pF
Input Loading Capacitance *	$C_{L(XIN)}$	As seen by an external clock driver on XOUT; XIN unconnected		36		pF

May 2000

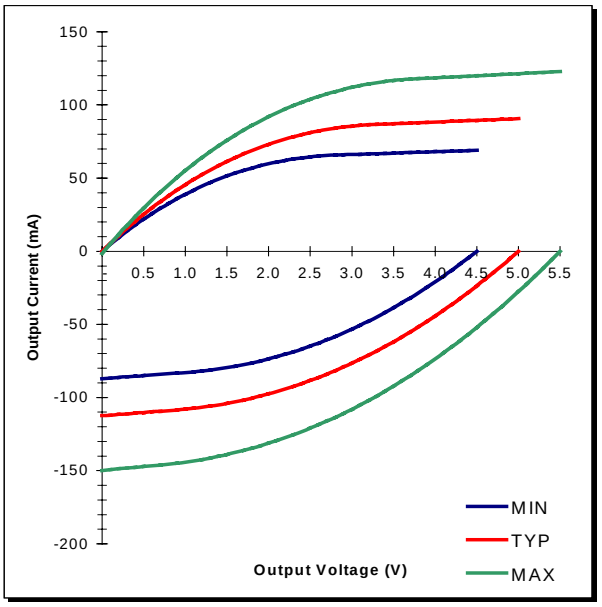
Table 5: DC Electrical Specifications, continued

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Crystal Oscillator Drive (XOUT)						
High-Level Output Source Current	I_{OH}	V_{DD} = V(XIN) = 5.5V, V_O = 0V	10	21	30	mA
Low-Level Output Sink Current	I_{OL}	V_{DD} = 5.5V, V(XIN) = 0V, V_O = 5.5V	-10	-21	-30	mA
Clock Outputs (CLK_A, CLK_B, CLK_C, CLK_D)						
High-Level Output Source Current	I_{OH}	V_O = 2.4V		-125		mA
Low-Level Output Sink Current	I_{OL}	V_O = 0.4V		23		mA
Output Impedance	z_{OH}	V_O = 0.5V_{DD}; output driving high		29		Ω
	z_{OL}	V_O = 0.5V_{DD}; output driving low		27		
Tristate Output Current	I_Z		-10		10	µA
Short Circuit Source Current *	I_{SCH}	V_{DD} = 5.5V, V_O = 0V; shorted for 30s, max.		-150		mA
Short Circuit Sink Current *	I_{SCL}	V_{DD} = V_O = 5.5V, shorted for 30s, max.		123		mA

Figure 3: CLK_A, CLK_B, CLK_C, CLK_D Clock Outputs

Voltage (V)	Low Drive Current (mA)			Voltage (V)	High Drive Current (mA)		
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.
0	0	0	0	0	-87	-112	-150
0.2	9	11	12	0.5	-85	-110	-147
0.5	22	25	29	1	-83	-108	-144
0.7	29	34	40	1.5	-80	-104	-139
1	39	46	55	2	-74	-97	-131
1.2	44	52	64	2.5	-65	-88	-121
1.5	51	61	76	2.7	-61	-84	-116
1.7	55	66	83	3	-53	-77	-108
2	60	73	92	3.2	-48	-71	-102
2.2	62	77	97	3.5	-39	-62	-92
2.5	65	81	104	3.7	-32	-55	-85
2.7	65	83	108	4	-21	-44	-74
3	66	85	112	4.2	-13	-36	-65
3.5	67	87	117	4.5	0	-24	-52
4	68	88	119	4.7		-15	-43
4.5	69	89	120	5		0	-28
5		91	121	5.2			-11
5.5			123	5.5			0



The data in this table represents nominal characterization data only.

Table 6: AC Timing Specifications

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Overall							
Output Frequency *	f_O	V_{DD} = 5.5V		0.8		150	MHz
		V_{DD} = 3.6V		0.8		100	
VCO Frequency *	f_{VCO}	V_{DD} = 5.5V		40		230	MHz
		V_{DD} = 3.6V		40		170	
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			1.9		ns
		V_O = 0.3V to 3.0V; C_L = 15pF			1.6		
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			1.8		ns
		V_O = 3.0V to 0.3V; C_L = 15pF			1.5		
Tristate Enable Delay *	t_{PZL}, t_{PZH}			1		8	ns
Tristate Disable Delay *	t_{PLZ}, t_{PHZ}			1		8	ns
Clock Stabilization Time *	t_{STB}	Output active from power-up, via PD pin			100		µs
Clock Outputs (PLL A clock via CLK_A pin)							
Duty Cycle *		Ratio of pulse width (as measured from rising edge to next falling edge at 2.5V) to one clock period	100	45		55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 2.5V relative to an ideal clock, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, No other PLLs active	100		45		ps
		On rising edges 500µs apart at 2.5V relative to an ideal clock, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, all other PLLs active (B=60MHz, C=40MHz, D=14.318MHz)	50		165		
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, No other PLLs active	100		110		ps
		From rising edge to the next rising edge at 2.5V, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, all other PLLs active (B=60MHz, C=40MHz, D=14.318MHz)	50		390		

May 2000

Table 7: AC Timing Specifications, continued

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Clock Outputs (PLL B clock via CLK_B pin)							
Duty Cycle *		Ratio of pulse width (as measured from rising edge to next falling edge at 2.5V) to one clock period	100	45		55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 2.5V relative to an ideal clock, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, No other PLLs active	100		45		ps
		On rising edges 500µs apart at 2.5V relative to an ideal clock, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, all other PLLs active (A=50MHz, C=40MHz, D=14.318MHz)	60		75		
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, No other PLLs active	100		120		ps
		From rising edge to the next rising edge at 2.5V, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, all other PLLs active (A=50MHz, C=40MHz, D=14.318MHz)	60		400		
Clock Outputs (PLL_C clock via CLK_C pin)							
Duty Cycle *		Ratio of pulse width (as measured from rising edge to next falling edge at 2.5V) to one clock period	100	45		55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 2.5V relative to an ideal clock, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, No other PLLs active	100		45		ps
		On rising edges 500µs apart at 2.5V relative to an ideal clock, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, all other PLLs active (A=50MHz, B=60MHz, D=14.318MHz)	40		105		
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, No other PLLs active	100		120		ps
		From rising edge to the next rising edge at 2.5V, C_L=15pF, f_{XIN}=14.318MHz, N_F=220, N_R=63, N_{Px}=50, all other PLLs active (A=50MHz, B=60MHz, D=14.318MHz)	40		440		
Clock Outputs (Crystal Oscillator via CLK_D pin)							
Duty Cycle *		Ratio of pulse width (as measured from rising edge to next falling edge at 2.5V) to one clock period	14.318	45		55	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	On rising edges 500µs apart at 2.5V relative to an ideal clock, C_L=15pF, f_{XIN}=14.318MHz, No other PLLs active	14.318		20		ps
		From rising edge to the next rising edge at 2.5V, C_L=15pF, f_{XIN}=14.318MHz, all other PLLs active (A=50MHz, B=60MHz, C=40MHz)	14.318		40		
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L=15pF, f_{XIN}=14.318MHz, No other PLLs active	14.318		90		ps
		From rising edge to the next rising edge at 2.5V, C_L=15pF, f_{XIN}=14.318MHz, all other PLLs active (A=50MHz, B=60MHz, C=40MHz)	14.318		450		

4.0 Package Information

Table 8: 16-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

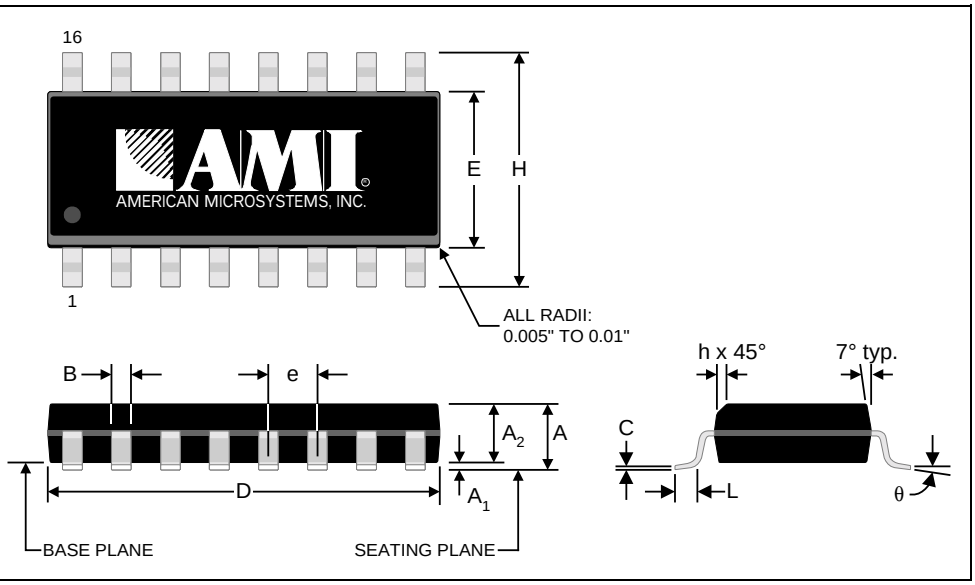


Table 9: 16-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air 16-pin 0.150" SOIC	Θ_{JA}	Air flow = 0 m/s	110	°C/W
Lead Inductance, Self	L_{11}	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.5	pF

May 2000

5.0 Ordering Information

5.1 Device Ordering Codes

DEVICE NUMBER	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS6372	11486-802	16-pin (0.150") SOIC (Small Outline Package)	0° C to 70° C (Commercial)	Tape-and-Reel
	11486-812	16-pin (0.150") SOIC (Small Outline Package)	0° C to 70° C (Commercial)	Tubes
	11486-902	16-pin (0.150") SOIC (Small Outline Package)	-40° C to 85° C (Industrial)	Tape-and-Reel
	11486-912	16-pin (0.150") SOIC (Small Outline Package)	-40° C to 85° C (Industrial)	Tubes

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