

September 2000

### 1.0 Features

- Generates all clocks required for single-processor platforms, including:
  - Two differential current-mode Host clock pairs
  - Three 66.67MHz 3.3V CK66 clock outputs
  - Ten 33.3MHz 3.3V PCI clock outputs
  - Two 3.3V Memory Reference clock outputs
  - Two 48MHz 3.3V CK48 clock outputs
  - Two buffered copies of the crystal reference
- Control of current-mode Host clocks via IREF current programming pin and ISEL\_0:1 current multiplier pins
- Host clock frequency selection via the SEL\_A, SEL\_B, and SEL133/100# pins
- Active-low PWR\_DWN# signal allows one complete clock cycle on each clock outputs and then shuts down the crystal oscillator, PLLs, and outputs
- Spread-spectrum modulation (-0.5% at 31.5kHz) of SSCG PLL clocks, enabled via SS\_EN# input
- Supports test mode and tristate output control to facilitate board testing
- Available in a 48-pin SSOP and TSSOP

Figure 1: Block Diagram

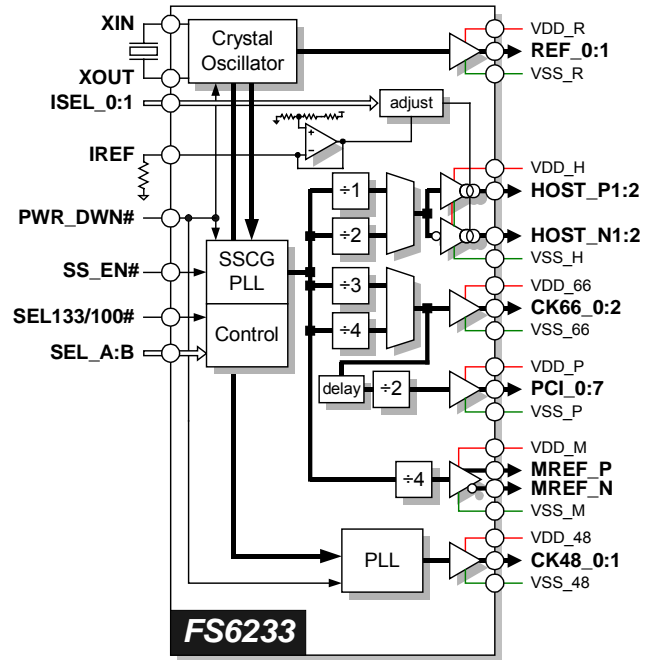


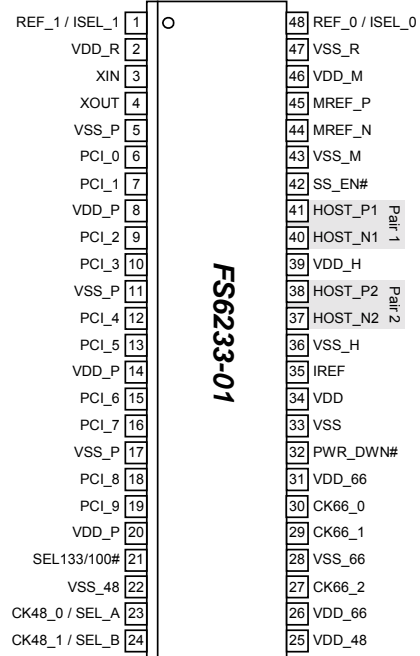
Figure 2: Pin Configuration

Table 1: Clock Parameters

| CLOCK GROUP | # PINS | SUPPLY VOLTAGE | SUPPLY GROUP | FREQ. (MHz) | PHASE | SKEW         |
|-------------|--------|----------------|--------------|-------------|-------|--------------|
| HOST_P      | 2      | 3.3V           | VDD_H        | 133.33      | 0°    | 150ps        |
| HOST_N      | 2      |                |              | 100.00      | 180°  | Pair to Pair |
| MREF_P      | 1      | 3.3V           | VDD_M        | 66.67       | 0°    | -            |
| MREF_N      | 1      |                |              | 50.00       | 180°  |              |
| CK66        | 3      | 3.3V           | VDD_66       | 66.67       | 0°    | 250ps        |
| PCI         | 10     | 3.3V           | VDD_P        | 33.33       | 0°    | 300ps        |
| CK48        | 2      | 3.3V           | VDD_48       | 48.008      | 0°    | -            |
| REF         | 2      | 3.3V           | VDD_R        | 14.318      | 0°    | -            |

Table 2: Clock Offsets

| RELATION       | PHASE | MIN   | TYP | MAX   |
|----------------|-------|-------|-----|-------|
| CK66 leads PCI | 0°    | 1.5ns |     | 3.5ns |



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## Motherboard Clock Generator IC



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### Table 3: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI<sup>U</sup> = Input with Internal Pull-Up; DI<sub>D</sub> = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active-low pin

| PIN                                       | TYPE | NAME               | DESCRIPTION   | SUPPLY |
|---|------|--------------------|---|--------|
| 48  | DIO  | CK48_0             | One of two 3.3V 48MHz clock outputs, generated from the non-spread PLL  | VDD_48 |
|   |      | SEL_A              | One of two latched inputs that select the HOST and MREF output frequency  |        |
| 24  | DIO  | CK48_1             | One of two 3.3V 48MHz clock outputs, generated from the non-spread PLL  | VDD_48 |
|   |      | SEL_B              | One of two latched inputs that select the HOST and MREF output frequency  |        |
| 30, 29, 27                                | DO   | CK66_0:3           | Three 3.3V 66.67MHz clock outputs, generated from the spread spectrum PLL   | VDD_66 |
| 41, 40                                    | AO   | HOST_P1<br>HOST_N1 | Host clock pair #1; one of two pairs of current-steering differential current-mode outputs. The current is established via a reference current at IREF and a multiplying factor set by ISEL_0:1 | VDD_H  |
| 38, 37                                    | AO   | HOST_P2<br>HOST_N2 | Host clock pair #2; one of two pairs of current-steering differential current-mode outputs  | VDD_H  |
| 35  | AI   | IREF               | A fixed precision resistor from this pin to ground provides a reference current used for the differential current-mode HOST clock outputs   | VDD    |
| 44  | DO   | MREF_N             | One clock (180° out of phase with MREF_P) in a pair of outputs provided as a reference clock to a memory clock driver   | VDD_M  |
| 45  | DO   | MREF_P             | One clock in a pair of outputs provided as a reference clock to a memory clock driver   | VDD_M  |
| 6, 7, 9, 10,<br>12, 13, 15,<br>16, 18, 19 | DO   | PCI_0:9            | Ten 3.3V 33.3MHz PCI clocks, lagging the CK66 clock by 1.5 to 3.5ns   | VDD_P  |
| 32  | DI   | PWR_DWN#           | Asynchronous active-low LVTTTL power-down signal shuts down oscillator and PLL, puts all clocks in low state. Complete clock cycles on all outputs will occur before shut down begins.          | VDD_48 |
| 2   | DIO  | REF_0              | One of two 3.3V buffered copies of the crystal reference frequency clock  | VDD_R  |
|   |      | ISEL_0             | One of two latched inputs that select the multiplying factor of the IREF reference current for the HOST pair outputs  |        |
| 1   | DIO  | REF_1              | One of two 3.3V buffered copies of the crystal reference frequency clock  | VDD_R  |
|   |      | ISEL_1             | One of two latched inputs that select the multiplying factor of the IREF reference current for the HOST pair outputs  |        |
| 21  | DI   | SEL133/100#        | Selects 133MHz (logic high) or 100MHz (logic low) Host clock frequency  | VDD_48 |
| 42  | DI   | SS_EN#             | Active low spread-spectrum enable turns on spread spectrum modulation   | VDD_M  |
| 34  | P    | VDD                | 3.3V core power supply  | -      |
| 25  | P    | VDD_48             | 3.3V power supply for CK48 clock outputs  | -      |
| 26, 31                                    | P    | VDD_66             | 3.3V power supply for CK66 clock outputs  | -      |
| 39  | P    | VDD_H              | 3.3V power supply for the differential HOST clock outputs   | -      |
| 46  | P    | VDD_M              | 3.3V power supply for MREF clock outputs  | -      |
| 8, 14, 20                                 | P    | VDD_P              | 3.3V power supply for PCI clock outputs   | -      |
| 2   | P    | VDD_R              | 3.3V power supply for the REF clock output and the crystal oscillator   | -      |
| 33  | P    | VSS                | Core ground   | -      |
| 22  | P    | VSS_48             | Ground for the CK48 clock outputs   | -      |
| 28  | P    | VSS_66             | Ground for the CK66 clock outputs   | -      |
| 36  | P    | VSS_H              | Ground for the differential HOST clock outputs  | -      |
| 43  | P    | VSS_M              | Ground for the MREF clock outputs   | -      |
| 5, 11, 17                                 | P    | VSS_P              | Ground for the PCI clock outputs  | -      |
| 47  | P    | VSS_R              | Ground for the REF clock outputs and the crystal oscillator   | -      |
| 3   | AI   | XIN                | 14.318MHz crystal oscillator input  | VDD_R  |
| 4   | AO   | XOUT               | 14.318MHz crystal oscillator output   | VDD_R  |

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## 2.0 Programming Information

**Table 4: Function/Clock Enable Configuration**

| CONTROL INPUTS <sup>(1)</sup> |              |       |       | CLOCK OUTPUTS (MHz) |               |                   |              |             |              |          |
|-------------------------------|--------------|-------|-------|---------------------|---------------|-------------------|--------------|-------------|--------------|----------|
| PWR_DWN#                      | SEL_133/100# | SEL_A | SEL_B | HOST_P<br>1:2       | HOST_N<br>1:2 | MREF_P,<br>MREF_N | CK66_<br>0:2 | PCI_<br>0:9 | CK48_<br>0:1 | REF      |
| 1                             | 0            | 0     | 0     | 100.00              | 100.00        | 50.00             | 66.67        | 33.33       | 48.008       | 14.318   |
| 1                             | 0            | 0     | 1     | reserved            | reserved      | reserved          | reserved     | reserved    | reserved     | reserved |
| 1                             | 0            | 1     | 0     | reserved            | reserved      | reserved          | reserved     | reserved    | reserved     | reserved |
| 1                             | 0            | 1     | 1     | tristate            | tristate      | tristate          | tristate     | tristate    | tristate     | tristate |
| 1                             | 1            | 0     | 0     | 133.33              | 133.33        | 66.67             | 66.67        | 33.33       | 48.008       | 14.318   |
| 1                             | 1            | 0     | 1     | reserved            | reserved      | reserved          | reserved     | reserved    | reserved     | reserved |
| 1                             | 1            | 1     | 0     | reserved            | reserved      | reserved          | reserved     | reserved    | reserved     | reserved |
| 1                             | 1            | 1     | 1     | XIN ÷ 2             | XIN ÷ 2       | XIN ÷ 4           | XIN ÷ 4      | XIN ÷ 8     | XIN ÷ 2      | XIN      |
| 0                             | X            | X     | X     | 2 × IREF            | tristate      | low               | low          | low         | low          | low      |

1. It is expected that the Control Inputs will be defined on power-up and will not change during normal operation.

**Table 5: Synthesis Error**

| CLOCK                   | TARGET (MHz) | ACTUAL (MHz) | DEVIATION (ppm) |
|-------------------------|--------------|--------------|-----------------|
| HOST_P1:2,<br>HOST_N1:2 | 100.0000     | 99.9963      | -36.657         |
|                         | 133.3333     | 133.3072     | -195.924        |
| MREF_P,<br>MREF_N       | 50.0000      | 49.9982      | -36.657         |
|                         | 66.6667      | 66.6536      | -195.924        |
| CK66                    | 66.6667      | 66.6642      | -36.657         |
| PCI                     | 33.3333      | 33.3321      | -36.657         |
| CK48 <sup>(1)</sup>     | 48.000       | 48.008       | +167            |

1. 48MHz USB clock is required to be +167ppm off from 48.000MHz to conform to USB standards.

2. Spread spectrum is disabled

## 3.0 HOST Buffer Current Control

The current supplied at the HOST outputs is controlled by two parameters:

- 1) the value of the programming resistor from the IREF pin to ground (VSS), and
- 2) the multiplier factor determined by the logic setting of the ISEL\_0 and ISEL\_1 pins.

### 3.1 Current Reference

The HOST output current is a mirrored and scaled copy of the reference current flowing through the programming resistor on the IREF pin. Conceptually, the circuit given in Figure 2 shows how the mirror current is generated.

The voltage that appears at the IREF pin is one-third of the voltage at the VDD\_I pin. The reference current is

$$I_{REF} = \frac{\left(\frac{1}{3} \times VDD\_I\right)}{R_{IREF}}$$

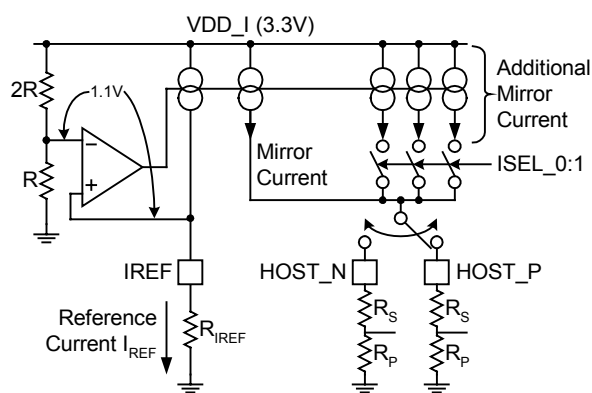
### 3.2 Current Scaling

The mirrored reference current can be increased by adding one or more copies of the mirror current together. The additional current is controlled by the logic settings on the ISEL\_0 and ISEL\_1 pins.

**Table 6: Current Multiplier**

| ISEL_0 | ISEL_1 | MULTIPLIER               |
|--------|--------|--------------------------|
| 0      | 0      | $I_o = 5 \times I_{REF}$ |
| 0      | 1      | $I_o = 6 \times I_{REF}$ |
| 1      | 0      | $I_o = 4 \times I_{REF}$ |
| 1      | 1      | $I_o = 7 \times I_{REF}$ |

**Figure 2: Current Reference Circuit**



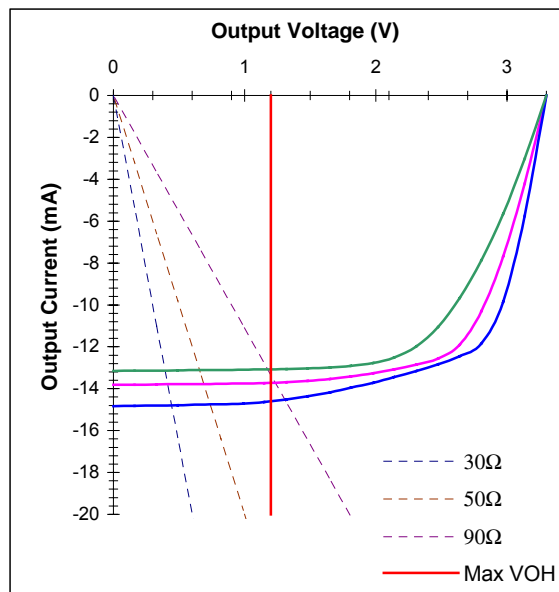
**Table 7: HOST Current Selection**

| PROGRAM RESISTOR $R_{REF}$ | REFERENCE CURRENT $I_{REF}$ | CURRENT MULTIPLIER       | TRACE IMPEDANCE | OUTPUT VOLTAGE |
|----------------------------|-----------------------------|--------------------------|-----------------|----------------|
| 475Ω (1%)                  | 2.32mA                      | $I_o = 5 \times I_{REF}$ | 60Ω             | 0.71V          |
| 475Ω (1%)                  | 2.32mA                      | $I_o = 6 \times I_{REF}$ | 50Ω             | 0.59V          |
| 475Ω (1%)                  | 2.32mA                      | $I_o = 4 \times I_{REF}$ | 60Ω             | 0.56V          |
| 475Ω (1%)                  | 2.32mA                      | $I_o = 7 \times I_{REF}$ | 50Ω             | 0.47V          |
| 475Ω (1%)                  | 2.32mA                      | $I_o = 7 \times I_{REF}$ | 60Ω             | 0.99V          |
| 475Ω (1%)                  | 2.32mA                      | $I_o = 7 \times I_{REF}$ | 50Ω             | 0.82V          |
| 221Ω (1%)                  | 5mA                         | $I_o = 5 \times I_{REF}$ | 30Ω             | 0.75V          |
| 221Ω (1%)                  | 5mA                         | $I_o = 5 \times I_{REF}$ | 25Ω             | 0.62V          |
| 221Ω (1%)                  | 5mA                         | $I_o = 6 \times I_{REF}$ | 30Ω             | 0.90V          |
| 221Ω (1%)                  | 5mA                         | $I_o = 6 \times I_{REF}$ | 25Ω             | 0.75V          |
| 221Ω (1%)                  | 5mA                         | $I_o = 4 \times I_{REF}$ | 30Ω             | 0.60V          |
| 221Ω (1%)                  | 5mA                         | $I_o = 4 \times I_{REF}$ | 25Ω             | 0.50V          |
| 221Ω (1%)                  | 5mA                         | $I_o = 7 \times I_{REF}$ | 30Ω             | 1.05V          |
| 221Ω (1%)                  | 5mA                         | $I_o = 7 \times I_{REF}$ | 25Ω             | 0.84V          |

NOTE: Shaded row indicates the Primary System Configuration

**Table 8: HOST Buffer Clock Outputs**

| Output Voltage (V) | HIGH DRIVE CURRENT (mA) AT PRIMARY SYSTEM CONFIGURATION |        |        |
|--------------------|---|--------|--------|
|                    | MIN.  | TYP.   | MAX.   |
| 3.30               | 0.00  | 0.00   | 0.00   |
| 3.14               | -3.03   | -4.22  | -5.76  |
| 2.97               | -5.66   | -7.68  | -9.86  |
| 2.81               | -7.87   | -10.30 | -11.85 |
| 2.64               | -9.67   | -11.91 | -12.45 |
| 2.48               | -11.05  | -12.56 | -12.84 |
| 2.31               | -11.98  | -12.85 | -13.16 |
| 2.14               | -12.52  | -13.07 | -13.45 |
| 1.98               | -12.77  | -13.26 | -13.72 |
| 1.81               | -12.91  | -13.42 | -13.96 |
| 1.65               | -12.99  | -13.54 | -14.17 |
| 1.48               | -13.04  | -13.64 | -14.36 |
| 1.32               | -13.07  | -13.70 | -14.52 |
| 1.15               | -13.08  | -13.73 | -14.64 |
| 0.99               | -13.09  | -13.75 | -14.71 |
| 0.82               | -13.11  | -13.76 | -14.74 |
| 0.66               | -13.12  | -13.78 | -14.76 |
| 0.49               | -13.13  | -13.79 | -14.78 |
| 0.33               | -13.13  | -13.80 | -14.80 |
| 0.16               | -13.14  | -13.81 | -14.82 |
| 0.00               | -13.15  | -13.82 | -14.83 |



Data in this table represents nominal characterization data only

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### 4.0 Power Management

The PWR\_DWN# signal is an asynchronous, active-low LVTTTL input that places the device in a low power inactive state without removing power from the device. All internal clocks are turned off, and all clock outputs are held low.

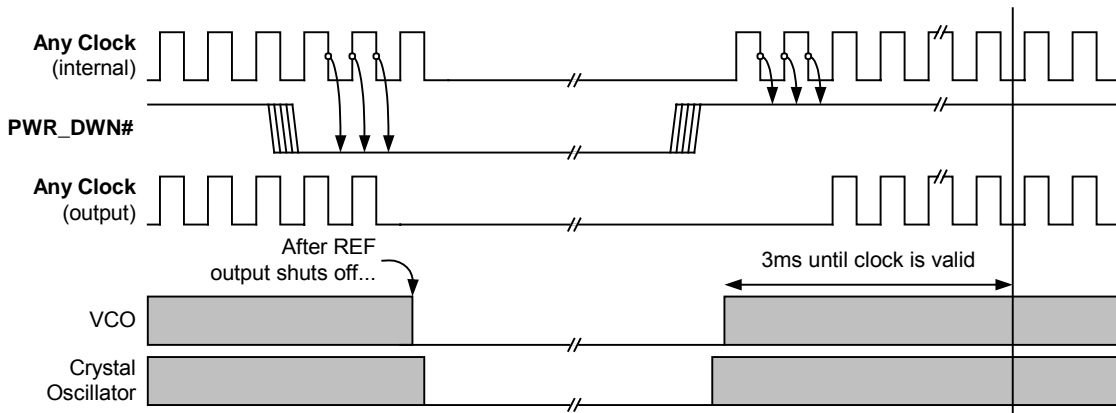
Since PWR\_DWN# is asynchronous, the signal is synchronized internally to each individual clock. As shown in Figure 3, a falling-rising-falling edge sequence on any individual clock output is required before that clock output is disabled low. This edge sequence ensures that one complete clock cycle will occur before the clock stops.

Table 9: Latency Table

| SIGNAL   | SIGNAL STATE |           | LATENCY |               |               |
|----------|--------------|-----------|---------|---------------|---------------|
|          |              |           |         | MIN.          | MAX.          |
| PWR_DWN# | 0            | Power OFF | Output: | 2 clocks      | 3 clocks      |
|          |              |           | Device: | 2× REF clocks | 3× REF clocks |
|          | 1            | Power ON  | 3ms     |               |               |

Upon the release of PWR\_DWN# (power-up), external circuitry should allow a minimum of 3ms for the PLL to lock before enabling any clocks.

Figure 3: PWR\_DWN# Timing



Shaded regions in the Crystal Oscillator and VCO waveforms indicate that the clock is valid and the Crystal Oscillator and VCO are active.

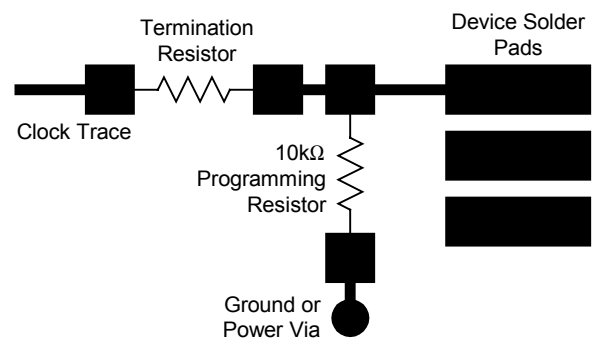
### 5.0 Dual Function I/O Pins

Several pins on this device serve as dual function input/output pins. During the initial application of VDD to the device, this type of pin functions as an input pin. Upon completion of power-up, the logic state present on the pin is latched internally, and the pin is converted to an output driver.

An external 10kΩ pull-down resistor to ground is required for a logic low and a 10kΩ pull-up resistor to the clock output VDD is required for a logic high. The 10kΩ resistor presents an insignificant load to the output driver that should not affect the output clock.

Note that the latching of the logic state occurs only on the application of the chip supply voltage (VDD). The logic state on the pin is not latched if the PWR\_DWN# signal is used to power-down the device with VDD still applied.

Figure 4: I/O Pin Programming



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## 6.0 Electrical Specifications

**Table 10: Absolute Maximum Ratings**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

| PARAMETER   | SYMBOL   | MIN.         | MAX.         | UNITS |
|---|----------|--------------|--------------|-------|
| Supply Voltage ( $V_{SS} = \text{ground}$ )                             | $V_{DD}$ | $V_{SS}-0.5$ | 7            | V     |
| Input Voltage, dc   | $V_I$    | $V_{SS}-0.5$ | $V_{DD}+0.5$ | V     |
| Output Voltage, dc  | $V_O$    | $V_{SS}-0.5$ | $V_{DD}+0.5$ | V     |
| Input Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )                 | $I_{IK}$ | -50          | 50           | mA    |
| Output Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )                | $I_{OK}$ | -50          | 50           | mA    |
| Storage Temperature Range (non-condensing)                              | $T_S$    | -65          | 150          | °C    |
| Ambient Temperature Range, Under Bias                                   | $T_A$    | -55          | 125          | °C    |
| Junction Temperature  | $T_J$    |              | 125          | °C    |
| Lead Temperature (soldering, 10s)                                       |          |              | 260          | °C    |
| Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7) |          |              | 2            | kV    |



### **CAUTION: ELECTROSTATIC SENSITIVE DEVICE**

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

**Table 11: Operating Conditions**

| PARAMETER                          | SYMBOL     | CONDITIONS/DESCRIPTION                                     | MIN.   | TYP.   | MAX.  | UNITS |
|------------------------------------|------------|--|--------|--------|-------|-------|
| Supply Voltage                     | $V_{DD}$   | Core (VDD)   | 3.135  | 3.3    | 3.465 | V     |
|                                    |            | Clock Buffers (VDD_48, VDD_66, VDD_H, VDD_M, VDD_P, VDD_R) | 3.135  | 3.3    | 3.465 |       |
| Operating Temperature Range        | $T_A$      |  | 0      |        | 70    | °C    |
| Crystal Resonator Frequency        | $f_{XTAL}$ |  | 14.316 | 14.318 | 14.32 | MHz   |
| Crystal Resonator Load Capacitance | $C_{XL}$   | XIN, XOUT pins   | 13.5   | 18     | 22.5  | pF    |
| Load Capacitance                   | $C_L$      | MREF_P, MREF_N   | 10     |        | 30    | pF    |
|                                    |            | PCI_0:9  | 10     |        | 30    |       |
|                                    |            | CK66_0:2   | 10     |        | 30    |       |
|                                    |            | CK48_0:1   | 10     |        | 20    |       |
|                                    |            | REF_0:1  | 10     |        | 20    |       |
| Load Resistance                    | $R_L$      | HOST_P1 to HOST_P2,<br>HOST_N1 to HOST_N2                  | 20     |        | 105   | Ω     |
| Maximum High-Level Output Voltage  | $V_{OH}$   | HOST_P1 to HOST_P2,<br>HOST_N1 to HOST_N2                  |        |        | 1.20  | V     |

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**Table 12: DC Electrical Specifications**

Unless otherwise stated, all power supplies = 3.3V ± 5%, no load on any output, and ambient temperature range  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are  $\pm 3\sigma$  from typical. Negative currents indicate current flows out of the device.

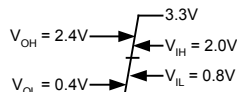
| PARAMETER   | SYMBOL        | CONDITIONS/DESCRIPTION   | MIN.         | TYP. | MAX.         | UNITS         |
|---|---------------|--|--------------|------|--------------|---------------|
| <b>Overall</b>  |               |  |              |      |              |               |
| Supply Current, Dynamic, with Loaded Outputs                    | $I_{DD}$      | $f_{HOST} = 133\text{MHz}$ ; all supplies = 3.465V, $R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$ |              |      |              | mA            |
| Supply Current, Static  | $I_{DDs}$     | PWR_DWN# low, all supplies = 3.465V, $R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$                |              |      |              | $\mu\text{A}$ |
| <b>Digital Inputs (PWR_DWN#, SEL133/100#, SS_EN#)</b>           |               |  |              |      |              |               |
| High-Level Input Voltage  | $V_{IH}$      |  | 2.0          |      | $V_{DD}+0.3$ | V             |
| Low-Level Input Voltage   | $V_{IL}$      |  | $V_{SS}-0.3$ |      | 0.8          | V             |
| Input Leakage Current   | $I_{IL}$      |  | -5           |      | +5           | $\mu\text{A}$ |
| <b>Crystal Oscillator Feedback (XIN)</b>                        |               |  |              |      |              |               |
| Threshold Bias Voltage  | $V_{TH}$      |  |              | 1.5  |              | V             |
| High-Level Input Current  | $I_{IH}$      | $V_{IH} = 3.3\text{V}$   |              | 32   |              | $\mu\text{A}$ |
| Low-Level Input Current   | $I_{IL}$      | $V_{IL} = 0\text{V}$   |              | -32  |              | $\mu\text{A}$ |
| Crystal Loading Capacitance *                                   | $C_{L(xtal)}$ | As seen by an external crystal connected to XIN and XOUT   | 13.5         | 18   | 22.5         | pF            |
| Input Loading Capacitance *                                     | $C_{L(XIN)}$  | As seen by an external clock driver on XOUT; XIN unconnected   |              | 36   |              | pF            |
| <b>Crystal Oscillator Drive (XOUT)</b>                          |               |  |              |      |              |               |
| High Level Output Source Current                                | $I_{OH}$      | $V_{I(XIN)} = 3.3\text{V}$ , $V_O = 0\text{V}$   |              | -8.0 |              | mA            |
| Low Level Output Sink Current                                   | $I_{OL}$      | $V_{I(XIN)} = 0\text{V}$ , $V_O = 3.3\text{V}$   |              | 8.7  |              | mA            |
| <b>Current Reference (IREF)</b>                                 |               |  |              |      |              |               |
| Bias Voltage  | $V_{OH}$      | no load  |              | 1.1  |              | V             |
| Short Circuit Output Source Current                             | $I_{OH}$      | $V_O = 0\text{V}$  |              |      |              | mA            |
| <b>MREF_P, MREF_N, CK66_0:2, PCI_0:9 Clock Outputs (Type 5)</b> |               |  |              |      |              |               |
| High Level Output Source Current                                | $I_{OH\ min}$ | $V_{DD\_M}, V_{DD\_66}, V_{DD\_P} = 3.135\text{V}$ , $V_O = 1.0\text{V}$                                 | -33          |      |              | mA            |
|   | $I_{OH\ max}$ | $V_{DD\_M}, V_{DD\_66}, V_{DD\_P} = 3.465\text{V}$ , $V_O = 3.135\text{V}$                               |              |      | -33          |               |
| Low Level Output Sink Current                                   | $I_{OL\ min}$ | $V_{DD\_M}, V_{DD\_66}, V_{DD\_P} = 3.135\text{V}$ , $V_O = 1.95\text{V}$                                | 30           |      |              | mA            |
|   | $I_{OL\ max}$ | $V_{DD\_M}, V_{DD\_66}, V_{DD\_P} = 3.465\text{V}$ , $V_O = 0.4\text{V}$                                 |              |      | 38           |               |
| Output Impedance  | $Z_{OL}$      | Measured at 1.65V, output driving low  | 12           |      | 55           | $\Omega$      |
|   | $Z_{OH}$      | Measured at 1.65V, output driving high   | 12           |      | 55           |               |
| Tristate Output Current   | $I_{OZ}$      |  | -10          |      | 10           | $\mu\text{A}$ |
| Short Circuit Output Source Current                             | $I_{OSH}$     | $V_O = 0\text{V}$ ; shorted for 30s, max.  |              | -51  |              | mA            |
| Short Circuit Output Sink Current                               | $I_{OSL}$     | $V_O = 3.3\text{V}$ ; shorted for 30s, max.  |              | 62   |              | mA            |

**Table 13: DC Electrical Specifications, continued**

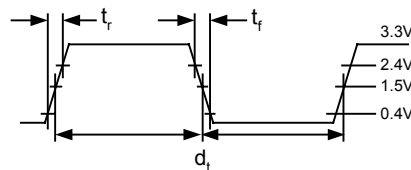
Unless otherwise stated, all power supplies = 3.3V ± 5%, no load on any output, and ambient temperature range  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are  $\pm 3\sigma$  from typical. Negative currents indicate current flows out of the device.

| PARAMETER   | SYMBOL          | CONDITIONS/DESCRIPTION   | MIN.   | TYP. | MAX.           | UNITS         |               |
|---|-----------------|--|--|------|----------------|---------------|---------------|
| <b>HOST_P1:2, HOST_N1:2 Clock Outputs (Type X1)</b>   |                 |  |  |      |                |               |               |
| Crossover Voltage   | $V_X$           | $R_S = 33.2\Omega$ , $R_P = 49.9\Omega$ ,<br>$R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$                                      | 45   |      | 55             | % $V_{OH}$    |               |
| High-Level Output Source Current  | $I_{OH}$        | $V_O = 0.65\text{V}$ , $R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$  | 12.9   |      |                | mA            |               |
|   |                 | $V_O = 0.74\text{V}$ , $R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$  |  |      | 14.9           |               |               |
| Output Source Current Tolerance   | $\Delta I_{OH}$ | $V_{DD} = 3.3\text{V}$ , over settings in Table 7  | -7   |      | +7             | % $I_{OH}$    |               |
|   |                 | $V_{DD\_I} = 3.3\text{V} \pm 5\%$ , over settings in Table 7   | -12  |      | +12            |               |               |
| Output Impedance  | $Z_{OH}$        | $\Delta V_O / \Delta I_O$ , where $V_{O1} = 1.0\text{V}$ , $V_{O2} = V_{SS}$ ,<br>$R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$ | 3000   |      |                | $\Omega$      |               |
| Tristate Output Current   | $I_{OZ}$        |  | -10  |      | 10             | $\mu\text{A}$ |               |
| <b>REF_0 / ISEL_0, REF_1 / ISEL_1 Clock Driver I/O, (Type 3)<br/>CK48_0 / SEL_A, CK48_1 / SEL_B Clock Driver I/O (Type 3)</b> |                 |  |  |      |                |               |               |
| High-Level Input Voltage  | Input           | $V_{IH}$   | 2.0  |      | $V_{DD} + 0.3$ | V             |               |
| Low-Level Input Voltage   |                 | $V_{IL}$   | $V_{SS} - 0.3$   |      | 0.8            | V             |               |
| High-Level Input Current  |                 | $I_{IH}$   |  |      | 5              | $\mu\text{A}$ |               |
| Low-Level Input Current (pull-up)   |                 | $I_{IL}$   | $V_{IL} = 0.4\text{V}$   |      | -9             | $\mu\text{A}$ |               |
| High Level Output Source Current  | Output          | $I_{OH}$   | $V_{DD\_R}$ , $V_{DD\_48} = 3.465\text{V}$ , $V_O = 2.4\text{V}$ | -32  |                | mA            |               |
| Low Level Output Sink Current   |                 | $I_{OL}$   | $V_{DD\_R}$ , $V_{DD\_48} = 3.465\text{V}$ , $V_O = 0.4\text{V}$ |      | 13             | mA            |               |
| Output Impedance  |                 | $Z_{OL}$   | Measured at 1.65V, output driving low                            | 20   |                | 60            | $\Omega$      |
|   |                 | $Z_{OH}$   | Measured at 1.65V, output driving high                           | 20   |                | 60            |               |
| Tristate Output Current   |                 | $I_{OZ}$   |  | -10  |                | 10            | $\mu\text{A}$ |
| Short Circuit Output Source Current   |                 | $I_{OSH}$  | $V_O = 0\text{V}$ ; shorted for 30s, max.                        |      | -41            |               | mA            |
| Short Circuit Output Sink Current   |                 | $I_{OSL}$  | $V_O = 3.3\text{V}$ ; shorted for 30s, max.                      |      | 40             |               | mA            |

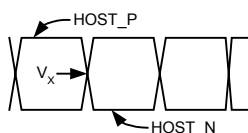
**Figure 5: DC Measurement Points**



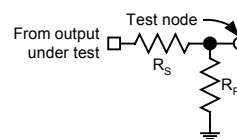
**Figure 6: Timing Diagram**



**Figure 7: HOST Clock Measurement Point**



**Figure 8: HOST Clock Test Point**





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**Table 14: AC Timing Specifications**

Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature  $T_A = 25^\circ\text{C}$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are  $\pm 3\sigma$  from typical. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

| PARAMETER                                 | SYMBOL              | CONDITIONS/DESCRIPTION  | MIN. | TYP. | MAX. | UNITS |
|---|---------------------|---|------|------|------|-------|
| <b>Overall</b>                            |                     |   |      |      |      |       |
| Spread Spectrum Modulation Frequency *    | $f_m$               | SS_EN# low  |      |      | 31.5 | kHz   |
| Spread Spectrum Modulation Index *        | $\delta_m$          | SS_EN# low  |      |      | -0.5 | %     |
| Clock Offset                              | $t_{pd}$            | CK66 leads @ 1.5V, $C_L=30\text{pF}$ to PCI @ 1.5V, $C_L = 30\text{pF}$ (measured on rising edges)  | 1.5  |      | 3.5  | ns    |
| Output Tristate Enable Delay *            | $t_{DZL}, t_{DZH}$  | SEL_A:B = 00, SEL133/100# = 0   | 1.0  |      | 10   | ns    |
| Output Tristate Disable Delay *           | $t_{DLZ}, t_{DHZ}$  | SEL_A:B = 11, SEL133/100# = 0   | 1.0  |      | 10   | ns    |
| Power-up PLL Lock Time                    | $t_L$               | via PWR_DWN#  |      |      | 3.0  | ms    |
| <b>HOST_P1:2, HOST_N1:2 Clock Outputs</b> |                     |   |      |      |      |       |
| Clock Skew *                              | $t_{sk(o)}$         | HOST pair to HOST pair @ $V_X$ , $R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$ , $R_S = 33.2\Omega$ , $R_P = 49.9\Omega$                     |      |      | 150  | ps    |
| Duty Cycle *                              | $d_t$               | Ratio of high pulse width to one clock period at $V_X$ , $R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$ , $R_S=33.2\Omega$ , $R_P=49.9\Omega$ | 45   |      | 55   | %     |
| Jitter, Period (peak-peak) *              | $t_{j(\Delta P)}$   | Rising edge to rising edge at $V_X$ , $R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$ , $R_S = 33.2\Omega$ , $R_P = 49.9\Omega$                |      |      | 200  | ps    |
| Rise Time *                               | $t_r$               | Measured at 20% – 80% of $V_{OH}$ ; $R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$ , $R_S = 33.2\Omega$ , $R_P = 49.9\Omega$                  | 175  |      | 450  | ps    |
| Rise/Fall Time Matching*                  |                     | Measured at 20% – 80% of $V_{OH}$ ; $R_{IREF} = 475\Omega$ , $I_{OH} = 6 \times I_{REF}$ , $R_S = 33.2\Omega$ , $R_P = 49.9\Omega$                  |      |      | 20   | %     |
| <b>MREF_P, MREF_N Clock Outputs</b>       |                     |   |      |      |      |       |
| Duty Cycle *                              | $d_t$               | Ratio of high pulse width to one clock period, measured at 1.5V   | 45   |      | 55   | %     |
| Jitter, Period (peak-peak) *              | $t_{j(\Delta P)}$   | From rising edge to rising edge at 1.5V, $C_L=30\text{pF}$  |      |      | 250  | ps    |
| Rise Time *                               | $t_{r \text{ min}}$ | Measured @ 0.4V – 2.4V; $C_L=10\text{pF}$   | 0.4  |      | 1.6  | ns    |
|   | $t_{r \text{ max}}$ | Measured @ 0.4V – 2.4V; $C_L=30\text{pF}$   |      |      |      |       |
| Fall Time *                               | $t_{f \text{ min}}$ | Measured @ 2.4V – 0.4V; $C_L=10\text{pF}$   | 0.4  |      | 1.6  | ns    |
|   | $t_{f \text{ max}}$ | Measured @ 2.4V – 0.4V; $C_L=30\text{pF}$   |      |      |      |       |

**Table 15: AC Timing Specifications, continued**

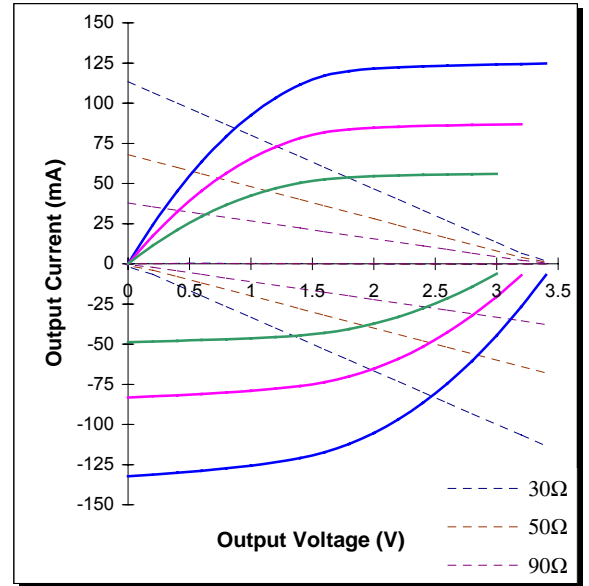
Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature  $T_A = 25^\circ\text{C}$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are  $\pm 3\sigma$  from typical. Spread spectrum modulation is disabled except for Rise/Fall time measurements.

| PARAMETER                     | SYMBOL            | CONDITIONS/DESCRIPTION  | MIN. | TYP. | MAX. | UNITS |
|-------------------------------|-------------------|---|------|------|------|-------|
| <b>PCI_0:9 Clock Outputs</b>  |                   |   |      |      |      |       |
| Duty Cycle *                  | $d_t$             | Ratio of high pulse width to one clock period, measured at 1.5V | 45   |      | 55   | %     |
| Clock Skew *                  | $t_{sk(o)}$       | One clock output relative to another at 1.5V                    |      |      | 500  | ps    |
| Jitter, Period (peak-peak) *  | $t_{j(\Delta P)}$ | From rising edge to rising edge at 1.5V, $C_L = 30\text{pF}$    |      |      | 500  | ps    |
| Rise Time *                   | $t_{r\ min}$      | Measured at 0.4V – 2.4V; $C_L = 10\text{pF}$                    | 0.5  |      |      | ns    |
|                               | $t_{r\ max}$      | Measured at 0.4V – 2.4V; $C_L = 30\text{pF}$                    |      |      | 2.0  |       |
| Fall Time *                   | $t_{f\ min}$      | Measured at 2.4V – 0.4V; $C_L = 10\text{pF}$                    | 0.5  |      |      | ns    |
|                               | $t_{f\ max}$      | Measured at 2.4V – 0.4V; $C_L = 30\text{pF}$                    |      |      | 2.0  |       |
| <b>CK66_0:2 Clock Outputs</b> |                   |   |      |      |      |       |
| Duty Cycle *                  | $d_t$             | Ratio of high pulse width to one clock period, measured at 1.5V | 45   |      | 55   | %     |
| Clock Skew *                  | $t_{sk(o)}$       | One clock output relative to another at 1.5V                    |      |      | 250  | ps    |
| Jitter, Period (peak-peak) *  | $t_{j(\Delta P)}$ | From rising edge to rising edge at 1.5V, $C_L = 30\text{pF}$    |      |      | 300  | ps    |
| Rise Time *                   | $t_{r\ min}$      | Measured at 0.4V – 2.4V; $C_L = 10\text{pF}$                    | 0.5  |      |      | ns    |
|                               | $t_{r\ max}$      | Measured at 0.4V – 2.4V; $C_L = 30\text{pF}$                    |      |      | 2.0  |       |
| Fall Time *                   | $t_{f\ min}$      | Measured at 2.4V – 0.4V; $C_L = 10\text{pF}$                    | 0.5  |      |      | ns    |
|                               | $t_{f\ max}$      | Measured at 2.4V – 0.4V; $C_L = 30\text{pF}$                    |      |      | 2.0  |       |
| <b>REF_0:1 Clock Outputs</b>  |                   |   |      |      |      |       |
| Duty Cycle *                  | $d_t$             | Ratio of high pulse width to one clock period, measured at 1.5V | 45   |      | 55   | %     |
| Jitter, Period (peak-peak) *  | $t_{j(\Delta P)}$ | From rising edge to rising edge at 1.5V, $C_L = 20\text{pF}$    |      |      | 1000 | ps    |
| Rise Time *                   | $t_{r\ min}$      | Measured at 0.4V – 2.4V; $C_L = 10\text{pF}$                    | 1.0  |      |      | ns    |
|                               | $t_{r\ max}$      | Measured at 0.4V – 2.4V; $C_L = 20\text{pF}$                    |      |      | 4.0  |       |
| Fall Time *                   | $t_{f\ min}$      | Measured at 2.4V – 0.4V; $C_L = 10\text{pF}$                    | 1.0  |      |      | ns    |
|                               | $t_{f\ max}$      | Measured at 2.4V – 0.4V; $C_L = 20\text{pF}$                    |      |      | 4.0  |       |
| <b>CK48_0:1 Clock Outputs</b> |                   |   |      |      |      |       |
| Duty Cycle *                  | $d_t$             | Ratio of high pulse width to one clock period, measured at 1.5V | 45   |      | 55   | %     |
| Jitter, Period (peak-peak) *  | $t_{j(\Delta P)}$ | From rising edge to rising edge at 1.5V, $C_L = 20\text{pF}$    |      |      | 350  | ps    |
| Rise Time *                   | $t_{r\ min}$      | Measured at 0.4V – 2.4V; $C_L = 10\text{pF}$                    | 1.0  |      |      | ns    |
|                               | $t_{r\ max}$      | Measured at 0.4V – 2.4V; $C_L = 20\text{pF}$                    |      |      | 4.0  |       |
| Fall Time *                   | $t_{f\ min}$      | Measured at 2.4V – 0.4V; $C_L = 10\text{pF}$                    | 1.0  |      |      | ns    |
|                               | $t_{f\ max}$      | Measured at 2.4V – 0.4V; $C_L = 20\text{pF}$                    |      |      | 4.0  |       |

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**Table 16: MCLK\_P, MCLK\_N, PCI\_0:9, CK66\_0:2 Clock Outputs**

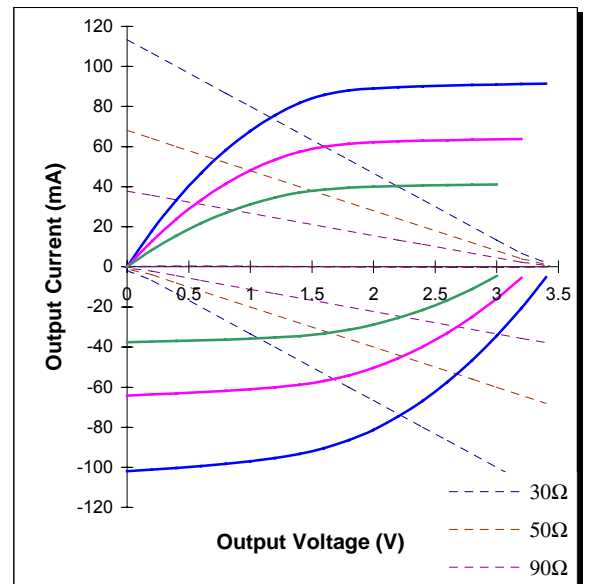
| Voltage (V) | High Drive Current (mA) |      |      | Voltage (V) | Low Drive Current (mA) |      |      |
|-------------|-------------------------|------|------|-------------|------------------------|------|------|
|             | MIN.                    | TYP. | MAX. |             | MIN.                   | TYP. | MAX. |
| 0           | 0                       | 0    | 0    | 0           | -49                    | -83  | -132 |
| 0.2         | 11                      | 17   | 24   | 0.2         | -48                    | -83  | -131 |
| 0.4         | 21                      | 32   | 45   | 0.4         | -48                    | -82  | -130 |
| 0.6         | 30                      | 45   | 64   | 0.6         | -47                    | -81  | -129 |
| 0.8         | 37                      | 56   | 79   | 0.8         | -47                    | -80  | -127 |
| 1.0         | 43                      | 65   | 92   | 1.0         | -46                    | -79  | -126 |
| 1.2         | 47                      | 73   | 103  | 1.2         | -46                    | -78  | -124 |
| 1.4         | 50                      | 78   | 112  | 1.4         | -45                    | -76  | -121 |
| 1.6         | 53                      | 82   | 117  | 1.6         | -43                    | -74  | -117 |
| 1.8         | 54                      | 84   | 120  | 1.8         | -41                    | -70  | -112 |
| 2.0         | 55                      | 85   | 121  | 2.0         | -37                    | -65  | -105 |
| 2.2         | 55                      | 85   | 122  | 2.2         | -33                    | -59  | -97  |
| 2.4         | 55                      | 86   | 123  | 2.4         | -28                    | -52  | -87  |
| 2.6         | 56                      | 86   | 123  | 2.6         | -22                    | -43  | -74  |
| 2.8         | 56                      | 86   | 124  | 2.8         | -14                    | -32  | -60  |
| 3.0         | 56                      | 87   | 124  | 3.0         | -6                     | -20  | -45  |
| 3.2         |                         | 87   | 124  | 3.2         |                        | -7   | -27  |
| 3.4         |                         |      | 125  | 3.4         |                        |      | -7   |



Data in this table represents nominal characterization data only

**Table 17: REF\_0:1, CK48\_0:1 Clock Outputs**

| Voltage (V) | High Drive Current (mA) |      |      | Voltage (V) | Low Drive Current (mA) |      |      |
|-------------|-------------------------|------|------|-------------|------------------------|------|------|
|             | MIN.                    | TYP. | MAX. |             | MIN.                   | TYP. | MAX. |
| 0           | 0                       | 0    | 0    | 0           | -38                    | -64  | -102 |
| 0.2         | 8                       | 13   | 18   | 0.2         | -37                    | -64  | -101 |
| 0.4         | 15                      | 24   | 33   | 0.4         | -37                    | -63  | -100 |
| 0.6         | 22                      | 33   | 47   | 0.6         | -37                    | -63  | -99  |
| 0.8         | 27                      | 41   | 58   | 0.8         | -36                    | -62  | -98  |
| 1.0         | 31                      | 48   | 68   | 1.0         | -36                    | -61  | -97  |
| 1.2         | 35                      | 53   | 76   | 1.2         | -35                    | -60  | -95  |
| 1.4         | 37                      | 57   | 82   | 1.4         | -34                    | -59  | -93  |
| 1.6         | 39                      | 60   | 86   | 1.6         | -33                    | -57  | -90  |
| 1.8         | 39                      | 61   | 88   | 1.8         | -31                    | -54  | -87  |
| 2.0         | 40                      | 62   | 89   | 2.0         | -29                    | -50  | -81  |
| 2.2         | 40                      | 63   | 90   | 2.2         | -25                    | -46  | -75  |
| 2.4         | 41                      | 63   | 90   | 2.4         | -21                    | -40  | -67  |
| 2.6         | 41                      | 63   | 90   | 2.6         | -17                    | -33  | -57  |
| 2.8         | 41                      | 63   | 91   | 2.8         | -11                    | -25  | -47  |
| 3.0         | 41                      | 64   | 91   | 3.0         | -5                     | -16  | -34  |
| 3.2         |                         | 64   | 91   | 3.2         |                        | -6   | -21  |
| 3.4         |                         |      | 91   | 3.4         |                        |      | -5   |



Data in this table represents nominal characterization data only

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## Motherboard Clock Generator IC



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### 7.0 Package Information

**Table 18: 48-pin SSOP (0.300") Package Dimensions**

|                | DIMENSIONS |        |             |       |
|----------------|------------|--------|-------------|-------|
|                | INCHES     |        | MILLIMETERS |       |
|                | MIN.       | MAX.   | MIN.        | MAX.  |
| A              | 0.095      | 0.110  | 2.41        | 2.79  |
| A <sub>1</sub> | 0.008      | 0.016  | 0.20        | 0.41  |
| b              | 0.008      | 0.0135 | 0.20        | 0.34  |
| c              | 0.005      | 0.010  | 0.13        | 0.25  |
| D              | 0.620      | 0.630  | 15.75       | 16.00 |
| E              | 0.395      | 0.420  | 10.03       | 10.67 |
| E <sub>1</sub> | 0.291      | 0.299  | 7.39        | 7.59  |
| e              | 0.025 BSC  |        | 0.64 BSC    |       |
| h              | 0.015      | 0.025  | 0.38        | 0.64  |
| L              | 0.020      | 0.040  | 0.51        | 1.01  |
| θ              | 0°         | 8°     | 0°          | 8°    |

The diagram shows the 48-pin SSOP package from three perspectives: top, side, and lead view. The top view shows the 48 pins and the LAMI logo. The side view shows the package height (A, E, E<sub>1</sub>) and the seating plane. The lead view shows the lead length (L), lead thickness (c), lead width (h), and lead angle (θ).

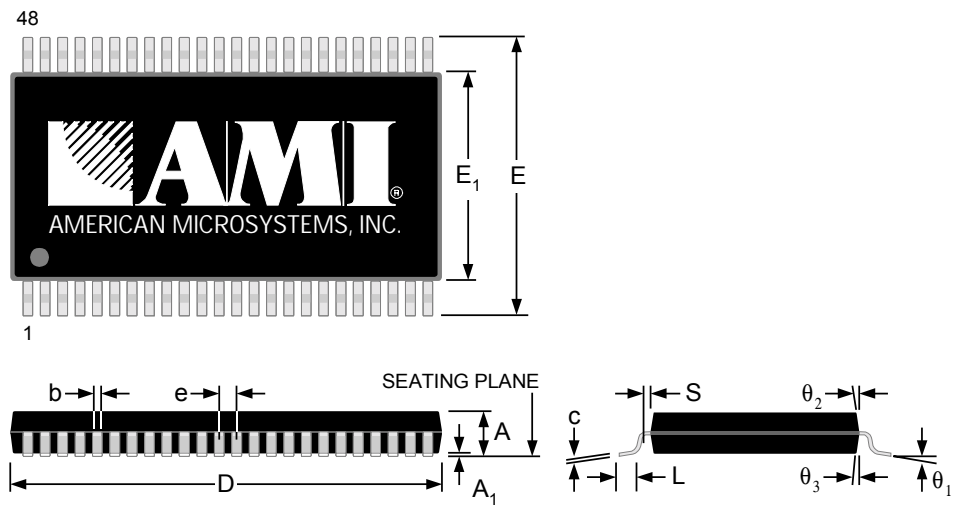
**Table 19: 48-pin SSOP (0.300") Package Characteristics**

| PARAMETER                               | SYMBOL          | CONDITIONS/DESCRIPTION                            | TYP. | UNITS |
|---|-----------------|---|------|-------|
| Thermal Impedance, Junction to Free-Air | $\Theta_{JA}$   | Air flow = 0 m/s                                  | 93   | °C/W  |
| Lead Inductance, Self                   | L <sub>11</sub> | Longest lead                                      | 5.5  | nH    |
| Lead Inductance, Mutual                 | L <sub>12</sub> | Longest lead to any 1 <sup>st</sup> adjacent lead | 3.0  | nH    |
|   | L <sub>13</sub> | Longest lead to any 2 <sup>nd</sup> adjacent lead | 2.1  |       |
| Lead Capacitance, Bulk                  | C <sub>11</sub> | Longest lead to V <sub>SS</sub>                   | 0.94 | pF    |
| Lead Capacitance, Mutual                | C <sub>12</sub> | Longest lead to any 1 <sup>st</sup> adjacent lead | 0.46 | pF    |
|   | C <sub>13</sub> | Longest lead to any 2 <sup>nd</sup> adjacent lead | 0.05 |       |

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**Table 20: 48-pin TSSOP (6.1mm) Package Dimensions**

|                | DIMENSIONS |       |             |       |
|----------------|------------|-------|-------------|-------|
|                | INCHES     |       | MILLIMETERS |       |
|                | MIN.       | MAX.  | MIN.        | MAX.  |
| A              | -          | 0.047 | -           | 1.20  |
| A <sub>1</sub> | 0.002      | 0.006 | 0.05        | 0.15  |
| b              | 0.0067     | 0.011 | 0.17        | 0.27  |
| c              | 0.0035     | 0.008 | 0.09        | 0.20  |
| D              | 0.488      | 0.496 | 12.40       | 12.60 |
| E              | 0.318 BSC  |       | 8.10 BSC    |       |
| E <sub>1</sub> | 0.236      | 0.244 | 6.00        | 6.20  |
| e              | 0.019 BSC  |       | 0.50 BSC    |       |
| L              | 0.018      | 0.030 | 0.45        | 0.75  |
| S              | 0.008      | -     | 0.20        | -     |
| θ <sub>1</sub> | 0°         | 8°    | 0°          | 8°    |
| θ <sub>2</sub> | 12° REF    |       | 12° REF     |       |
| θ <sub>3</sub> | 12° REF    |       | 12° REF     |       |



The diagram illustrates the mechanical dimensions of the 48-pin TSSOP package. The top view shows a rectangular package with 48 pins along the long edges. Dimensions include overall length (D), width (E), and lead pitch (e). The side view shows the package height (A), lead height (A<sub>1</sub>), and the seating plane. The lead detail view shows the lead thickness (S), lead length (L), and lead angle (θ<sub>1</sub>, θ<sub>2</sub>, θ<sub>3</sub>).

**Table 21: 48-pin TSSOP (6.1mm) Package Characteristics**

| PARAMETER                               | SYMBOL          | CONDITIONS/DESCRIPTION                            | TYP. | UNITS |
|---|-----------------|---|------|-------|
| Thermal Impedance, Junction to Free-Air | θ <sub>JA</sub> | Air flow = 0 m/s                                  | 89   | °C/W  |
| Lead Inductance, Self                   | L <sub>11</sub> | Longest lead                                      | 3.50 | nH    |
| Lead Inductance, Mutual                 | L <sub>12</sub> | Longest lead to any 1 <sup>st</sup> adjacent lead | 1.82 | nH    |
|   | L <sub>13</sub> | Longest lead to any 2 <sup>nd</sup> adjacent lead | 1.17 |       |
| Lead Capacitance, Bulk                  | C <sub>11</sub> | Longest lead to V <sub>SS</sub>                   | 0.63 | pF    |
| Lead Capacitance, Mutual                | C <sub>12</sub> | Longest lead to any 1 <sup>st</sup> adjacent lead | 0.30 | pF    |
|   | C <sub>13</sub> | Longest lead to any 2 <sup>nd</sup> adjacent lead | 0.03 |       |

# FS6233-01

## Motherboard Clock Generator IC



September 2000

## 8.0 Ordering Information

Table 22: Device Ordering Codes

| DEVICE NUMBER | ORDERING CODE | PACKAGE TYPE         | OPERATING TEMPERATURE RANGE | SHIPPING CONFIGURATION |
|---------------|---------------|----------------------|-----------------------------|------------------------|
| FS6233-01     | 11995-202     | 48-pin (0.300") SSOP | 0° C to 70° C (Commercial)  | Tape and Reel          |
|               | 11995-212     |                      |                             | Tubes                  |
|               | 11995-203     | 48-pin (6.1mm) TSSOP |                             | Tape and Reel          |
|               | 11995-213     |                      |                             | Tubes                  |

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