UNISONIC TECHNOLOGIES CO., LTD

12N50   Preliminary   *Power MOSFET*

12A, 500V N-CHANNEL POWER MOSFET

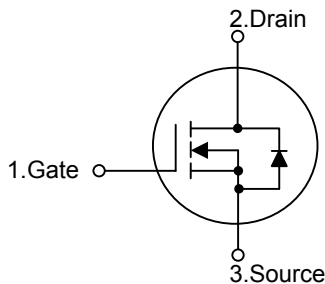TO-220

TO-220F1

TO-263
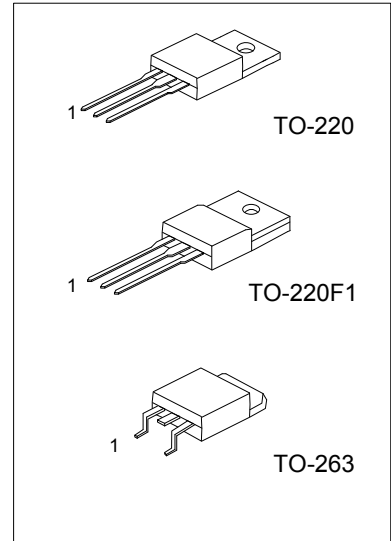
■ DESCRIPTION

The UTC **12N50** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **12N50** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

■ FEATURES

* $R_{DS(ON)}$=0.54Ω @ V_{GS}=10V
* High Switching Speed
* 100% Avalanche Tested

■ SYMBOL

2.Drain

1.Gate

3.Source

■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
12N50L-TA3-T	12N50G-TA3-T	TO-220	G	D	S	Tube
12N50L-TF1-T	12N50G-TF1-T	TO-220F1	G	D	S	Tube
12N50L-TQ2-T	12N50G-TQ2-T	TO-263	G	D	S	Tube
12N50L-TQ2-R	12N50G-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate   D: Drain   S: Source

12N50L-TA3-T

    (1)Packing Type

    (2)Package Type

    (3)Lead Free

(1) T: Tube, R: Tape Reel

(2) TA3: TO-220 ,TF1: TO-220F1, TQ2: TO-263

(3) G: Halogen Free, L: Lead Free

12N50

■ **ABSOLUTE MAXIMUM RATINGS** (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current	Continuous (T_C=25°C)	I_D	12 (Note 2)	A
	Pulsed (Note 3)	I_{DM}	48 (Note 2)	A
Avalanche Current (Note 3)		I_{AR}	12	A
Avalanche Energy	Single Pulsed (Note 4)	E_{AS}	684	mJ
	Repetitive (Note 5)	E_{AR}	19.5	mJ
Peak Diode Recovery dv/dt (Note 5)		dv/dt	4.5	V/ns
Power Dissipation	TO-220/ TO-263	P_D	192	W
(T_C=25°C)	TO-220F1		42	
Derate above 25°C	TO-220/ TO-263		1.53	W/°C
	TO-220F1		0.33	
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55~+150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Drain current limited by maximum junction temperature
3. Repetitive Rating: Pulse width limited by maximum junction temperature
4. L =9.5mH, I_{AS} = 12A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
5. I_{SD} ≤ 12A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	°C/W
Junction to Case	TO-220/ TO-263	θ_{JC}	0.65	°C/W
	TO-220F1		3.0	

Preliminary   *Power MOSFET*

■ **ELECTRICAL CHARACTERISTICS** (T_C=25°C, unless otherwise specified)

| PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250µA, V_{GS}=0V	500			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=500V, V_{GS}=0V			10	µA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+30V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-30V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250µA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=6A		0.42	0.54	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}			1450	1930	pF
Output Capacitance		C_{OSS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		198	265	pF
Reverse Transfer Capacitance		C_{RSS}			14.5	22	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{GS}=10V, V_{DS}=400V, I_D=12A		30	39	nC
Gate to Source Charge		Q_{GS}	(Note 1, 2)		8		nC
Gate to Drain Charge		Q_{GD}			12		nC
Turn-ON Delay Time		$t_{D(ON)}$			28	65	ns
Rise Time		t_R	V_{DD}=250V, I_D=12A, R_G=25Ω		54	120	ns
Turn-OFF Delay Time		$t_{D(OFF)}$	(Note 1, 2)		75	160	ns
Fall-Time		t_F			47	105	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				12	A
Maximum Body-Diode Pulsed Current		I_{SM}				48	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S=12A, V_{GS}=0V			1.5	V
Body Diode Reverse Recovery Time		t_{rr}	I_S=12A, V_{GS}=0V, dI_F/dt=100A/µs		154		ns
Body Diode Reverse Recovery Charge		Q_{RR}	(Note 1)		0.45		µC

Note: 1. Pulse Test: Pulse width ≤ 300µs, Duty cycle ≤ 2%
         2. Essentially independent of operating temperature
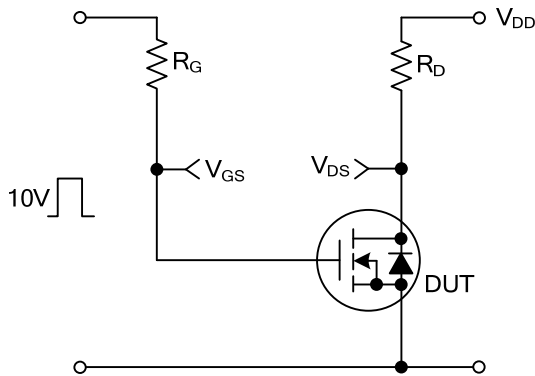
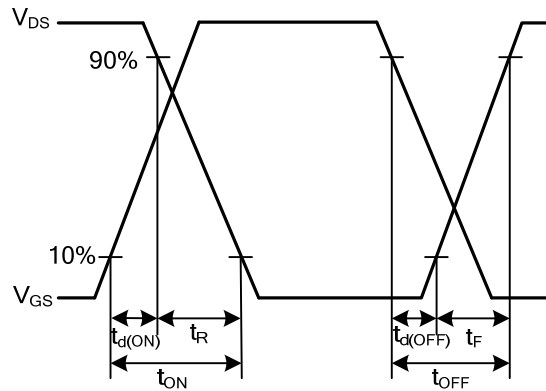## ■ TEST CIRCUITS AND WAVEFORMS

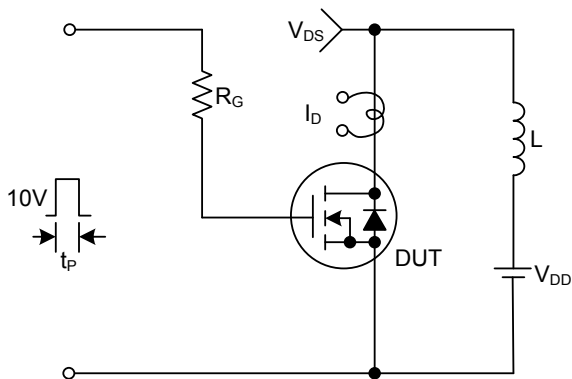Gate Charge Test Circuit
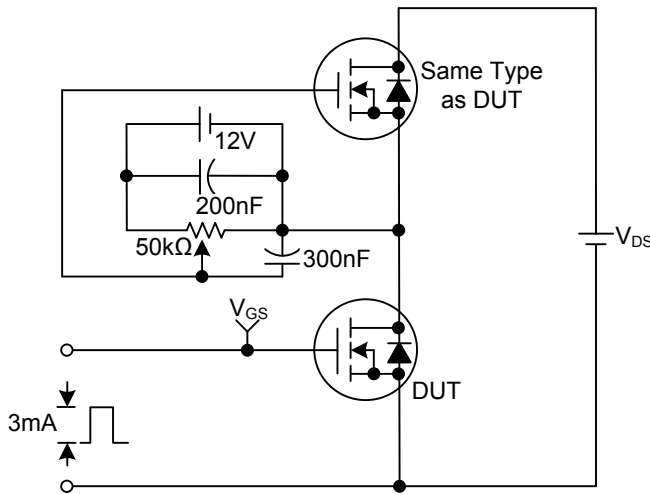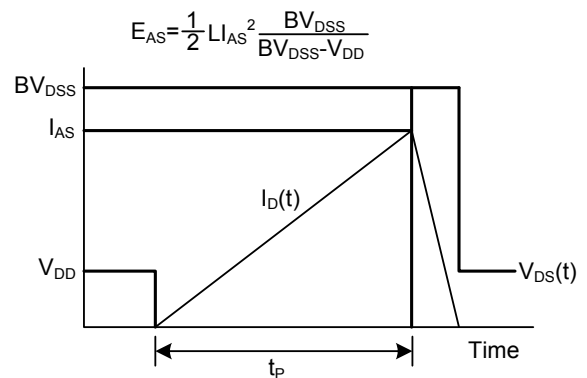
Gate Charge Waveforms
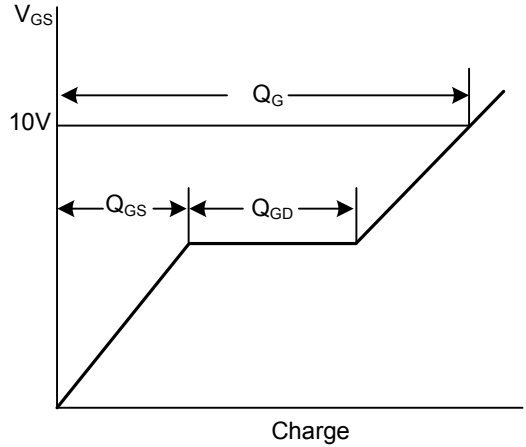
Resistive Switching Test Circuit

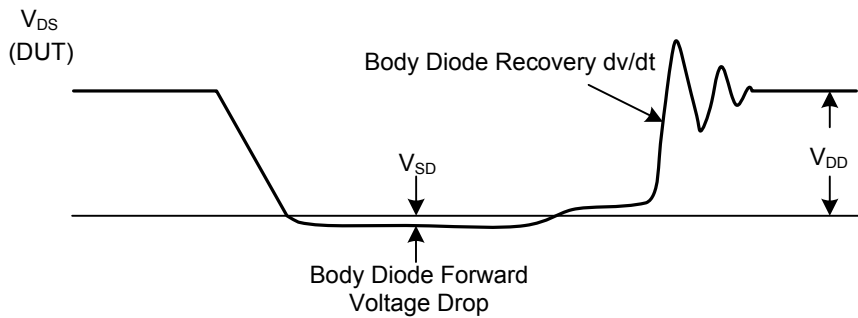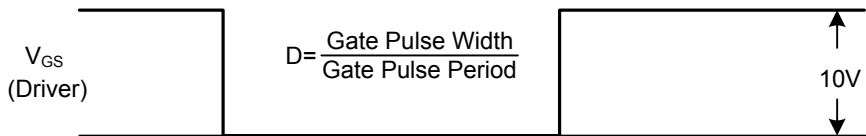Resistive Switching Waveforms
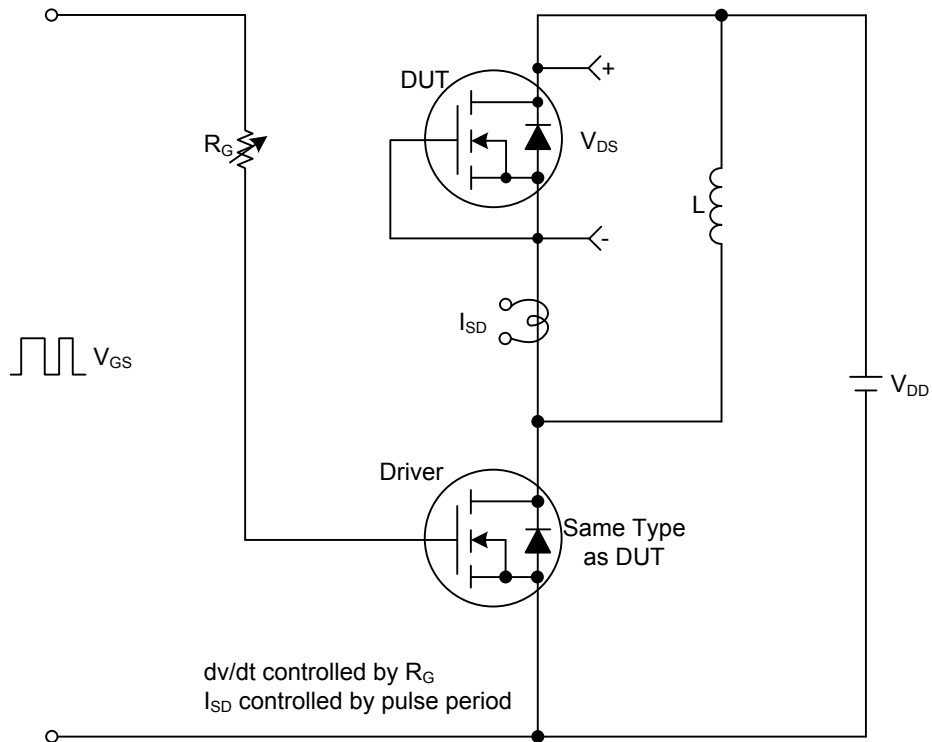
Unclamped Inductive Switching Test Circuit

Unclamped Inductive Switching Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

■ **TEST CIRCUITS AND WAVEFORMS(Cont.)**

Peak Diode Recovery dv/dt Test Circuit & Waveforms

$D = \dfrac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$

dv/dt controlled by R_G
I_{SD} controlled by pulse period

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www.unisonic.com.tw

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