



# TS1871-TS1872-TS1874

1.8V input/output rail-to-rail  
low power operational amplifiers

## Features

- Operating range from  $V_{CC} = 1.8V$  to  $6V$
- Rail-to-rail input and output
- Extended  $V_{icm}$  ( $V_{DD} - 0.2V$  to  $V_{CC} + 0.2V$ )
- Low supply current ( $400\mu A$ )
- Gain bandwidth product ( $1.6MHz$ )
- High unity gain stability
- ESD tolerance ( $2kV$ )
- Latch-up immunity
- Available in SOT23-5 micro package

## Applications

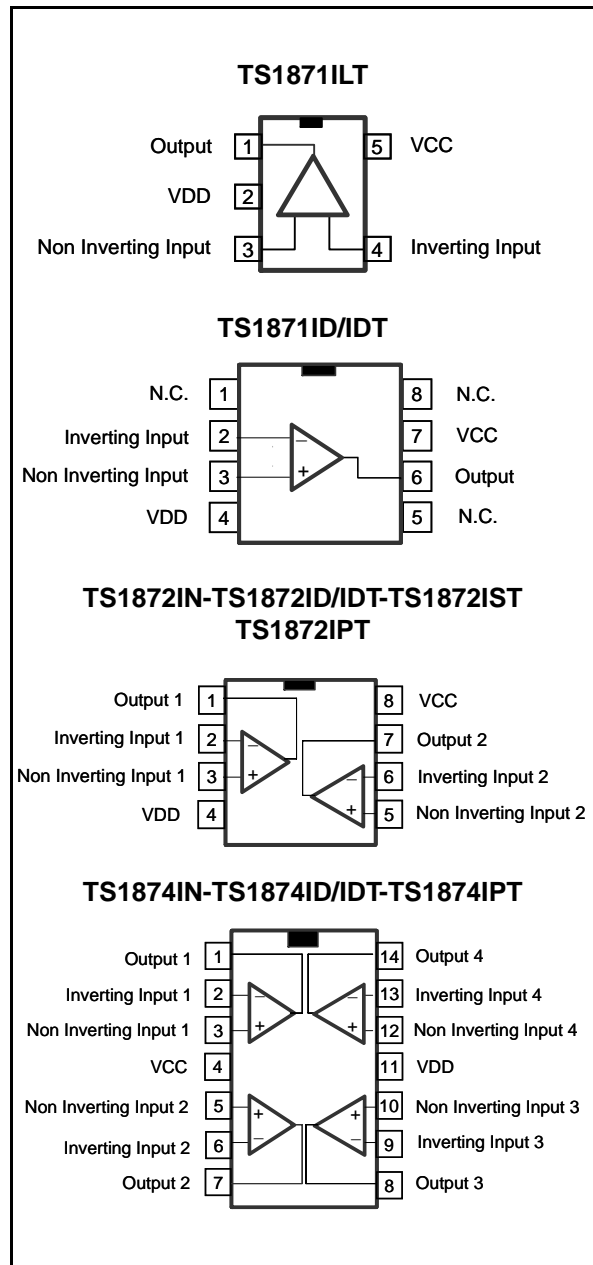
- Battery-powered applications (toys)
- Portable communication devices (cell phones)
- Audio driver (headphone drivers)
- Laptop/notebook computers

## Description

The TS187x (single, dual and quad) is an operational amplifier family able to operate with voltages as low as  $1.8V$  and that features both input and output rail-to-rail.

The common mode input voltage extends  $200mV$  beyond the supply voltages at  $25^{\circ}C$  while the output voltage swing is within  $100mV$  of each rail with a  $600\Omega$  load resistor. This device consumes typically  $400\mu A$  per channel while offering  $1.6MHz$  of gain-bandwidth product. The amplifier provides high output drive capability typically at  $65mA$  load.

These features make the TS187x family ideal for sensor interface, battery-supplied and portable applications.



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# 1 Absolute maximum ratings and operating conditions

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	7	V
$V_{id}$	Differential input voltage <sup>(2)</sup>	$\pm 1$	V
$V_{in}$	Input voltage	$V_{DD} - 0.3$ to $V_{CC} + 0.3$	V
$T_{stg}$	Storage temperature	-65 to +150	°C
$T_j$	Maximum junction temperature	150	°C
$R_{thja}$	Thermal resistance junction to ambient <sup>(3)</sup>		°C/W
	SOT23-5	250	
	DIP8	85	
	DIP14	66	
	MiniSO-8	190	
	SO-8	125	
	SO-14	103	
	TSSOP8 TSSOP14	120 100	
$R_{thjc}$	Thermal resistance junction to case		°C/W
	SOT23-5	81	
	DIP8	41	
	DIP14	33	
	MiniSO-8	39	
	SO-8	40	
	SO-14	31	
	TSSOP8 TSSOP14	37 32	
ESD	HBM: human body model <sup>(4)</sup>	2	kV
	MM: machine model <sup>(5)</sup>	200	V
	CDM: charged device model <sup>(6)</sup>	1.5	kV
	Latch-up immunity	200	mA
	Lead temperature (soldering, 10 sec)	250	°C
	Output short-circuit duration	see note <sup>(7)</sup>	

- All voltage values, except differential voltage are with respect to network terminal.
- Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. If  $V_{id} > \pm 1V$ , the maximum input current must not exceed  $\pm 1mA$ . When  $V_{id} > \pm 1V$ , add an input series resistor to limit input current.
- Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
- Human body model: A 100pF capacitor is charged to the specified voltage, then discharged through a 1.5k $\Omega$  resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
- Machine model: A 200pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 $\Omega$ ). This is done for all couples of connected pin combinations while the other pins are floating.
- Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.
- Short-circuits from the output to  $V_{CC}$  can cause excessive heating. The maximum output current is approximately 80mA, independent of the magnitude of  $V_{CC}$ . Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	1.8 to 6	V
$V_{icm}$	Common mode input voltage range $T_{oper} = 25^{\circ}\text{C}$ , $1.8 \leq V_{CC} \leq 6\text{V}$ $T_{min} < T_{oper} < T_{max}$ , $1.8 \leq V_{CC} \leq 6\text{V}$	$V_{DD} - 0.2$ to $V_{CC} + 0.2$ $V_{DD}$ to $V_{CC}$	V
$T_{oper}$	Operating free air temperature range	-40 to + 125	$^{\circ}\text{C}$

## 2 Electrical characteristics

**Table 3. Electrical characteristics at  $V_{CC} = +1.8V$   
with  $V_{DD} = 0V$ ,  $C_L$  &  $R_L$  connected to  $V_{CC}/2$ , and  $T_{amb} = 25^\circ C$  (unless otherwise specified)<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage	$V_{icm} = V_{out} = V_{CC}/2$ TS1871A/2A/4A $T_{min} \leq T_{amb} \leq T_{max}$ TS1871/2/4 $T_{min} \leq T_{amb} \leq T_{max}$		0.1	1 1.5 3 6	mV
$\Delta V_{io}$	Input offset voltage drift			2		$\mu V/^\circ C$
$I_{io}$	Input offset current	$V_{icm} = V_{out} = V_{CC}/2$ <sup>(2)</sup> $T_{min} \leq T_{amb} \leq T_{max}$		3	30 60	nA
$I_{ib}$	Input bias current	$V_{icm} = V_{out} = V_{CC}/2$ <sup>(1)</sup> $T_{min} \leq T_{amb} \leq T_{max}$		40	125 150	nA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0 \leq V_{icm} \leq V_{CC}$ , $V_{out} = V_{CC}/2$ $T_{min} \leq T_{amb} \leq T_{max}$	55 52	77		dB
$A_{vd}$	Large signal voltage gain	<b><math>V_{out} = 0.5V</math> to <math>1.3V</math></b> $R_L = 2k\Omega$ $R_L = 600\Omega$	77 70	92 85		dB
$V_{OH}$	High level output voltage	<b><math>V_{id} = 100mV</math></b> $R_L = 2k\Omega$ $R_L = 600\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 600\Omega$	1.65 1.62 1.65 1.62	1.77 1.74		V
$V_{OL}$	Low level output voltage	<b><math>V_{id} = -100mV</math></b> $R_L = 2k\Omega$ $R_L = 600\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 600\Omega$		88 115	100 150 100 150	mV
$I_o$	Output source current	$V_{id} = 100mV$ , $V_O = V_{DD}$	20	65		mA
	Output sink current	$V_{id} = -100mV$ , $V_O = V_{CC}$	20	65		
$I_{CC}$	Supply current (per amplifier)	<b><math>V_{out} = V_{CC}/2</math></b> $A_{VCL} = 1$ , no load $T_{min} \leq T_{amb} \leq T_{max}$		400	560 600	$\mu A$
GBP	Gain bandwidth product	$R_L = 10k\Omega$ , $C_L = 100pF$ , $f = 100kHz$	0.9	1.6		MHz
SR	Slew rate	$R_L = 10k\Omega$ , $C_L = 100pF$ , $A_V = 1$	0.38	0.54		$V/\mu s$
$\phi_m$	Phase margin	$C_L = 100pF$		53		Degrees
en	Input voltage noise	$f = 1kHz$		27		$nV/\sqrt{Hz}$
THD	Total harmonic distortion			0.01		%

1. All parameter limits at temperatures different from  $25^\circ C$  are guaranteed by correlation.

2. Maximum values include unavoidable inaccuracies of the industrial tests.

**Table 4. Electrical characteristics at  $V_{CC} = +3V$   
with  $V_{DD} = 0V$ ,  $C_L$  &  $R_L$  connected to  $V_{CC}/2$ , and  $T_{amb} = 25^\circ C$  (unless otherwise specified)<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage	$V_{icm} = V_{out} = V_{CC}/2$ TS1871A/2A/4A $T_{min} \leq T_{amb} \leq T_{max}$ TS1871/2/4 $T_{min} \leq T_{amb} \leq T_{max}$		0.1	1 1.5 3 6	mV
$\Delta V_{io}$	Input offset voltage drift			2		$\mu V/^\circ C$
$I_{io}$	Input offset current	$V_{icm} = V_{out} = V_{CC}/2$ <sup>(2)</sup> $T_{min} \leq T_{amb} \leq T_{max}$		3	30 60	nA
$I_{ib}$	Input bias current	$V_{icm} = V_{out} = V_{CC}/2$ <sup>(1)</sup> $T_{min} \leq T_{amb} \leq T_{max}$		4	125 150	nA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0 \leq V_{icm} \leq V_{CC}$ , $V_{out} = V_{CC}/2$ $T_{min} \leq T_{amb} \leq T_{max}$	60 57	80		dB
$A_{vd}$	Large signal voltage gain	<b><math>V_{out} = 0.5V</math> to <math>2.5V</math></b> $R_L = 2k\Omega$ $R_L = 600\Omega$	80 74	92 95		dB
$V_{OH}$	High level output voltage	<b><math>V_{id} = 100mV</math></b> $R_L = 2k\Omega$ $R_L = 600\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 600\Omega$	2.82 2.80 2.82 2.80	2.95 2.95		V
$V_{OL}$	Low level output voltage	<b><math>V_{id} = -100mV</math></b> $R_L = 2k\Omega$ $R_L = 600\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 600\Omega$		88 115	120 160 120 160	mV
$I_o$	Output source current	$V_{id} = 100mV$ , $V_O = V_{DD}$	20	80		mA
	Output sink current	$V_{id} = -100mV$ , $V_O = V_{CC}$	20	80		
$I_{CC}$	Supply current (per amplifier)	<b><math>V_{out} = V_{CC}/2</math></b> $A_{VCL} = 1$ , no load $T_{min} \leq T_{amb} \leq T_{max}$		450	650 690	$\mu A$
GBP	Gain bandwidth product	$R_L = 10k\Omega$ , $C_L = 100pF$ , $f = 100kHz$	1	1.7		MHz
SR	Slew rate	$R_L = 10k\Omega$ , $C_L = 100pF$ , $A_V = 1$	0.42	0.6		V/ $\mu s$
$\phi_m$	Phase margin	$C_L = 100pF$		53		Degrees
en	Input voltage noise	$f = 1kHz$		27		nV/ $\sqrt{Hz}$
THD	Total harmonic distortion			0.01		%

1. All parameter limits at temperatures different from  $25^\circ C$  are guaranteed by correlation.
2. Maximum values include unavoidable inaccuracies of the industrial tests.

**Table 5. Electrical characteristics at  $V_{CC} = +5V$  with  $V_{DD} = 0V$ ,  $C_L$  &  $R_L$  connected to  $V_{CC}/2$ , and  $T_{amb} = 25^\circ C$  (unless otherwise specified) <sup>(1)</sup>**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage	$V_{icm} = V_{out} = V_{CC}/2$ TS1871A/2A/4A $T_{min} \leq T_{amb} \leq T_{max}$ TS1871/2/4 $T_{min} \leq T_{amb} \leq T_{max}$		0.1	1 1.5 3 6	mV
$\Delta V_{io}$	Input offset voltage drift			2		$\mu V/^\circ C$
$I_{io}$	Input offset current	$V_{icm} = V_{out} = V_{CC}/2$ <sup>(2)</sup> $T_{min} \leq T_{amb} \leq T_{max}$		3	30 60	nA
$I_{ib}$	Input bias current	$V_{icm} = V_{out} = V_{CC}/2$ <sup>(1)</sup> $T_{min} \leq T_{amb} \leq T_{max}$		70	130 150	nA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0 \leq V_{icm} \leq V_{CC}$ , $V_{out}$ not equal to $V_{CC}/2$ $T_{min} \leq T_{amb} \leq T_{max}$	65 62	85		dB
SVR	Supply voltage rejection ratio $20 \log (\Delta V_{cc}/\Delta V_{io})$	$V_{CC} = 1.8$ to $5V$	70	90		dB
$A_{vd}$	Large signal voltage gain	<b><math>V_{out} = 1V</math> to <math>4V</math></b> $R_L = 2k\Omega$ $R_L = 600\Omega$	83 77	92 85		dB
$V_{OH}$	High level output voltage	<b><math>V_{id} = 100mV</math></b> $R_L = 2k\Omega$ $R_L = 600\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 600\Omega$	4.80 4.75 4.80 4.75	4.95 4.90		V
$V_{OL}$	Low level output voltage	<b><math>V_{id} = -100mV</math></b> $R_L = 2k\Omega$ $R_L = 600\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ , $R_L = 600\Omega$		88 115	130 188 130 188	mV
$I_o$	Output source current	$V_{id} = 100mV$ , $V_O = V_{DD}$	20	80		mA
	Output sink current	$V_{id} = -100mV$ , $V_O = V_{CC}$	20	80		
$I_{CC}$	Supply current (per amplifier)	<b><math>V_{out} = V_{CC}/2</math></b> $A_{VCL} = 1$ , no load $T_{min} \leq T_{amb} \leq T_{max}$		500	835 875	$\mu A$
GBP	Gain bandwidth product	$R_L = 10k\Omega$ , $C_L = 100pF$ , $f = 100kHz$	1	1.8		MHz
SR	Slew rate	$R_L = 10k\Omega$ , $C_L = 100pF$ , $A_V = 1$	0.42	0.6		V/ $\mu s$
$\phi_m$	Phase margin	$C_L = 100pF$		55		Degrees
en	Input voltage noise	$f = 1kHz$		27		nV/ $\sqrt{Hz}$
THD	Total harmonic distortion			0.01		%

1. All parameter limits at temperatures different from 25°C are guaranteed by correlation.
2. Maximum values include unavoidable inaccuracies of the industrial tests.

Figure 1. Input offset voltage distribution

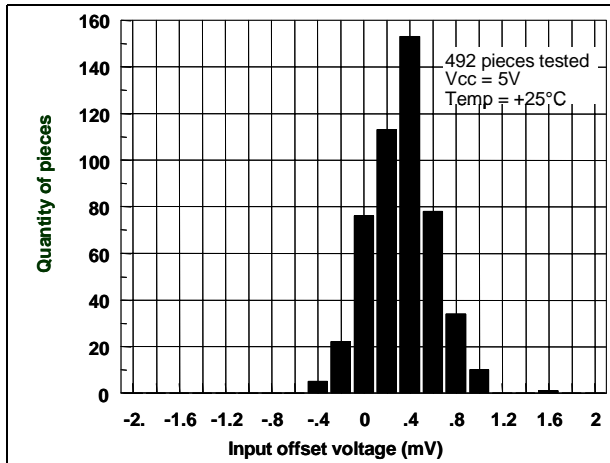


Figure 2. Input offset voltage vs. temperature

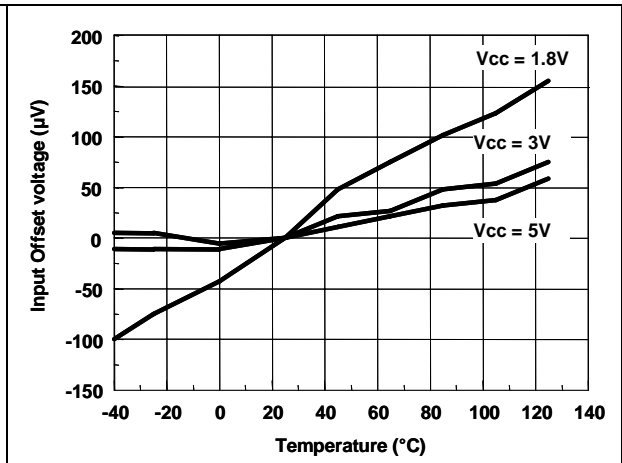


Figure 3. Input bias current vs. temperature

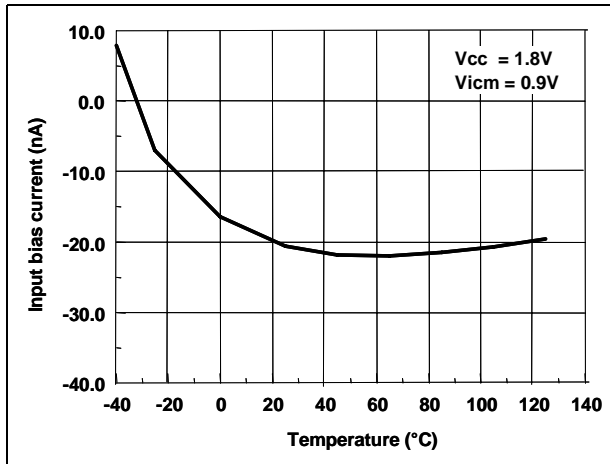


Figure 4. Input bias current vs. temperature

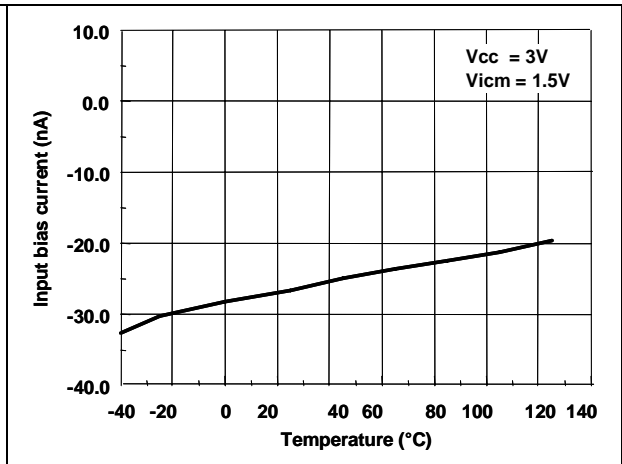


Figure 5. Supply current/amplifier vs. supply voltage

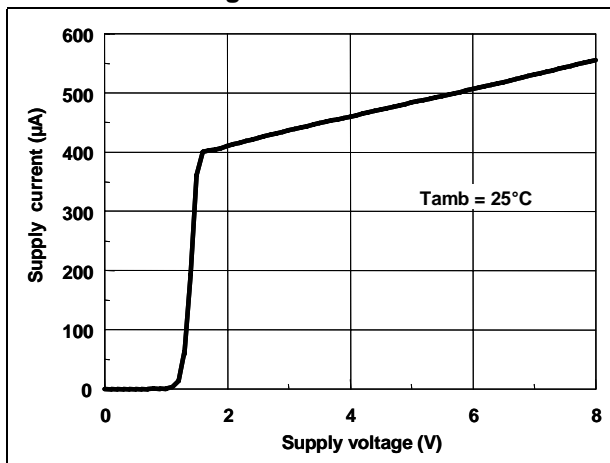


Figure 6. Supply current/amplifier vs. temperature

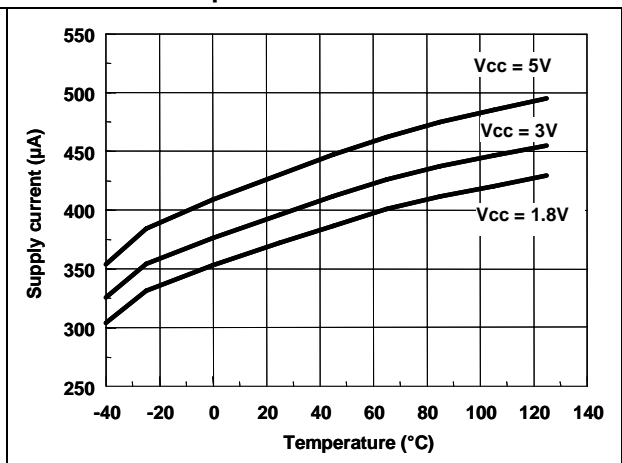




Figure 7. Common mode rejection vs. temperature

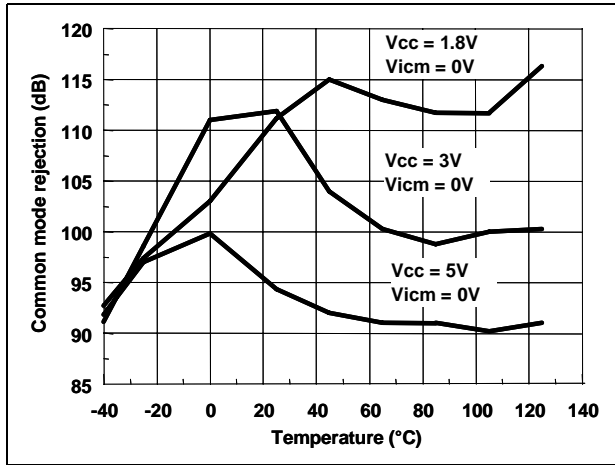


Figure 8. Supply voltage rejection vs. temperature

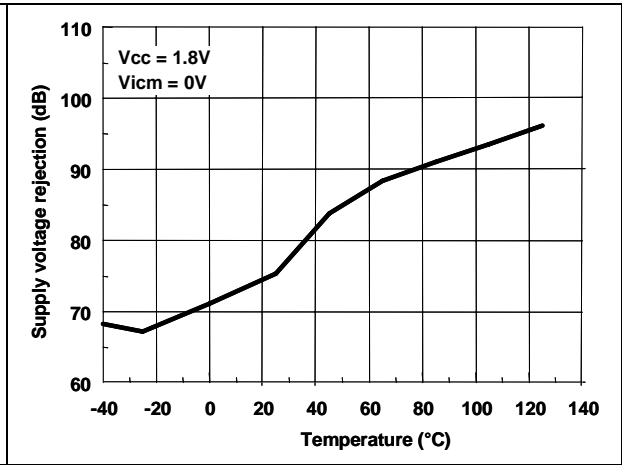


Figure 9. Supply voltage rejection vs. temperature

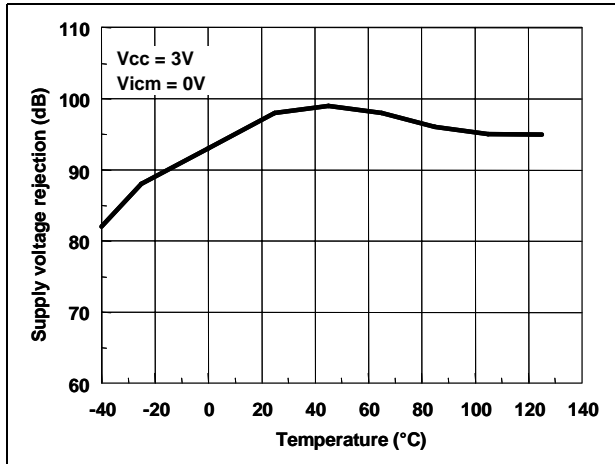


Figure 10. Supply voltage rejection vs. temperature

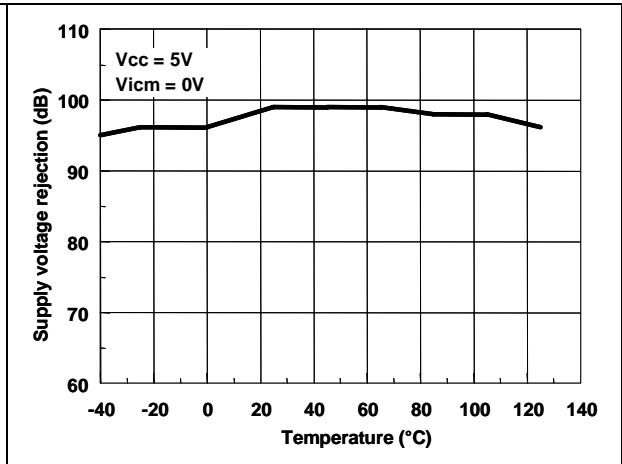


Figure 11. Power supply voltage rejection vs. frequency

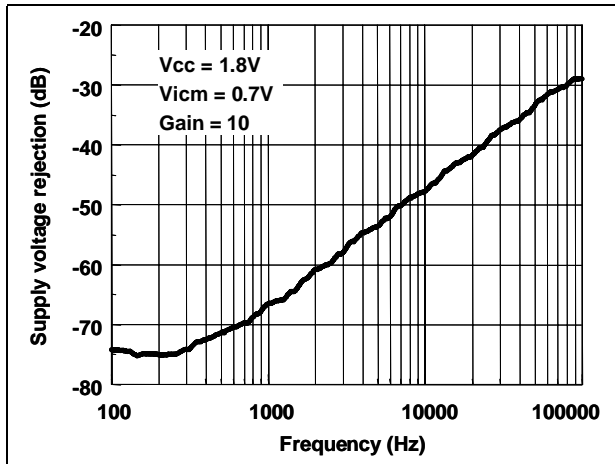


Figure 12. Open loop gain vs. frequency

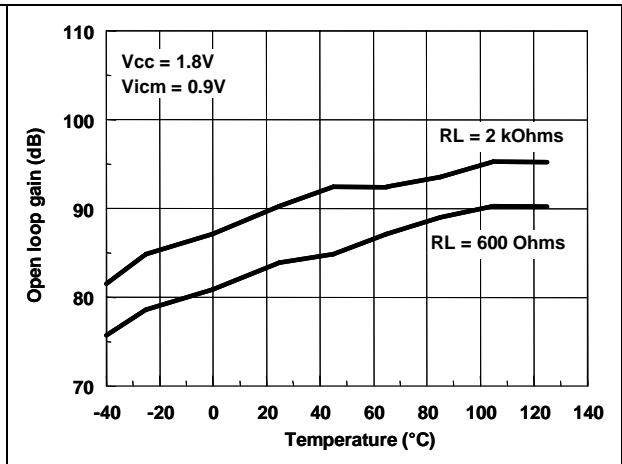


Figure 13. Open loop gain vs. temperature

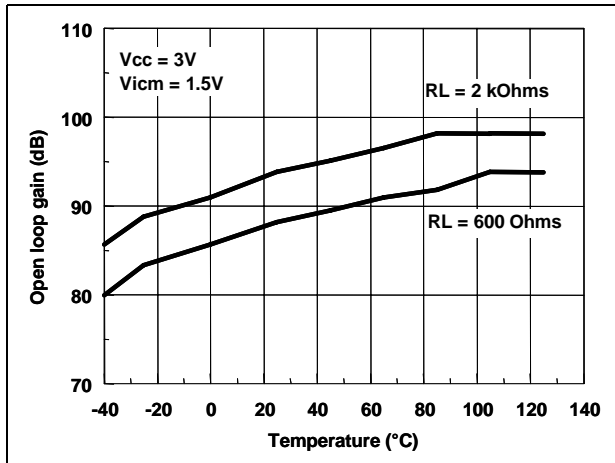


Figure 14. Open loop gain vs. temperature

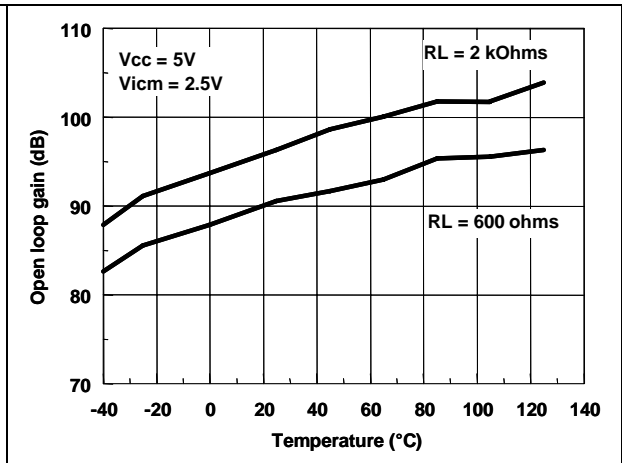


Figure 15. High level output voltage vs. temperature

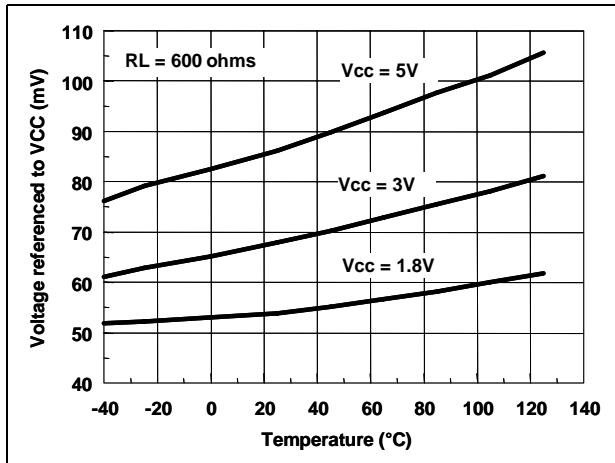


Figure 16. Low level output voltage vs. temperature

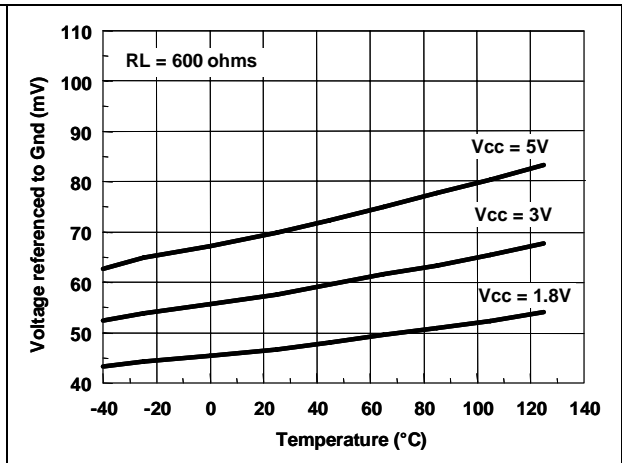


Figure 17. High level output voltage vs. temperature

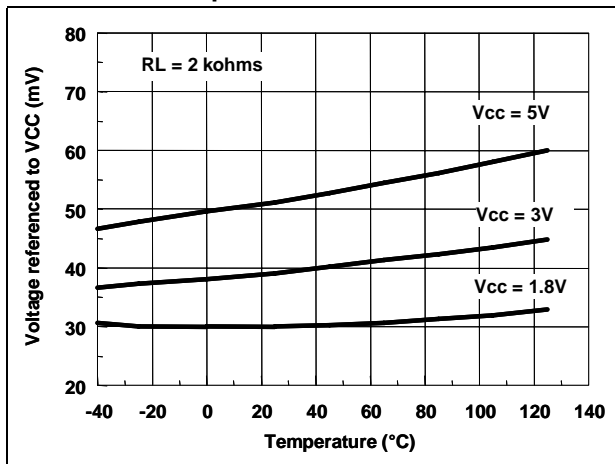


Figure 18. Low level output voltage vs. temperature

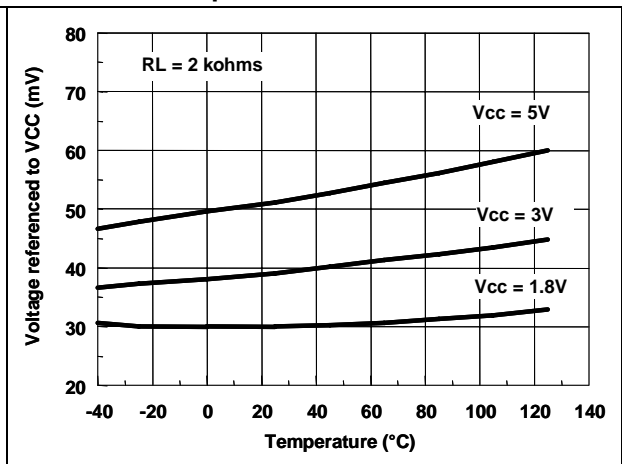


Figure 19. Output current vs. temperature

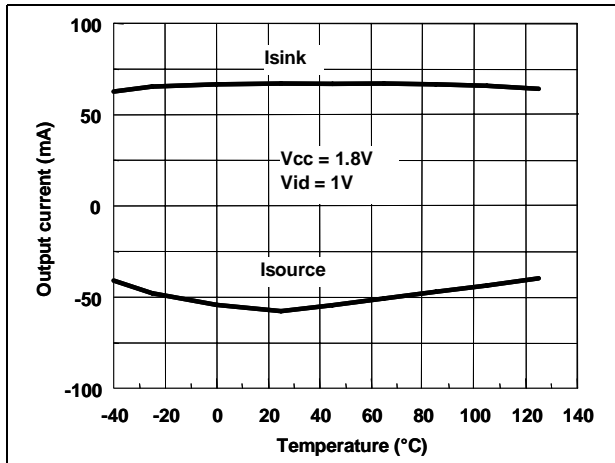


Figure 20. Output current vs. temperature

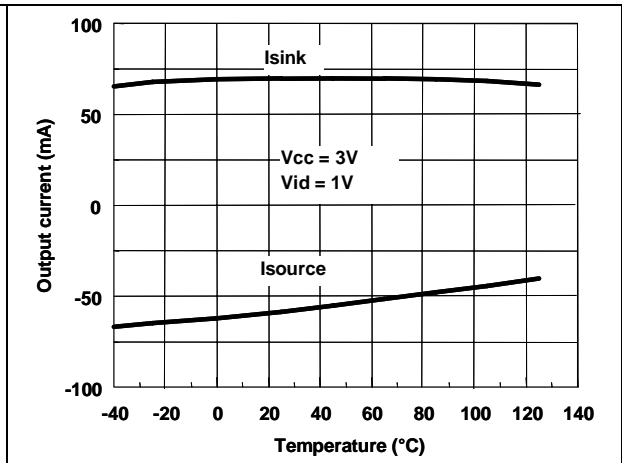


Figure 21. Output current vs. temperature

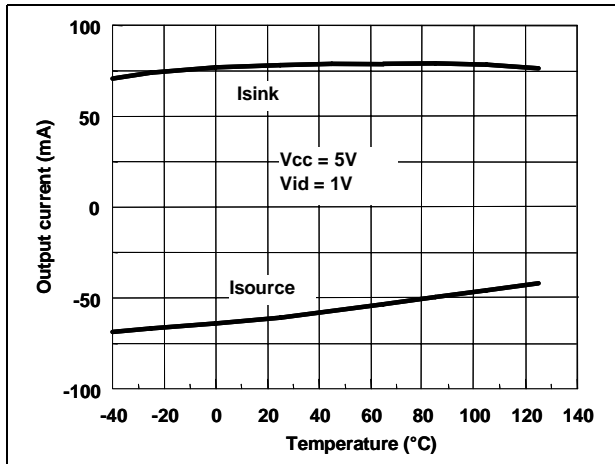


Figure 22. Output current vs. output voltage

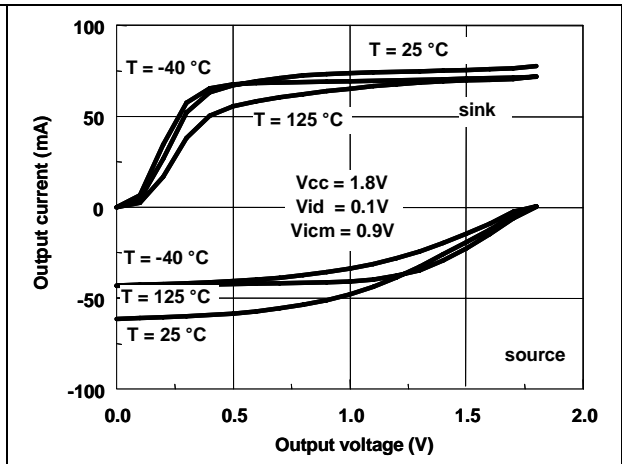


Figure 23. Output current vs. output voltage

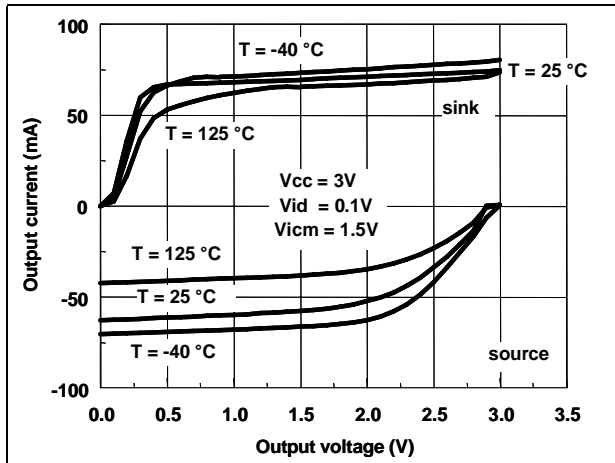


Figure 24. Output current vs. output voltage

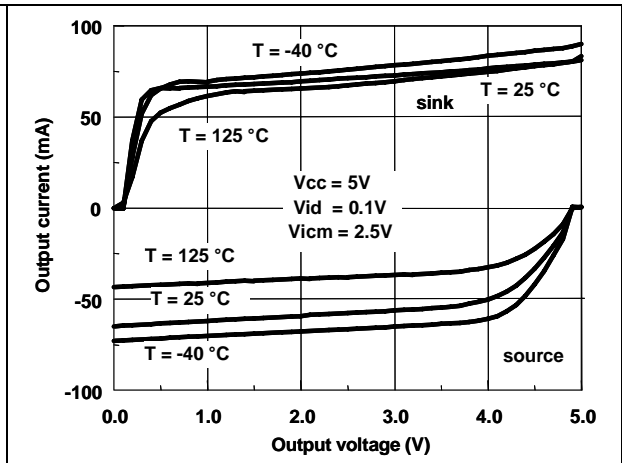


Figure 25. Gain and phase vs. frequency

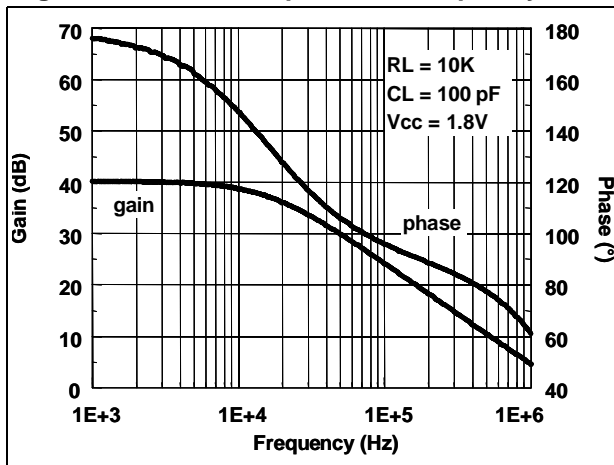


Figure 26. Gain and phase vs. frequency

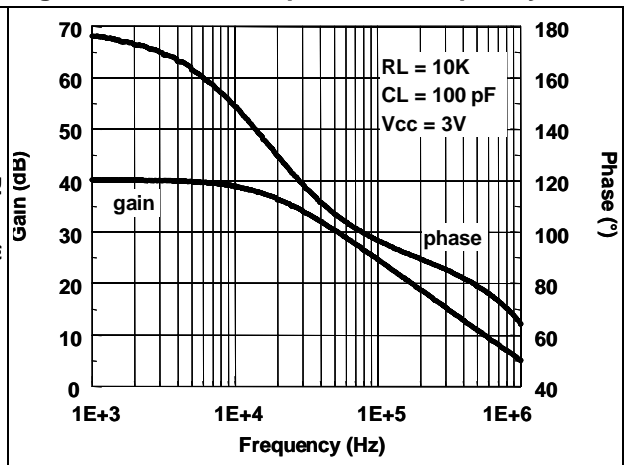


Figure 27. Gain and phase vs. frequency

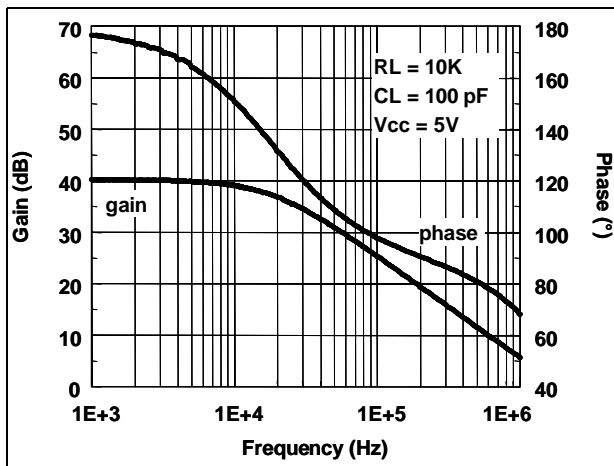


Figure 28. Gain bandwidth product vs. temperature

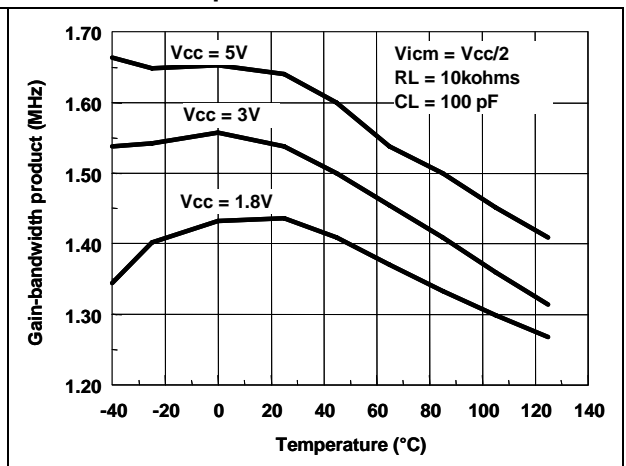


Figure 29. Gain bandwidth product vs. supply voltage

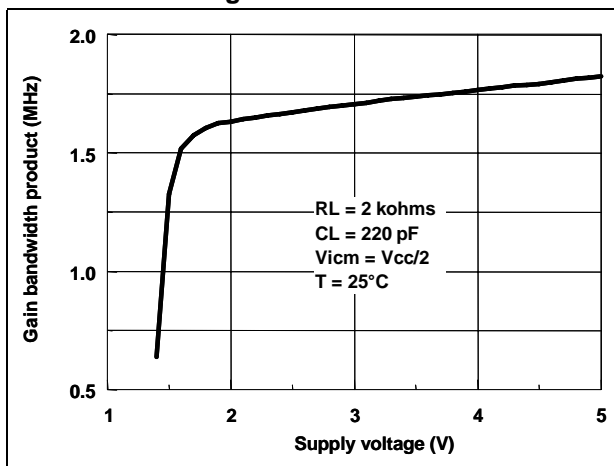


Figure 30. Slew rate vs. temperature

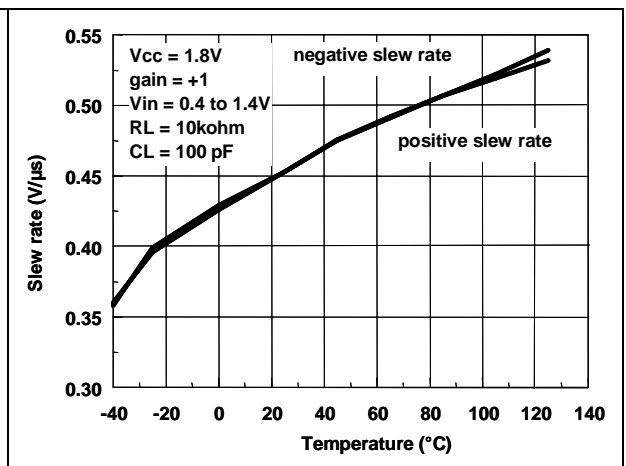


Figure 31. Slew rate vs. temperature

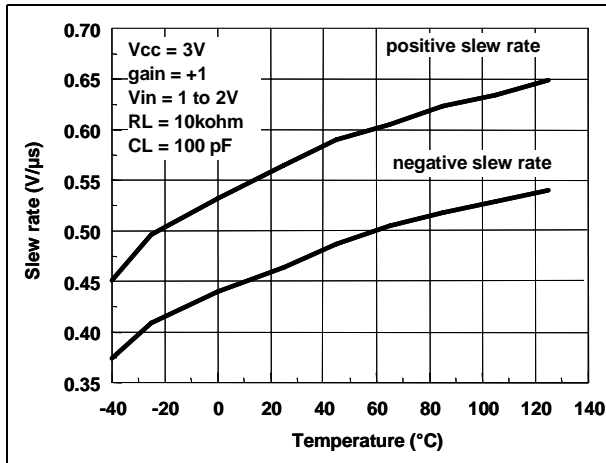


Figure 32. Slew rate vs. temperature

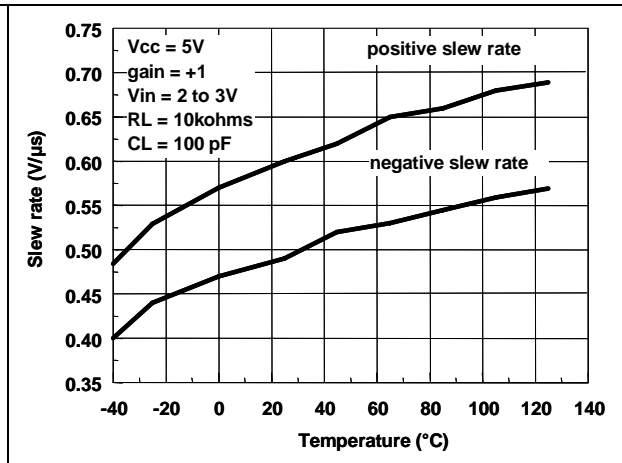


Figure 33. Phase margin vs. load capacitor

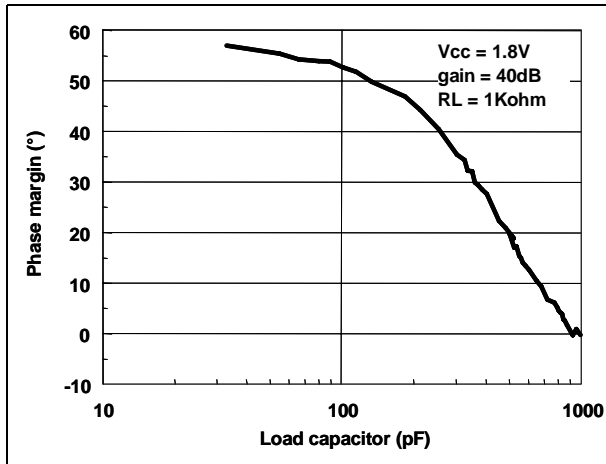


Figure 34. Phase margin vs. output current

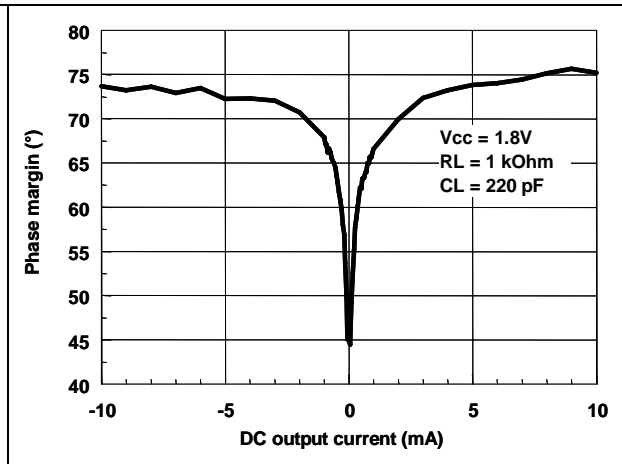


Figure 35. Gain margin vs. output current

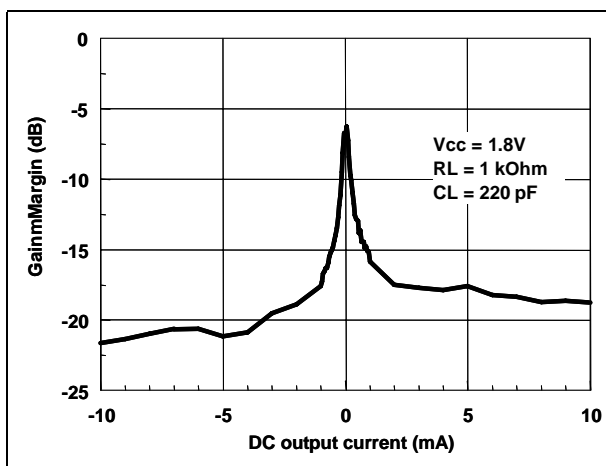


Figure 36. Equivalent input noise vs. frequency

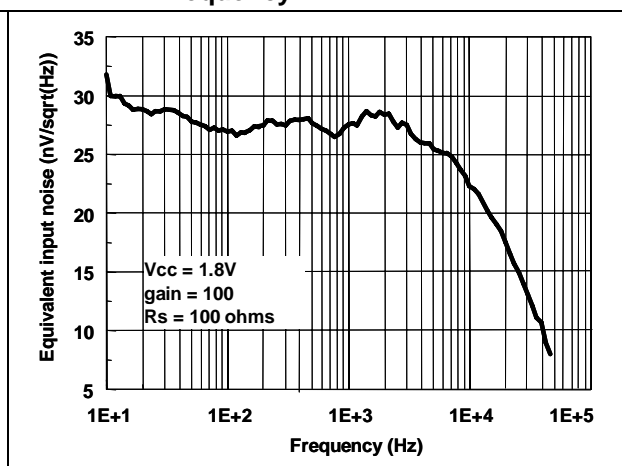


Figure 37. Distortion vs. output voltage

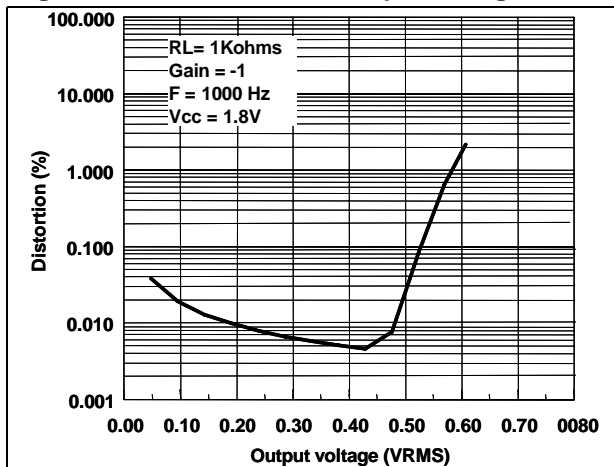


Figure 38. Distortion vs. output voltage

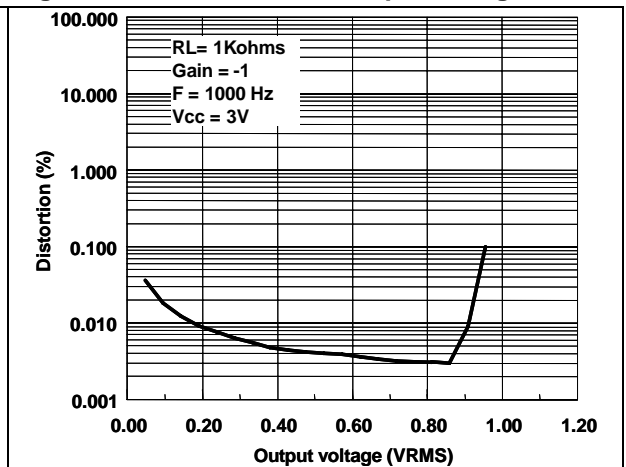


Figure 39. Distortion vs. output voltage

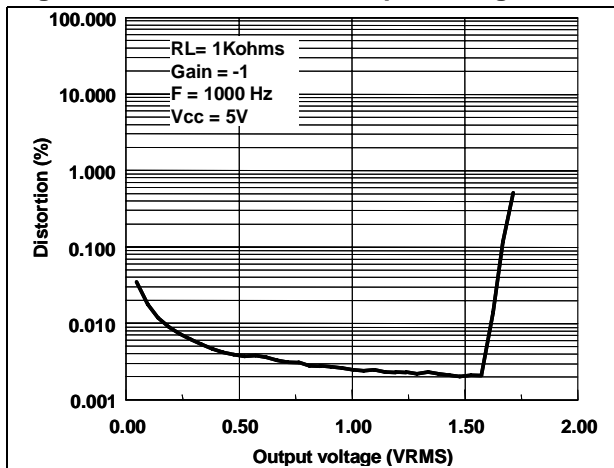


Figure 40. Distortion vs. output voltage

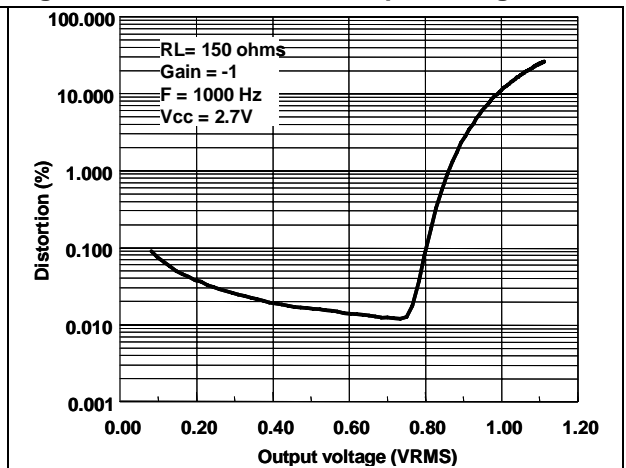


Figure 41. Distortion vs. output voltage

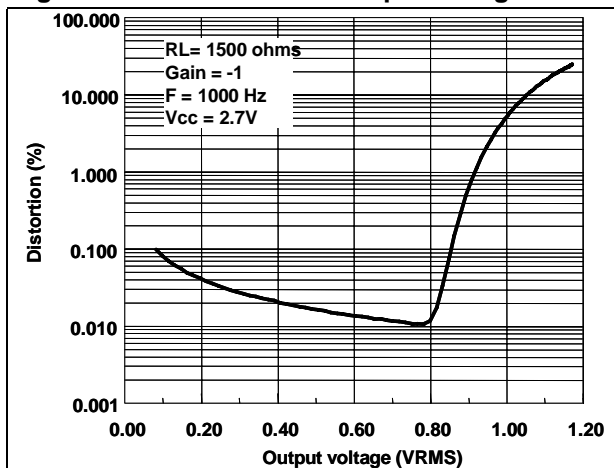


Figure 42. Distortion vs. output voltage

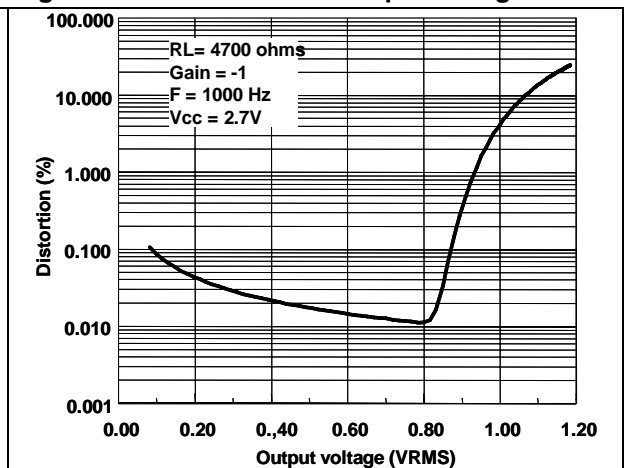


Figure 43. Distortion vs. frequency

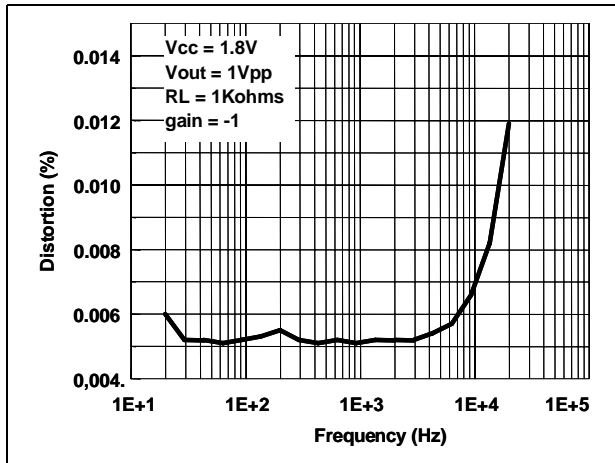


Figure 44. Distortion vs. frequency

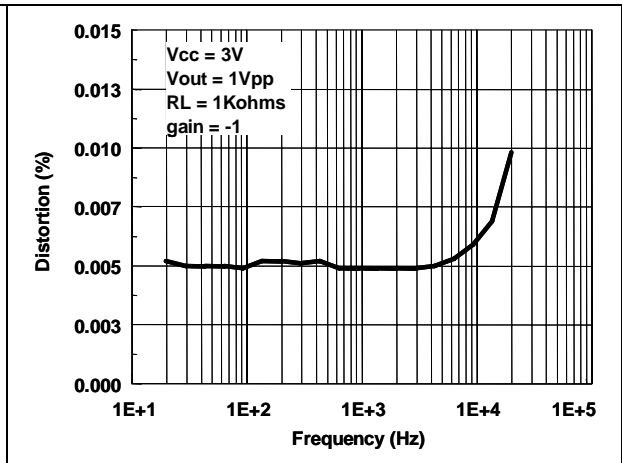


Figure 45. Distortion vs. frequency

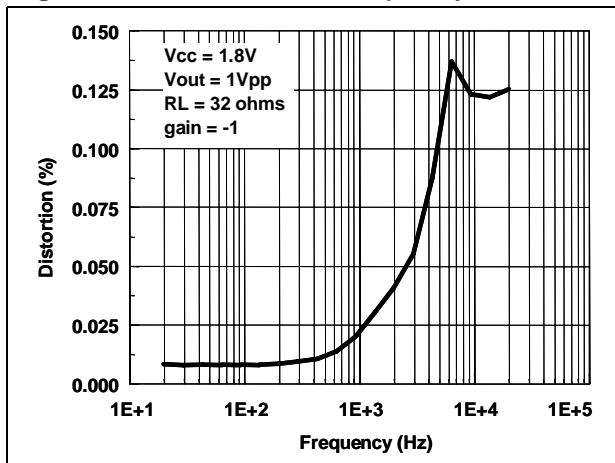


Figure 46. Distortion vs. frequency

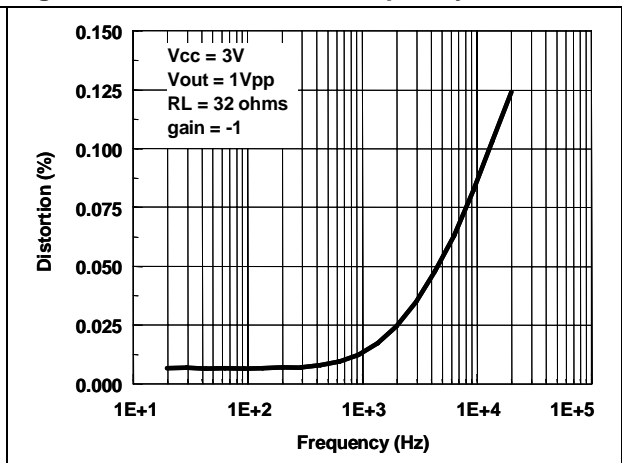
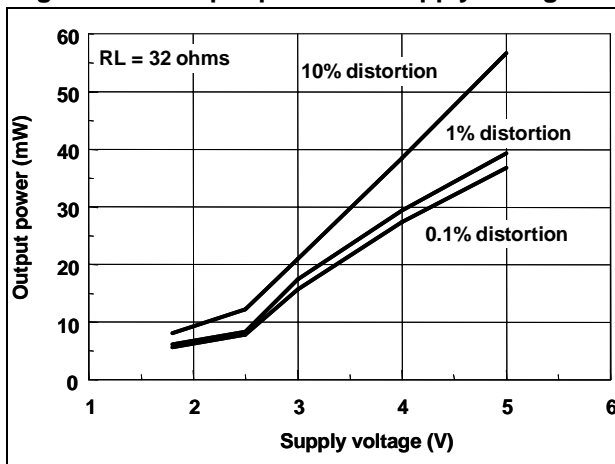


Figure 47. Output power vs. supply voltage



### 3 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

#### 3.1 SOT23-5 package information

Figure 48. SOT23-5 package mechanical drawing

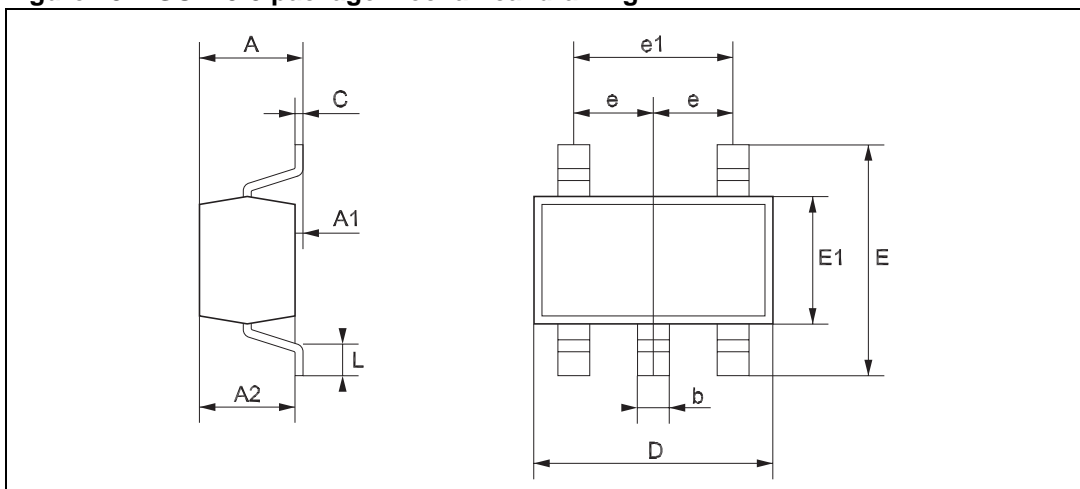


Table 6. SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.00		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6



### 3.2 DIP8 package information

Figure 49. DIP8 package mechanical drawing

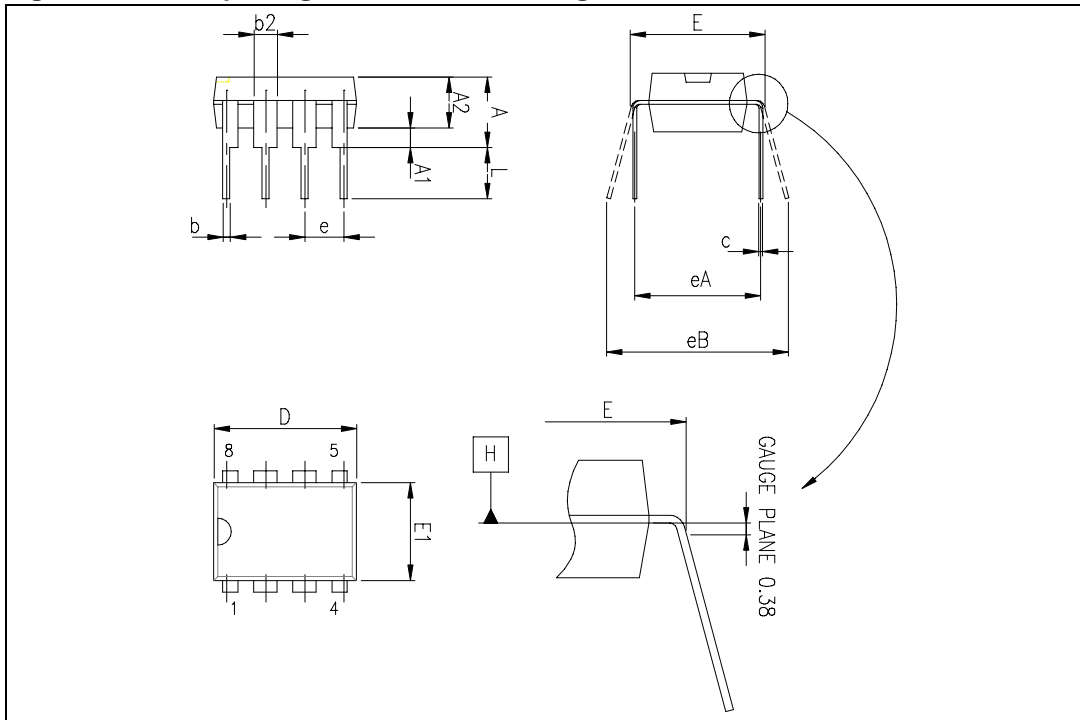


Table 7. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

### 3.3 SO-8 package information

Figure 50. SO-8 package mechanical drawing

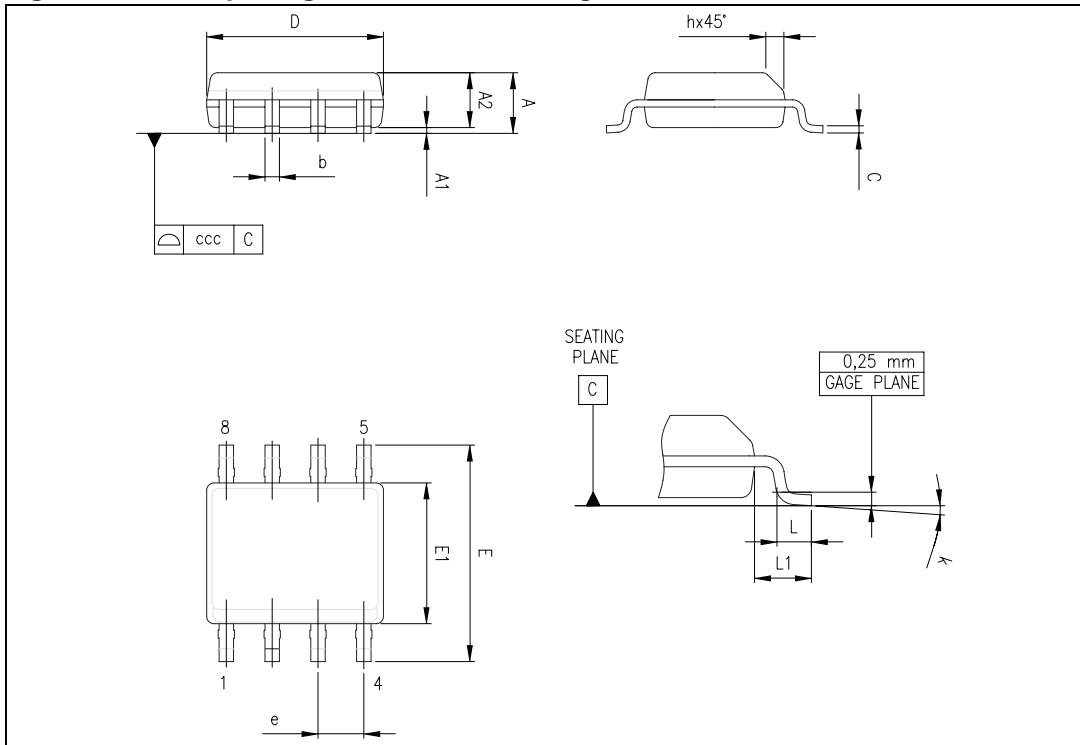


Table 8. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
H	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

### 3.4 TSSOP8 package information

Figure 51. TSSOP8 package mechanical drawing

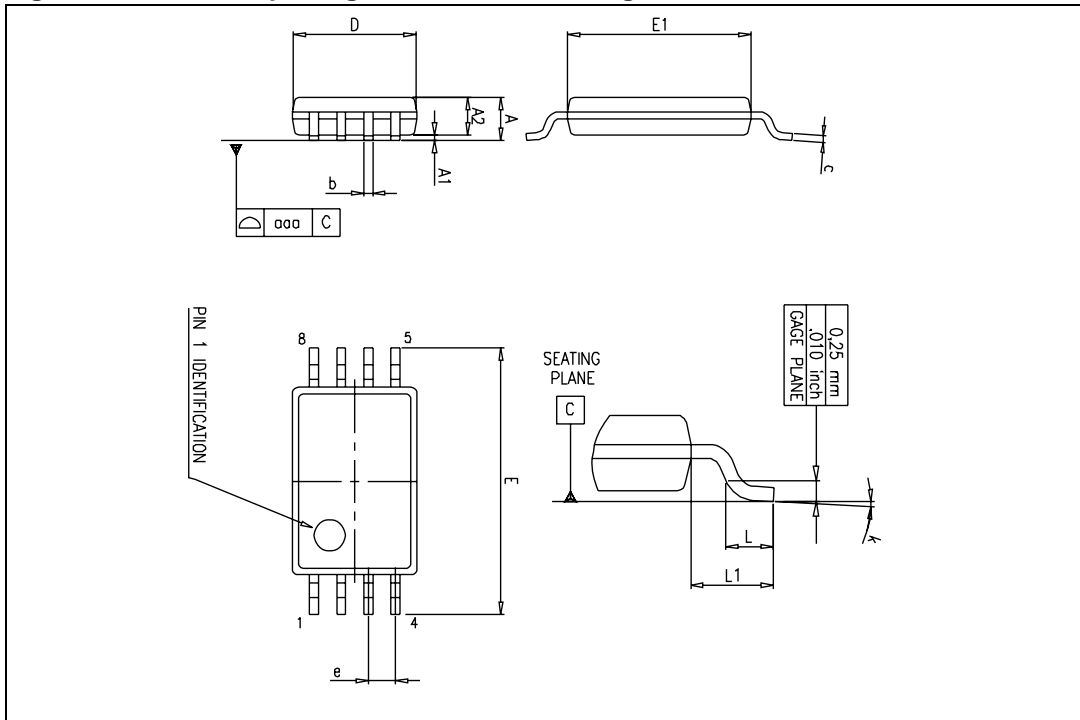


Table 9. TSSOP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.1			0.004	

### 3.5 MiniSO-8 package

Figure 52. MiniSO-8 package mechanical drawing

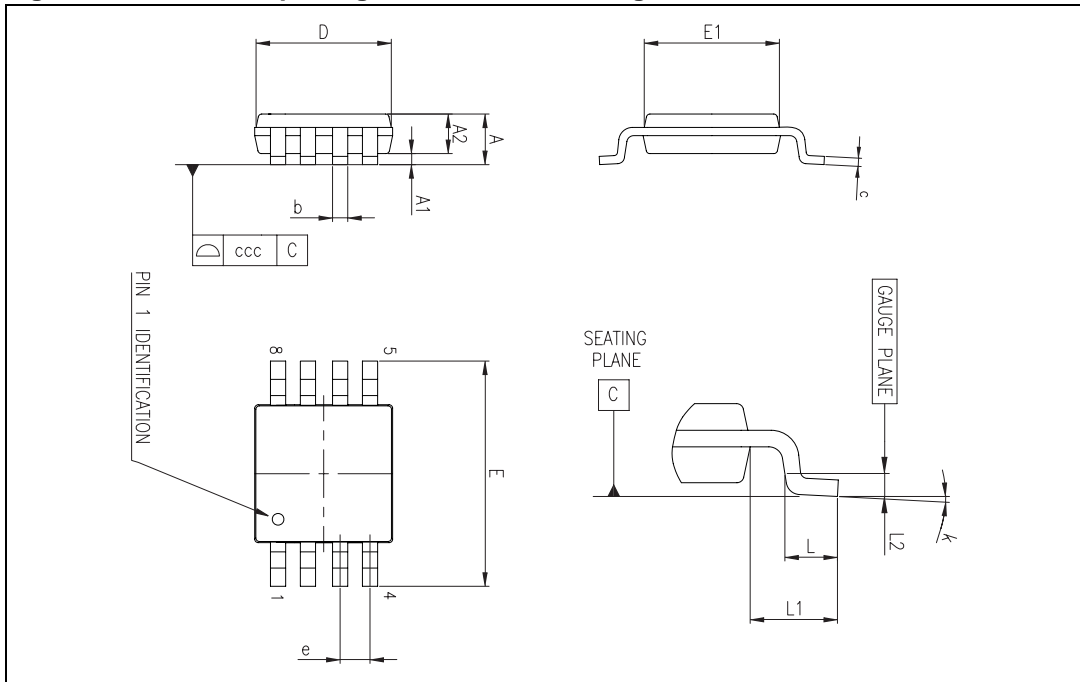


Table 10. MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

### 3.6 DIP14 package information

Figure 53. DIP14 package mechanical drawing

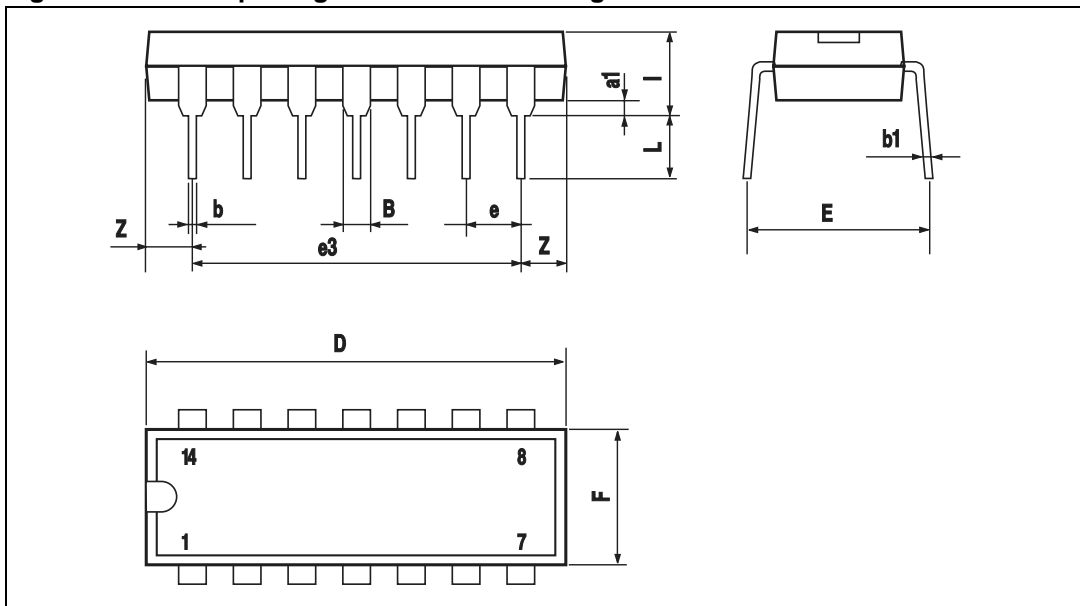


Table 11. DIP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

### 3.7 SO-14 package information

Figure 54. SO-14 package mechanical drawing

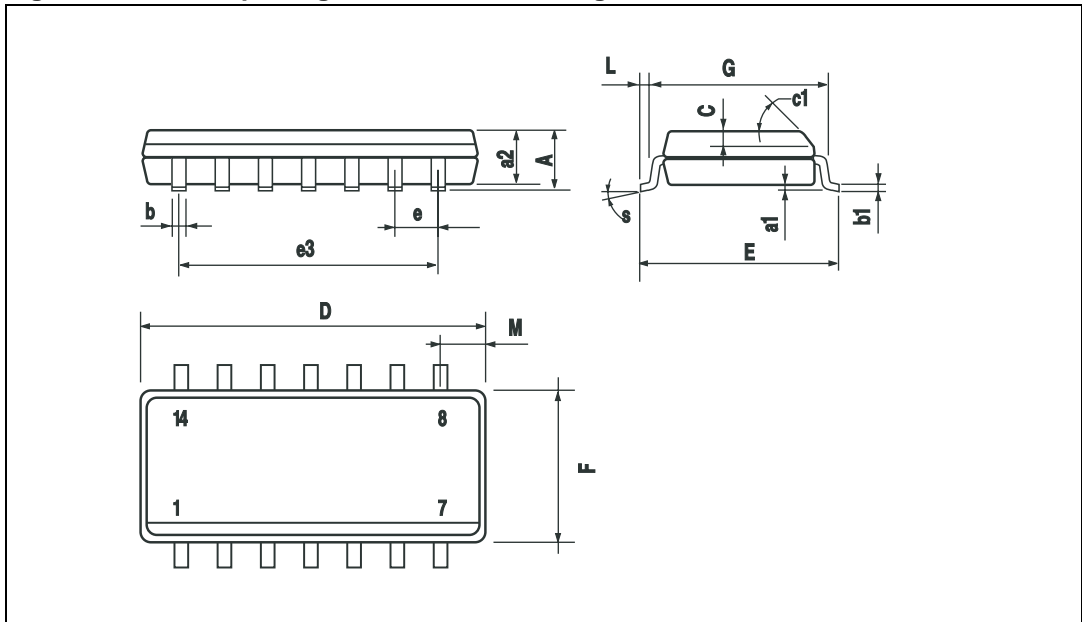


Table 12. SO-14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

### 3.8 TSSOP14 package information

Figure 55. TSSOP14 package mechanical drawing

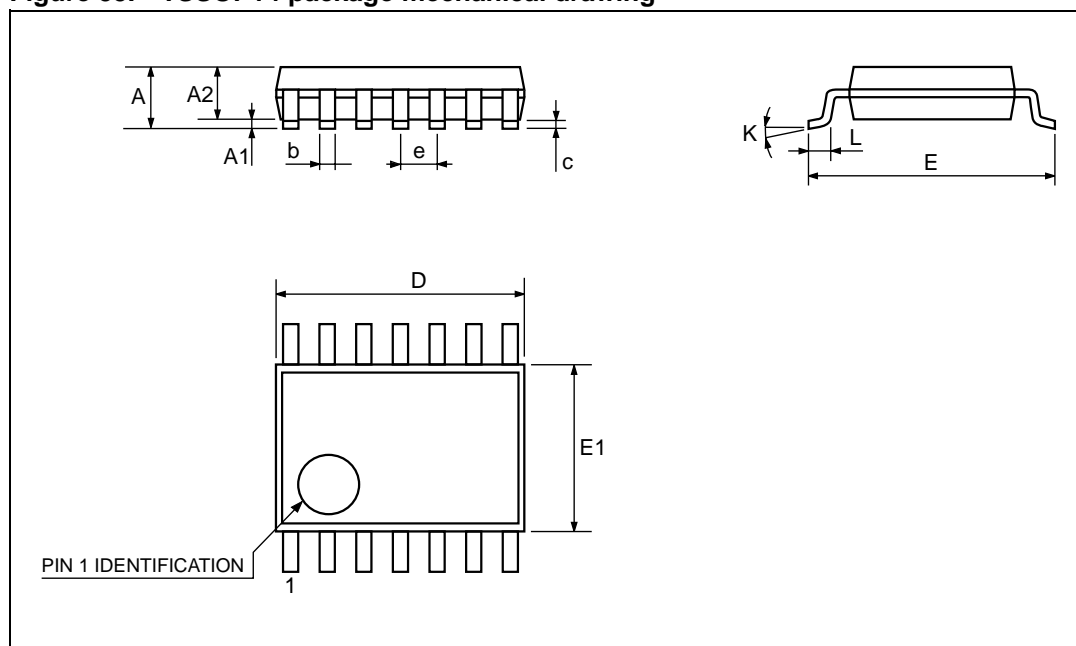


Table 13. TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L1	0.45	0.60	0.75	0.018	0.024	0.030

## 4 Ordering information

Table 14. Order codes

Order code	Temperature range	Package	Packing	Marking
TS1871ID/IDT TS1871AID/AIDT	-40°C to +125°C	SO-8	Tube or tape & reel	1871I 1871AI
TS1871IYD/IYDT <sup>(1)</sup> TS1871AIYD/AIYDT <sup>(1)</sup>		SO-8 (Automotive grade)	Tube or tape & reel	1871Y 1871AY
TS1871ILT TS1871AILT		SOT23-5L	Tape & reel	K171 K172
TS1871IYLT <sup>(1)</sup> TS1871AIYLT <sup>(1)</sup>		SOT23-5L (Automotive grade)	Tape & reel	K182 K183
TS1872IN TS1872AIN		DIP8	Tube	1872IN 1872AIN
TS1872ID/IDT TS1872AID/AIDT		SO-8	Tube or tape & reel	1872I 1872AI
TS1872IYD/IYDT <sup>(1)</sup> TS1872AIYD/AIYDT <sup>(1)</sup>		SO-8 (Automotive grade)	Tube or tape & reel	1872Y 1872AY
TS1872IPT TS1872AIPT		TSSOP8	Tape & reel	1872I 1872A
TS1872IYPT <sup>(1)</sup> TS1872AIYPT <sup>(1)</sup>		TSSOP8 (Automotive grade)	Tape & reel	1872Y 872AY
TS1872IST TS1872AIST		MiniSO-8	Tape & reel	K171 K172
TS1874IN TS1874AIN		DIP14	Tube Tube	1874IN 1874AIN
TS1874ID/IDT TS1874AID/AIDT		SO-14	Tube or tape & reel	1874I 1874AI
TS1874IYD/IYDT <sup>(1)</sup> TS1874AIYD/AIYDT <sup>(1)</sup>		SO-14 (Automotive grade)	Tube or tape & reel	TS1874Y TS1874AY
TS1874IPT TS1874AIPT		TSSOP14	Tape & reel	1874I 1874AI
TS1874IYPT <sup>(1)</sup> TS1874AIYPT <sup>(1)</sup>		TSSOP14 (Automotive grade)	Tape & reel	TS1874Y TS1874AY

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.



## 5 Revision history

**Table 15. Document revision history**

Date	Revision	Changes
1-Apr-2002	1	First release.
2-Jan-2005	2	Modifications on AMR <a href="#">Table 1 on page 3</a> (explanation of $V_{id}$ and $V_i$ limits).
21-May-2007	3	<p>Added limits over temperature range in <a href="#">Table 3 on page 5</a>, <a href="#">Table 4 on page 6</a>, <a href="#">Table 5 on page 7</a>.</p> <p>Added SVR in <a href="#">Table 5</a> (SVR parameter removed from <a href="#">Table 3</a> and <a href="#">Table 4</a>).</p> <p>Added equivalent input voltage noise in <a href="#">Table 3</a>, <a href="#">Table 4</a>, and <a href="#">Table 5</a>.</p> <p>Added <math>R_{thjc}</math> values in <a href="#">Table 1</a>.</p> <p>Added automotive grade part numbers to order codes table.</p> <p>Moved order codes table to <a href="#">Section 4 on page 24</a>.</p> <p>Updated format of package information.</p>
17-Jan-2008	4	Updated footnote for automotive grade order codes in <a href="#">Table 14</a> .

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