



# MX23L6410

## 64M-BIT (8M x 8 / 4M x 16) Mask ROM

### FEATURES

- Bit organization
  - 8M x 8 (byte mode)
  - 4M x 16 (word mode)
- Fast access time
  - Random access: 90ns (max.) for 3.0V~3.6V
  - 100ns (max.) for 2.7V~3.6V

**Notes: die form: 2.7~3.6V 90ns**

- Current
  - Operating: 50mA (max.)
  - Standby: 15uA (max.)
- Supply voltage
  - 2.7V~3.6V
- Package
  - 44 pin SOP (500 mil)
  - 48 pin TSOP (12mm x 20mm)
  - 44 pin TSOP (Type II)

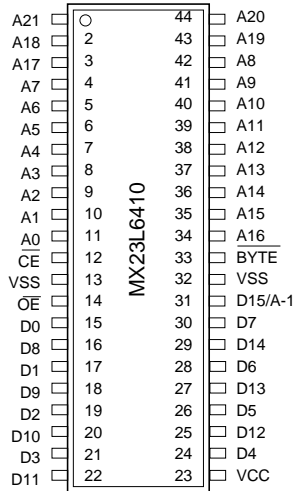
### ORDER INFORMATION

Part No.	Access Time	Package
MX23L6410MC-10	100ns	44 pin SOP
MX23L6410MC-12	120ns	44 pin SOP
MX23L6410MC-15	150ns	44 pin SOP
MX23L6410TC-90	90ns	48 pin TSOP
MX23L6410TC-10	100ns	48 pin TSOP
MX23L6410TC-12	120ns	48 pin TSOP
MX23L6410TC-15	150ns	48 pin TSOP
MX23L6410RC-10	100ns	48 pin TSOP (Reverse type)
MX23L6410RC-12	120ns	48 pin TSOP (Reverse type)
MX23L6410RC-15	150ns	48 pin TSOP (Reverse type)
MX23L6410YC-10	100ns	44 pin TSOP
MX23L6410YC-12	120ns	44 pin TSOP
MX23L6410YC-15	150ns	44 pin TSOP
MX23L6410TI-10	100ns	48 pin TSOP

Note: Industrial grade temperature: -40° C~ 85° C  
Commercial grade temperature: 0° C ~ 70° C

## PIN CONFIGURATION

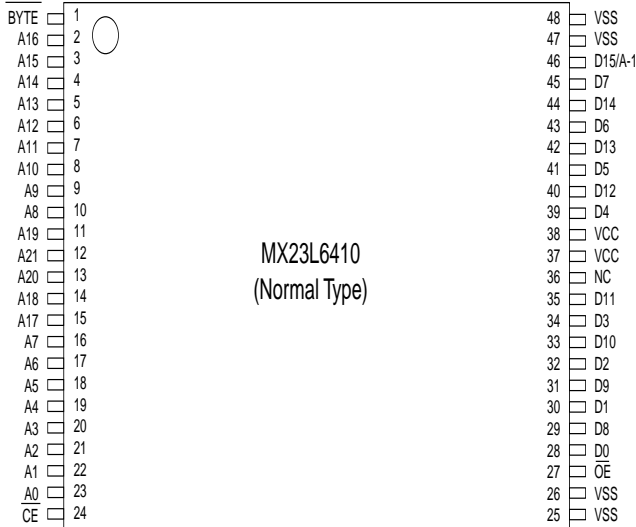
### 44 SOP/44 TSOP



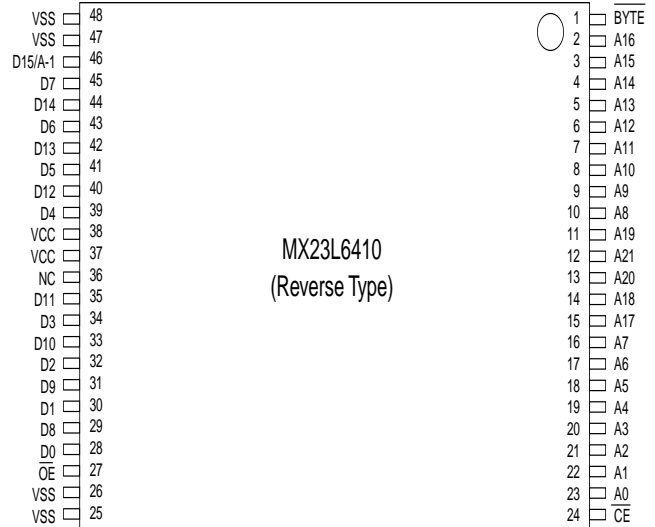
## PIN DESCRIPTION

Symbol	Pin Function
A0~A21	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode) / LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
Byte	Word / Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

### 48 TSOP (NORMAL TYPE)

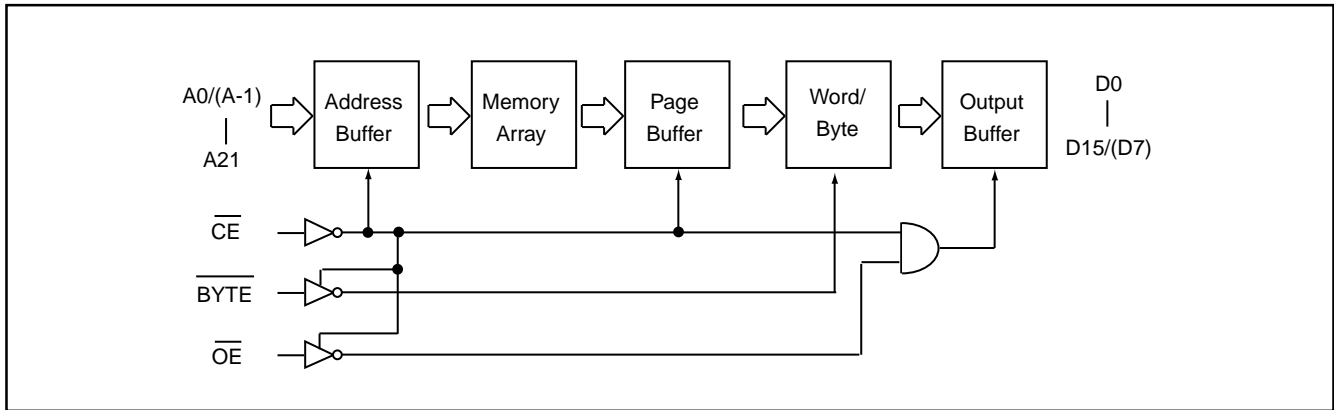


### 48 TSOP (REVERSE TYPE)



## MODE SELECTION

$\overline{CE}$	$\overline{OE}$	Byte	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

**BLOCK DIAGRAM**

**ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Ratings
Supply Voltage Relative to VSS	VCC	-0.3V to 4.3V
Voltage on any Pin Relative to VSS	VIN	-0.5V to VCC + 2V
Ambient Operating Temperature	T <sub>opr</sub>	0° C to 70° C (Commercial Grade) -40° C to 85° C (Industrial Grade)
Storage Temperature	T <sub>stg</sub>	-65° C to 125° C

**DC CHARACTERISTICS (T<sub>a</sub> = 0° C ~ 70° C for Commercial Grade, T<sub>a</sub> = -40° C ~ 85° C for Industrial Grade, VCC = 2.7V~3.6V)**

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	I <sub>OH</sub> = -0.4mA
Output Low Voltage	VOL	-	0.4V	I <sub>OL</sub> = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	50mA	f=5MHz, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$ = VIH
Standby Current (CMOS)	ISTB2	-	15uA	$\overline{CE}$ > VCC-0.2V
Input Capacitance	CIN	-	10pF	T <sub>a</sub> = 25° C, f = 1MHZ
Output Capacitance	COUT	-	10pF	T <sub>a</sub> = 25° C, f = 1MHZ

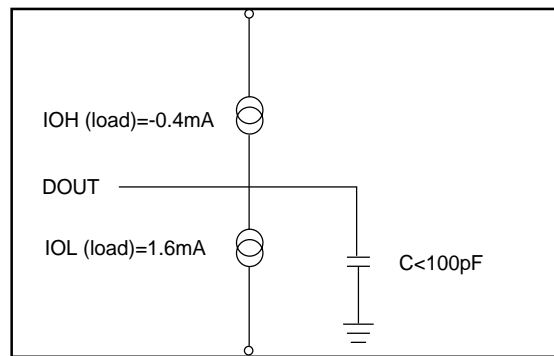
**AC CHARACTERISTICS** ( $T_a = 0^\circ\text{C} \sim 70^\circ\text{C}$  for Commercial Grade,  $T_a = -40^\circ\text{C} \sim 85^\circ\text{C}$  for Industrial Grade,  $V_{CC} = 2.7\text{V} \sim 3.6\text{V}$ )

Item	Symbol	23L6410-90		23L6410-10		23L6410-12		23L6410-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	90ns	-	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	90ns	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	90ns	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	30ns	-	30ns	-	60ns	-	70ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from  $\overline{\text{OE}}$  or  $\overline{\text{CE}}$  going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

### AC Test Conditions

Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



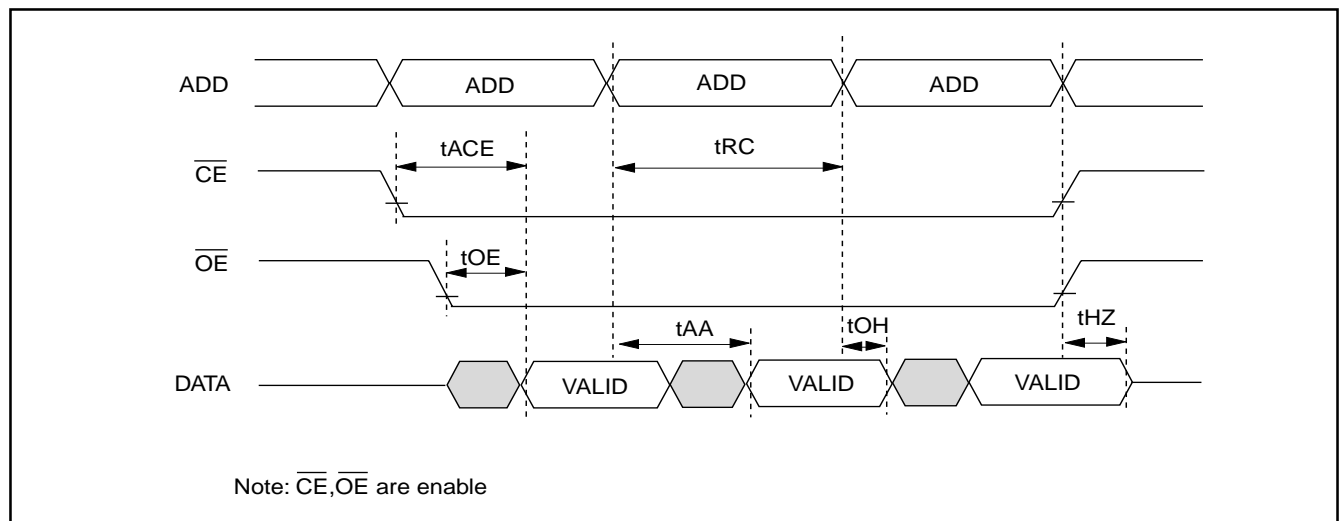
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

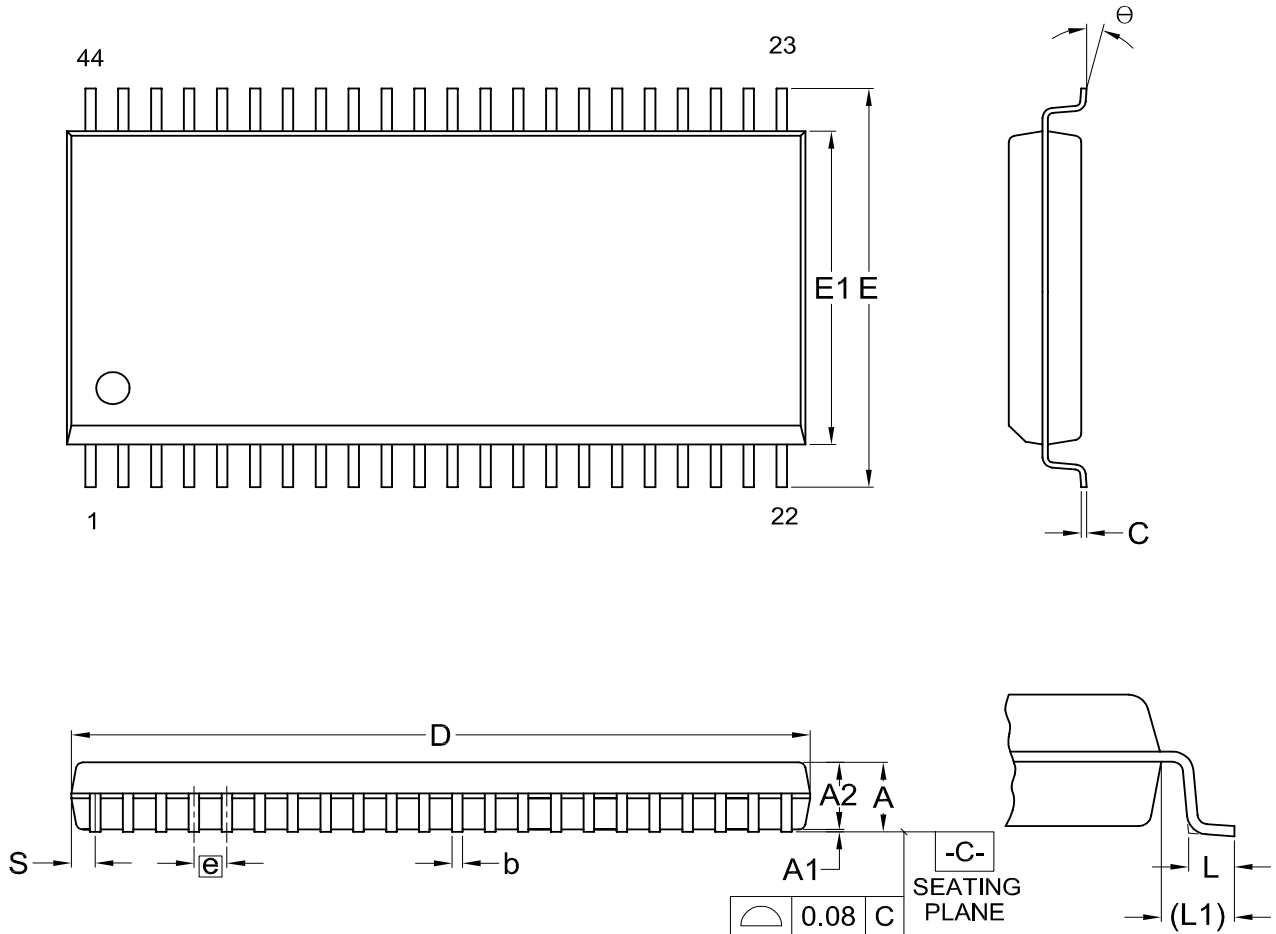
### TIMING DIAGRAM

### RANDOM READ



## PACKAGE INFORMATION

Title: Package Outline for SOP 44L (500MIL)

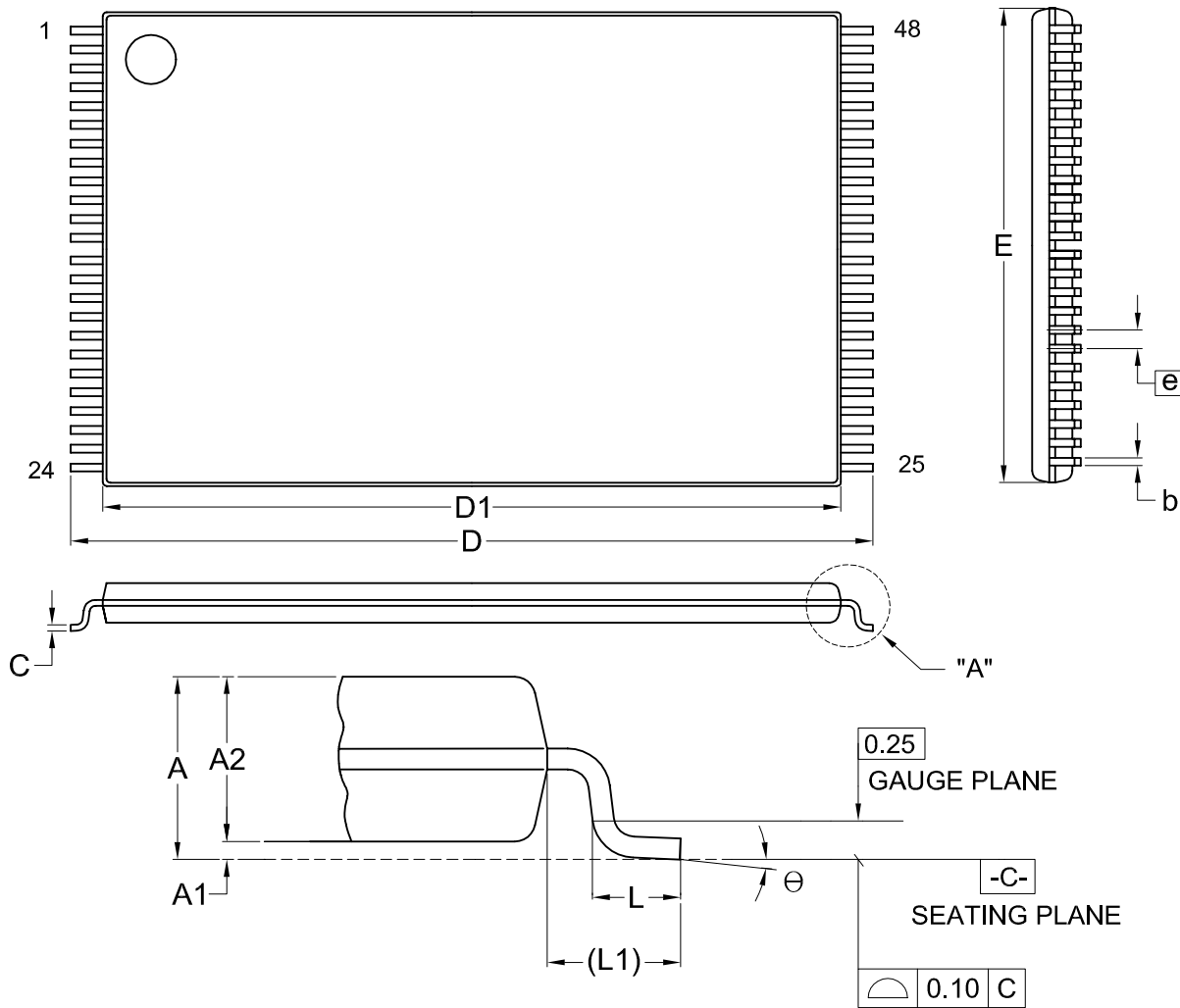


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	$\theta$
UNIT														
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47		0.56	1.51	0.78	0
	Nom.	---	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73		0.96	1.91	1.04	10
Inch	Min.	---	0.004	0.102	0.014	0.006	1.117	0.623	0.491		0.022	0.059	0.031	0
	Nom.	---	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501		0.038	0.075	0.041	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1405	6	MO-175			11-26-'03

**Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM**



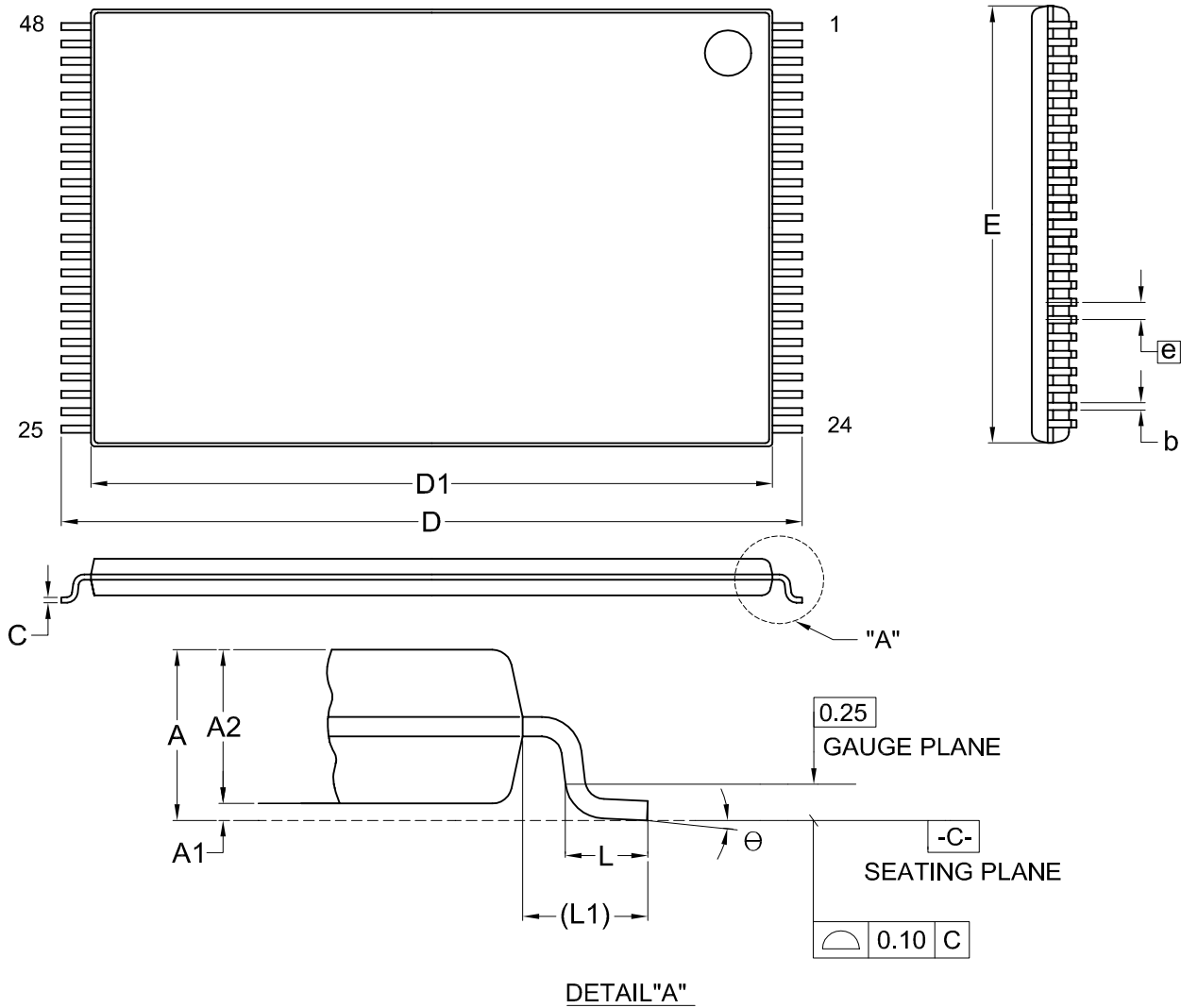
**DETAIL "A"**

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	θ
UNIT													
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	7	MO-142			12-01-'03

**Title: Package Outline for TSOP(I) 48L (12X20mm)REVERSE FORM**

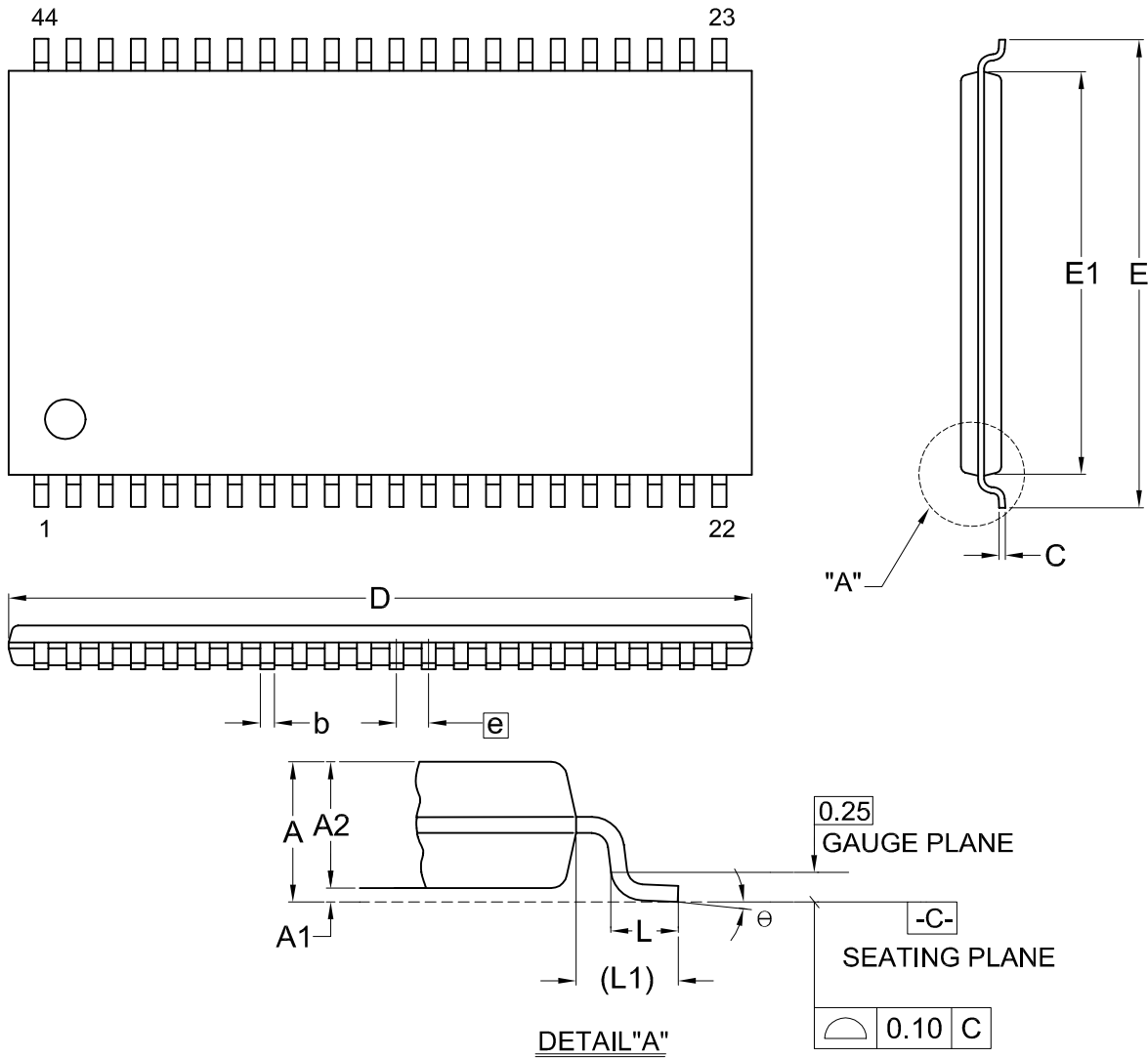


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
UNIT													
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607.1	7	MO-142			12-01-'03

**Title: Package Outline for TSOP(II) 44L (400MIL)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	Θ
UNIT													
mm	Min.	---	0.05	0.95	0.30	0.12	18.31	11.56	10.06		0.40	0.70	0
	Nom.	---	0.10	1.00	0.35	0.15	18.41	11.76	10.16	0.80	0.50	0.80	5
	Max.	1.20	0.15	1.05	0.45	0.21	18.51	11.96	10.26		0.60	0.90	8
Inch	Min.	---	0.002	0.037	0.012	0.005	0.721	0.455	0.396		0.016	0.028	0
	Nom.	---	0.004	0.039	0.014	0.006	0.725	0.463	0.400	0.031	0.020	0.031	5
	Max.	0.047	0.006	0.041	0.018	0.008	0.729	0.471	0.404		0.024	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1701	6	MS-024			12-01-'03



**REVISION HISTORY**

<b>REVISION</b>	<b>DESCRIPTION</b>	<b>PAGE</b>	<b>DATE</b>
1.9	AC CHARACTERISTICS tOH 10ns-->0ns	P3	JAN/29/1999
2.0	DC CHARACTERISTICS ISTB2 5uA-->15uA	P3	SEP/03/1999
2.1	DC Characteristics voltage range VCC=2.9V~3.6V-->3.0V~3.6V	P3	DEC/24/1999
2.2	Modify Operating Current:60mA-->50mA	P1,3	DEC/29/2000
2.3	Modify Package Information	P5,6	JUL/18/2001
	Added 44-pin TSOP Package	P1,7	
	Added Access time:100ns	P1,3	
2.4	Change VCC from 3.0~3.6V to 2.7~3.3V	P1,3	AUG/03/2001
2.5	Change Voltage:2.7V~3.3V-->2.7V~3.6V	P1,3	AUG/21/2001
2.6	Change Voltage:2.7V~3.6V-->2.4V~3.6V	P1,3	NOV/26/2001
	Change Operating Current:50mA-->13mA	P1,3	
2.7	Change Voltage:2.4V~3.6V-->2.7V~3.6V	P1,3	NOV/29/2001
	Change Operating Current:13mA-->50mA	P1,3	
2.8	Removed 44-pin TSOP Package	P1,7	JAN/15/2002
2.9	1. Add supply voltage relative to VSS	P3	JUL/19/2002
	2. Change voltage on any pin relative to VSS:-0.5V to VCC+2.0	P3	
3.0	1. Modify Package Information	P5~7	NOV/21/2002
3.1	1. Add 44-pin TSOP package	P1,8	MAY/13/2003
3.2	1. Add access time:90ns	P1,3	JUL/09/2003
3.3	1. Delete MX23L6410RC/MC/YC-90	P1	SEP/08/2003
3.4	1. Modify random access: 90ns (max.) for 3.0V~3.6V; 100ns (max.) for 2.7V~3.6V	P1	SEP/26/2003
3.5	1. Add Notes: die form: 2.7~3.6V 90ns	P1	MAY/25/2004
3.6	1. Add I-grade package	P1	JUL/15/2004
3.7	1. Add I-grade temperature	P3,4	JUL/29/2004



**MX23L6410**

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