Standard Products

PWM5031 RadHard High Speed PWM Controller

www.aeroflex.com/Power

August 2, 2005

FEATURES

- Radiation Hardness:
  - Total Dose 1MRad(Si)
  - Single Event Upset (SEU) 100MeV-cm^2/mg
- CMOS Low Power Design
- Sleep & Enable Control Lines
- Optimized for Applications: Buck, Boost, Flyback, Forward and Center Tapped Push-Pull Converters
- Supports Current Mode or Voltage Mode Operations
- Selectable 50% / 100% Duty Cycle
- Under-Voltage Lockout with Hysteresis
- Dual ±1Amp Peak Totem Pole Outputs
- 1 MHz Maximum – User Selectable
- Low RO Error Amp
- Auxiliary Op Amp with Shut Down Pin
- Power OK Indicator
- Designed for Commercial, Industrial and Aerospace Applications
- Ceramic 24-Gull lead, Hermetic Package, .6L x .3W x .13H
  - Contact Factory for Die Availability
- DSCC SMD Pending

  NOTE: Aeroflex Plainview does not currently have a DSCC Certified Radiation Hardened Assurance Program

Developed in Partnership with JHU/APL and the Technology Application Group for the Mars Technology Program; Part of NASA's Mars Exploration Program

OVERVIEW AND GENERAL OPERATION

The chip is a fixed frequency Pulse Width Modulator based on the industry standard UC1843x Series with significant enhancements in performance and functionality. The chip operates in either the voltage or current mode and can support a wide variety of converter topologies.

Radiation hardened by design techniques ensure the chip's outstanding radiation tolerance (>1MRads) while reducing operating current by more than an order of magnitude over comparable parts.

The PWM5031 provides an under voltage lockout feature with hysteresis that also provides an output to indicate Power is OK. An input called Sleep is used to power down the entire chip, the Enable input is used to shut down the Oscillator / Output Drives, and the Soft input drives the Output to zero. There is also a signal input called ENAUX that is used to disable the output to the auxiliary op-amp.

The dual output drivers are designed using a Totem Pole output capable of sinking and sourcing 50mA constant current and peak currents up to 1 Amp to support a large variety of Power MOSFETs.

Additional features that boost the appeal and utility of the part are:

- Dual break-before-make Totem Pole output stage is employed that virtually eliminates cross conduction and current shoot through
- Logic level input that allows the user to select either 50% or 100% maximum duty cycle operation
- Improved oscillator stage that vastly increases waveform linearity and reduces output voltage error
- Uncommitted on-board op-amp which can be used for signal conditioning, pulse feedback, or any other user defined purpose

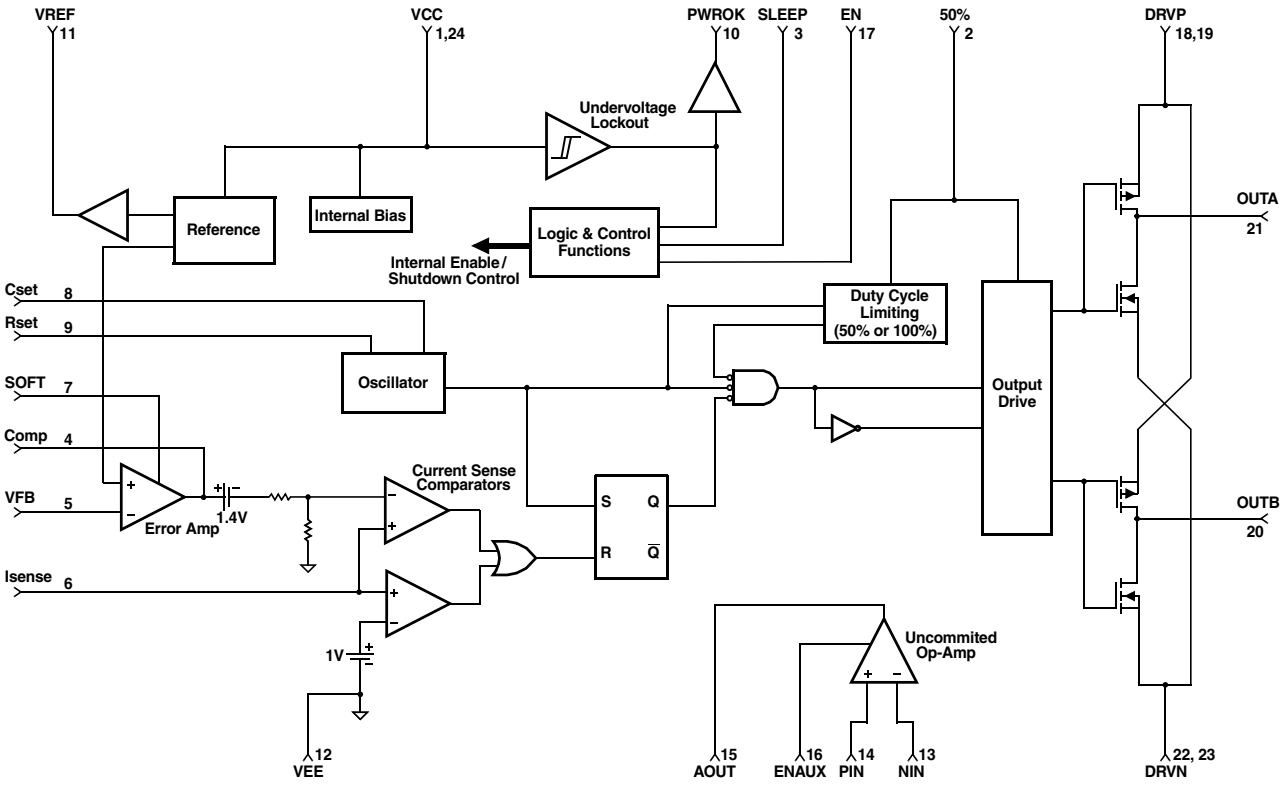


FIGURE 1 – Block Diagram

PWM5031 PWM PIN DESCRIPTION

PIN #	SIGNAL NAME	FUNCTION DESCRIPTION
1 24	VCC	Logic Power
2	50%	Input selects maximum duty cycle (50% or 100%). Logic "1" selects 50% max duty cycle and Output B is the complement of Output A. Logic "0" selects 100% and Output A is in-phase with Output B.
3	SLEEP	This Input shuts down all functions on chip when asserted (Active Hi)
4	COMP	Output of the error amplifier. Place compensation network from this pin to VFB to stabilize converter.
5	VFB	Negative Input to the error amplifier
6	ISENSE	Input Current sense pin used for current mode control
7	SOFT	This High impedance Input is used to limit the error amplifier output voltage. Applying an RC circuit to this pin provides the standard softstart function. Pull the pin to ground to force zero duty cycle.
8	CSET	Works with Rset to establish oscillator free running frequency. Place cap from this Input pin to ground. Can synchronize oscillator by overdriving this pin with an external frequency source.
9	RSET	Works with Cset to establish oscillator free running frequency. Place resistor from this Input pin to ground.
10	PWROK	Logical output of UV lockout circuit -- logic "1" indicates chip has valid Vcc
11	VREF	Buffered 3V Output reference voltage
12	VEE	Logic Ground
13	NIN	Auxiliary Op-Amp Inverting Input
14	PIN	Auxiliary Op-Amp Non-Inverting Input
15	AOUT	Auxiliary Op-Amp Output
16	ENAUX	Input Enable of Auxiliary Op-Amp (Active Hi)
17	EN	Logic Input that enables the oscillator and output drivers. Reference voltage remains valid (Active Hi).
18 19	DRVN	Output stage negative rail
20	OUT B	Totem pole Output B
21	OUT A	Totem pole Output A
22 23	DRVP	Output stage positive rail

ABSOLUTE MAXIMUM RATINGS[1]

Junction Temperature Range	-55°C to +150°C
Storage Temperature Range	-65°C to +150°C
V_{CC} & DRVP Supply Voltages	7.0 V_{DC}
Steady State Output Current	±50 mA
Peak Output Current (Internally Limited)	±1.0 A
Analog Inputs (Pins 5, 6, 13, 14)	V_{EE} - 0.5 V to V_{CC} + 0.5 V
Power Dissipation at T_A = +25°C	500 mW
Lead Temperature (soldering, 10 seconds)	300°C

Note 1: All voltages are with respect to Pin 12. All currents are positive into the specified terminal.

OPERATING CONDITIONS

PARAMETER	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
DC Operating Voltage	-	V_{CC}	4.5	5.0	5.5	V
Quiescent Current	SLEEP @ '0'; EN & ENAUX @ '1'	I_{CC}	-	-	4.0	mA
Output Drive Voltage	-	DRVP	-	-	5.0	V
Output Duty Cycle – Maximum 50% Pin = Logic 0 50% Pin = Logic 1	 100% Duty Cycle 50% Duty Cycle	 - -	 97* -	 - -	 - 50	 % %
Thermal Resistance T_{JC}	-	-	-	-	6.0	°C/W
Sleep Mode	-	I_{CCS}	-	-	20	µA

* Dependent on Value of C_{SET} & Operating Frequency

ELECTRICAL CHARACTERISTICS

4.5 V ≤ Vcc ≤ 5.5 V, -55°C ≤ T_A ≤ +125°C, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Reference Voltage	T_A = 25°C, I_O = -1 mA	2.95	3.05	3.15	V
Line Regulation		-	±.1	-	%
Load Regulation	0 ≤ I_O ≤ 25 mA	-	±.05	-	%
Thermal Regulation		-	±1	-	%
Output Short Circuit	Note 2	-	-	-40	mA
Oscillator Section					
Frequency Range	Note 2	20	-	1,000	KHz
Frequency Stability (Part to Part)	Note 2	-	±1.5	±2	%
Temperature Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 2)	-	±0.5	±1	%
R_{SET} Range	Note 2	50	-	-	KΩ
C_{SET} Range	Note 2	-	-	600	pF

ELECTRICAL CHARACTERISTICS con't

4.5 V ≤ Vcc ≤ 5.5 V, -55°C ≤ T_A ≤ +125°C, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amp Section					
Input Offset Voltage	Note 2	-	-	3.3	mV
Input Common Mode Voltage Range	Note 2	V_{EE} + 0.2	-	V_{CC} - 0.2	V
Input Bias Current	Note 2	-	-	-1.0	µA
Open Loop Voltage Gain (AVOL)	Note 2	100	-	-	dB
Unity Gain Bandwidth	Note 2	1.0	2.0	-	MHz
Power Supply Rejection Ratio (PSRR)	Note 2	60	-	-	dB
Output Sink Current	V_{FB} = 3.0V, V_{SOFT} = 1.1V	-	-	+62	mA
Output Source Current	V_{FB} = 2.0V, V_{SOFT} = 5V	-	-	-40	mA
V_{OUT} High (Limited by V_{SOFT})	V_{FB} = 2.0V, R_L = 15K to GND	V_{SOFT} - 0.2	-	-	V
V_{OUT} Low	V_{FB} = 3.0V, R_L = 15K to +5V	-	-	V_{EE} + 0.2	V
Current Sense Section					
Input Offset Voltage	Note 2	-	-	3.3	mV
Common Mode Input Voltage	V_{SOFT} = 5V, Note 2 & 3	0.1	-	1.0	V
Input Bias Current	Note 2	-	-	1.0	µA
I_{SENSE} to Output Delay		-	80	100	ns
Output Section					
Output Low Level	I_{SINK} = 1.0mA	-	-	0.1	V
	I_{SINK} = 50mApk	-	-	0.3	V
Output High Level	I_{SOURCE} = 1.0mA, DRVP = 5V	4.9	-	-	V
	I_{SOURCE} = 50mApk, DRVP = 5V	4.7	-	-	V
Peak Output Current		-	±1.35	-	A
Steady State Output Current		-	50	-	mA
Rise Time	T_A = 25°C, C_L = 1.0nF	-	8.0	-	ns
Fall Time	T_A = 25°C, C_L = 1.0nF	-	6.0	-	ns

ELECTRICAL CHARACTERISTICS con't

4.5 V ≤ Vcc ≤ 5.5 V, -55°C ≤ T_A ≤ +125°C, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Auxiliary Amp Section					
Input Offset Voltage		-	-	3.5	mV
Input Common Mode Voltage Range	Off V_{EE} or V_{CC} Rail, Note 2	V_{EE} + 0.2	-	V_{CC} - 0.2	V
Input Bias Current	Note 2	-	-	1.0	µA
AVOL	f = 40KHz, 2V ≤ V_O ≤ 4V, Note 2	100	-	-	dB
Unity Gain Bandwidth	Note 2	1.0	-	-	MHz
PSRR	4.5V ≤ V_{CC} ≤ 5.5V, Note 2	60	70	-	dB
Output Sink Current	V_{PIN} < V_{NIN}, ENAUX = Hi	-	-	+80	mA
Output Source Current	V_{PIN} > V_{NIN}, ENAUX = Hi	-	-	-50	mA
V_{OUT} High	V_{PIN} > V_{NIN}, ENAUX = Hi	V_{CC} - 0.2	-	-	V
V_{OUT} Low	V_{PIN} < V_{NIN}, ENAUX = Hi	-	-	V_{EE} + 0.2	V
Under-Voltage Lockout Section					
Start Threshold		4.0	4.1	4.25	V
Operating Voltage After Turn On, Min.		3.4	3.5	3.65	V
Digital Inputs					
V_{IL}	Logic Low	-	-	0.8	V
V_{IH}	Logic High	2.0	-	-	V
Leakage Current - I_{IN}		-	-	100	nA
Digital Ouput (PWROK)					
V_{OL}	Logic low at 1.6mA	-	-	V_{EE} + 0.3	V
V_{OH}	Logic high at -1.6mA	V_{CC} - 0.6	-	-	V

Note 2. Parameters are guaranteed by design, not tested.
Note 3. Parameter measured at trip point of latch with V_{FB} = 0.

DETAILED COMPONENT OPERATION AND PERFORMANCE

POWER SUPPLIES

Three I/O pins are used to supply power to the chip:

1) Two DRVP (referenced to DRVN) for the output stage.
2) VCC (referenced to VEE) for all other functions.

VCC and DRVP are at 5V ± 10%. The two supplies are routed from separate pins to prevent power stage switching spikes from interfering with the chip's other circuits. VCC is specified to draw a maximum of 4.0mA under normal operating conditions.

For protection against inadvertent over/undervoltages, the chip's input pins are diode clamped to the supply rails through current limiting resistors.

Undervoltage Lockout

The chip includes an internal undervoltage lockout circuit with built in hysteresis and a logic level power good indicator. The positive and negative going thresholds are nominally 4.1V and 3.5V, respectively. If Vcc is below this range, the oscillator, error amplifier, main comparators, and output drive circuits are all disabled. The power OK indicator is active high (logic "1") when a valid supply voltage is applied.

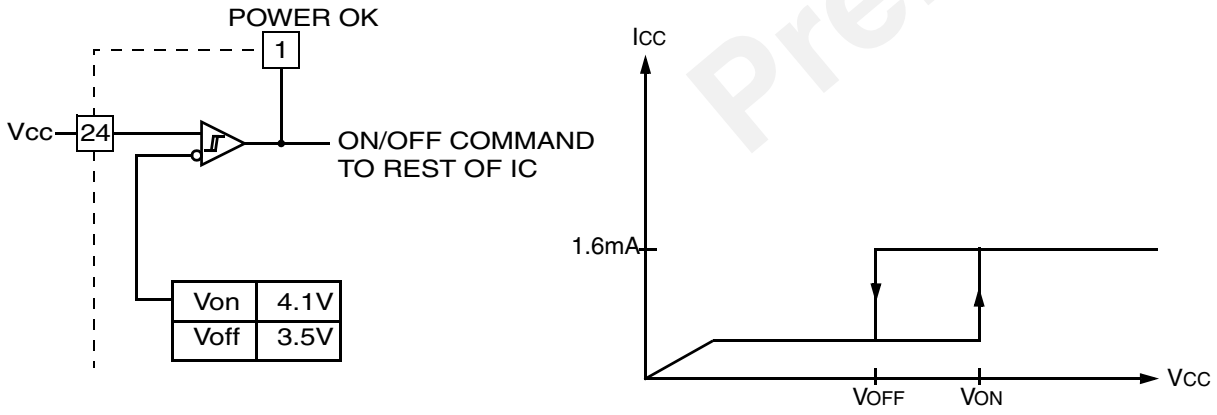


FIGURE 2 –Undervoltage Lockout

Shutdown Logic

The chip has two logic level inputs for implementing shutdown functions. Asserting a logic "1" on the SLEEP pin disables all chip functions and puts the chip into a very low power consumption mode. Asserting a logic "0" on the EN pin shuts down all functions except the reference, bias generators, and auxiliary amplifier.

INPUTS			OUTPUTS				
Sleep	EN	ENAUX	OUTA&B	AOUT	COMP	PWROK	Vref
0	0	0	0	0	0	Active	3 VDC
0	0	1	0	Active	0	Active	3 VDC
0	1	0	Active	0	Active	Active	3 VDC
0	1	1	Active	Active	Active	Active	3 VDC
1	X	X	0	0	0	0	0
1	X	X	0	0	0	0	0
1	X	X	0	0	0	0	0
1	X	X	0	0	0	0	0

Truth Table

OSCILLATOR

The chip uses two precision current mirrors that alternately charge and discharge an external capacitor to generate an extremely linear sawtooth oscillator waveform. At the start of each cycle, the charging current, set by the choice of resistor at the Rset pin, is 1:1 mirrored over to the Cset pin where it charges an external capacitor. When the capacitor voltage reaches the comparator's upper threshold (nominally V_{REF}), the comparator switches current mirrors and begins to discharge the external capacitor. The discharge current is set at roughly five times the charging current to result in fast discharge and minimal Dead Time. When the voltage reaches the comparator's lower threshold (0.9V), the comparator switches back to the charging mirror, powers down the discharge mirror, and the whole process repeats.

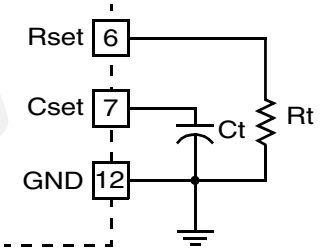
The frequency is set by choosing Rset and Cset such that:

$$F_{OSC} \approx \frac{1}{0.84 \times R_{SET} \times C_{SET}} \qquad 20KHz \le F_{OSC} \le 1MHz$$

Suggested Ranges for Cset and Rset are:

50K ohms < Rset < 300K

10pf < Cset < 600pF



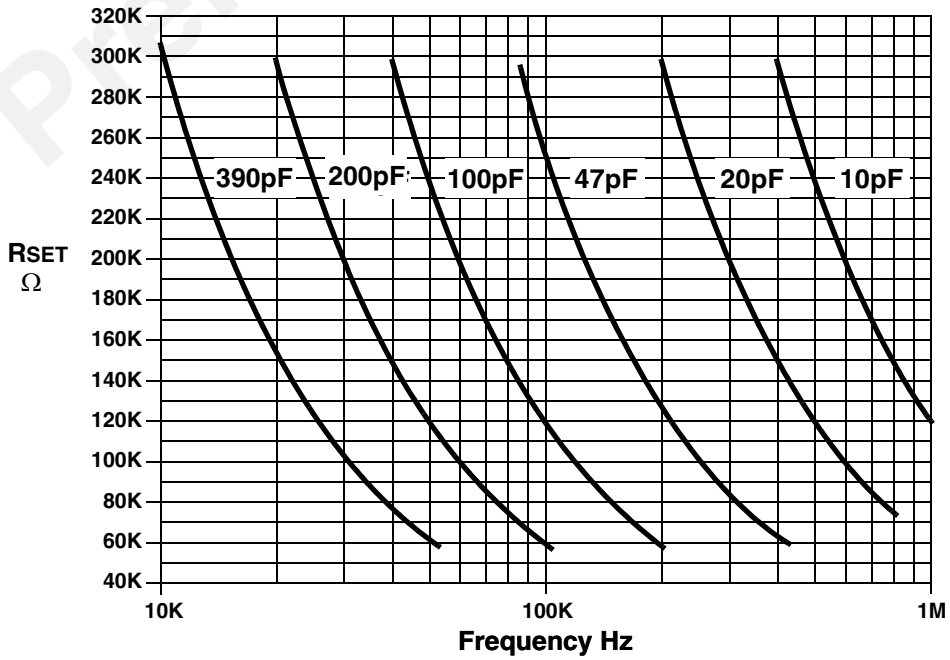


FIGURE 3 – Timing Resistance vs Frequency

Dead Time

The amount of dead time determines the maximum duty cycle that can be achieved. The Dead Time and the frequency of operation will determine the duty cycle.

$$Dead\ Time = 5280\ (C_{set} + 12pF) \qquad Duty\ Cycle = 1 - \left(\frac{Dead\ Time}{1/F_{osc}}\right)$$

Selecting Rset and Cset

To select values for Rset and Cset perform the following steps to insure the smallest Dead Time..

1) Determine what frequency is required for your design.
2) Use Figure 4 to select a capacitor value for Cset that will provide the highest duty cycle (shortest Dead Time) at the frequency required.
3) Calculate the value of Rset using the formula:

$$R_{set} = \frac{1}{.84 \times F_{osc} \times C_{set}}$$

Note small values of Rset increase power consumption for the PWM5031 and small values of Cset may make PCB and stray capacitance a source of error.

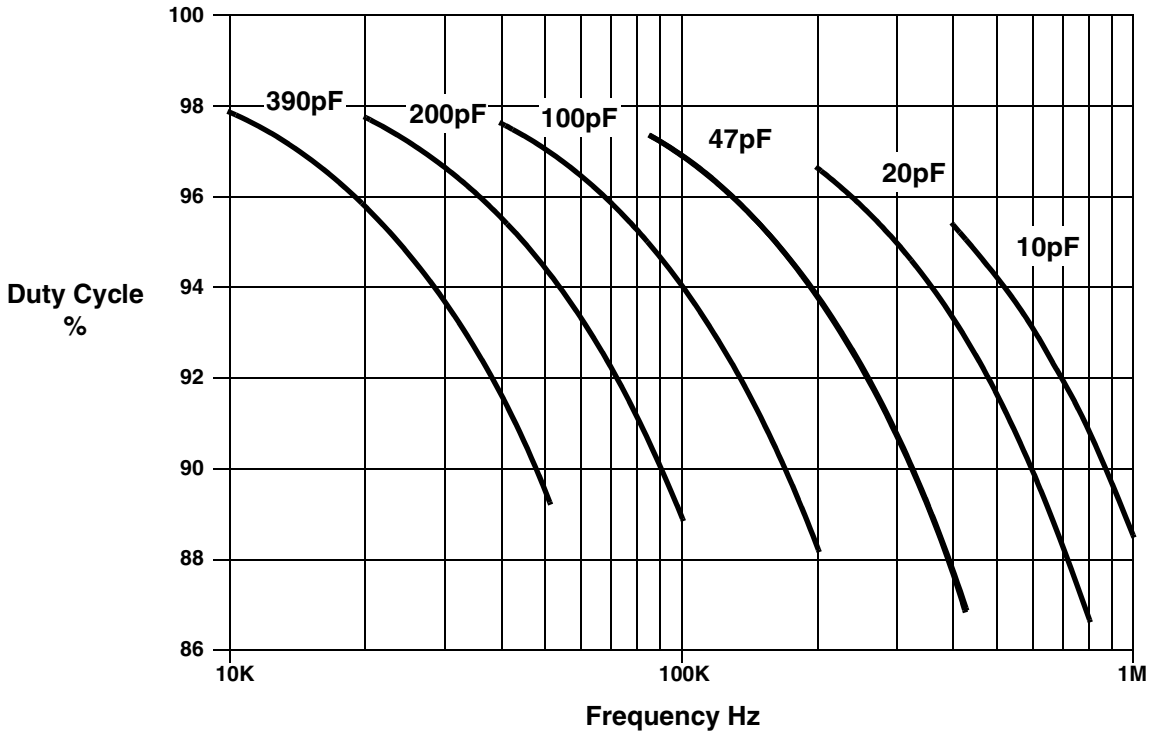


FIGURE 4 – Duty Cycle vs Frequency

If desired, the user can synchronize the oscillator to an external frequency source by coupling a pulse train to the Cset pin:

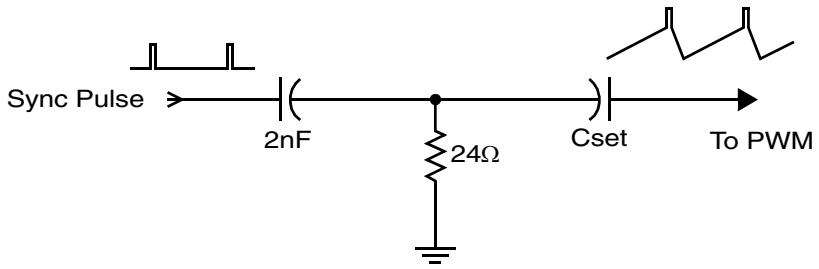


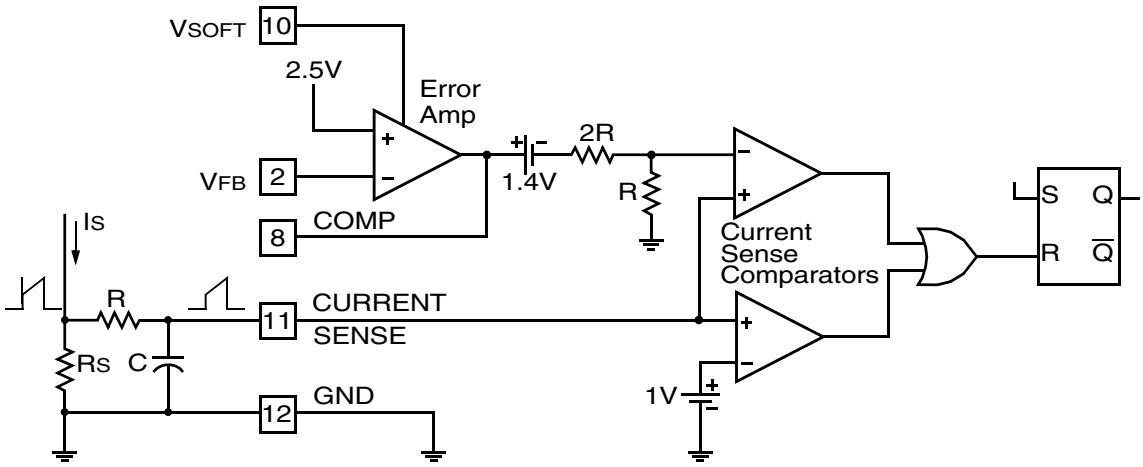
FIGURE 5 – PWM can be synchronized to external source with just two additional components.

Operation is similar to the free running case. Cset is alternately charged and discharged by the same current mirrors and the same comparator and thresholds are used. The only difference is that when a sync pulse is received, the capacitor voltage is level shifted up and reaches the comparator's upper threshold voltage *before it normally would in the free running case*. If a series of pulses are received with shorter period than that of the free running oscillator, the comparator will trip in response to the sync pulse and the oscillator will be synchronized. *(NOTE: The user must ensure that the sync pulse does not induce a voltage on CSET that exceeds the PWM5031 voltage rating. If this cannot be guaranteed, a simple diode clamp to the positive rail should be used to prevent damage to the PWM)*

ERROR AMPLIFIER

The main error amplifier is a N-type input folded cascode configuration with a few interesting additions. The positive input is internally tied to 2.5V derived from the on chip reference. The negative input typically draws less than 1µA and has a voltage offset of less than 2mV. At 20µA bias current, the amplifier exceeds 2MHz bandwidth and 120dB open loop gain (see Figure 7).

The amplifier is designed to limit at whatever voltage is applied to the SOFT pin. As mentioned previously, this function will allow the user to implement a softstart circuit, a controlled turn-on delay, or any number of other useful functions.



Peak Current (Is) is determined by the formula:

$$I_S MAX = \frac{1.0V}{R_S} \quad \text{or} \quad I_S MAX = \frac{V_{SOFT} - 1.4}{3R_S}$$

A small RC filter may be required to suppress switch transients

FIGURE 6 – Current Sense Circuit

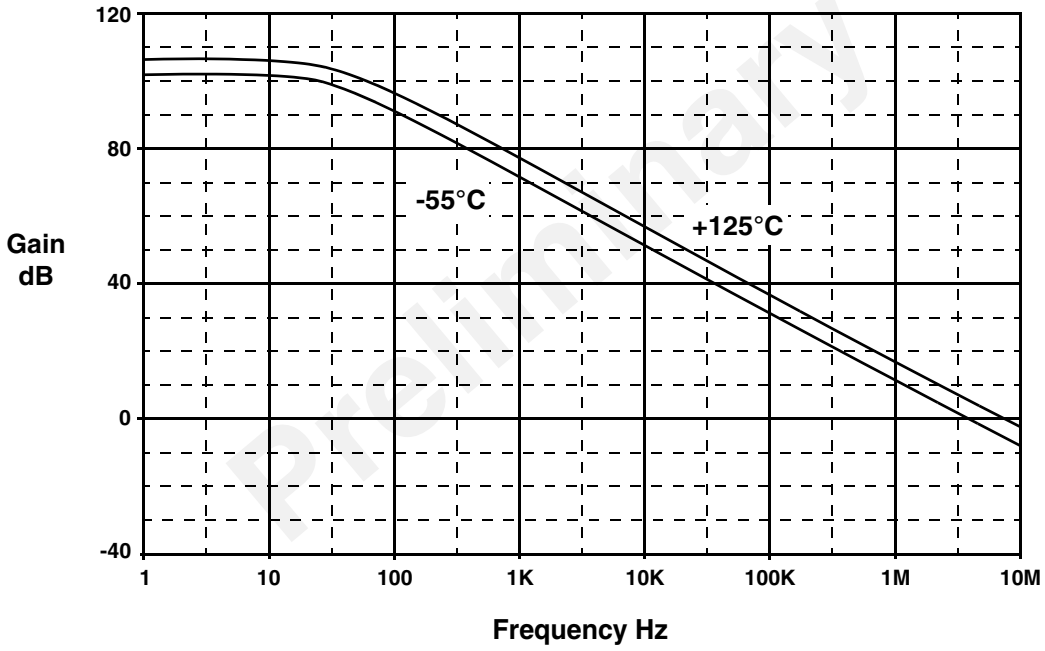


FIGURE 7 – Error Frequency Amplifier Open-Loop Response at +125°C & -55°C

OUTPUT DRIVE

Dual push-pull outputs OutA and OutB are provided for driving off chip switches. The output stages are identical:

- Totem Pole configuration
- Break-before-make switching to prevent harmful cross-conduction spikes
- Separate positive and negative supply connections to decouple power stage and sensitive logic
- Near rail-to-rail voltage swing
- ±1A maximum peak current capability (capacitive load)

The outputs have two modes of control depending on whether the 50% toggle option is selected. In the case where the 50% pin is logic low, the outputs are in-phase with each other and the duty cycle is free to take on any value up to 100%. However, when the 50% pin is asserted high (logic "1"), the outputs switch from the in-phase condition to the logical complement (out-of-phase) of each other and the duty cycle is limited to a maximum of 50%.

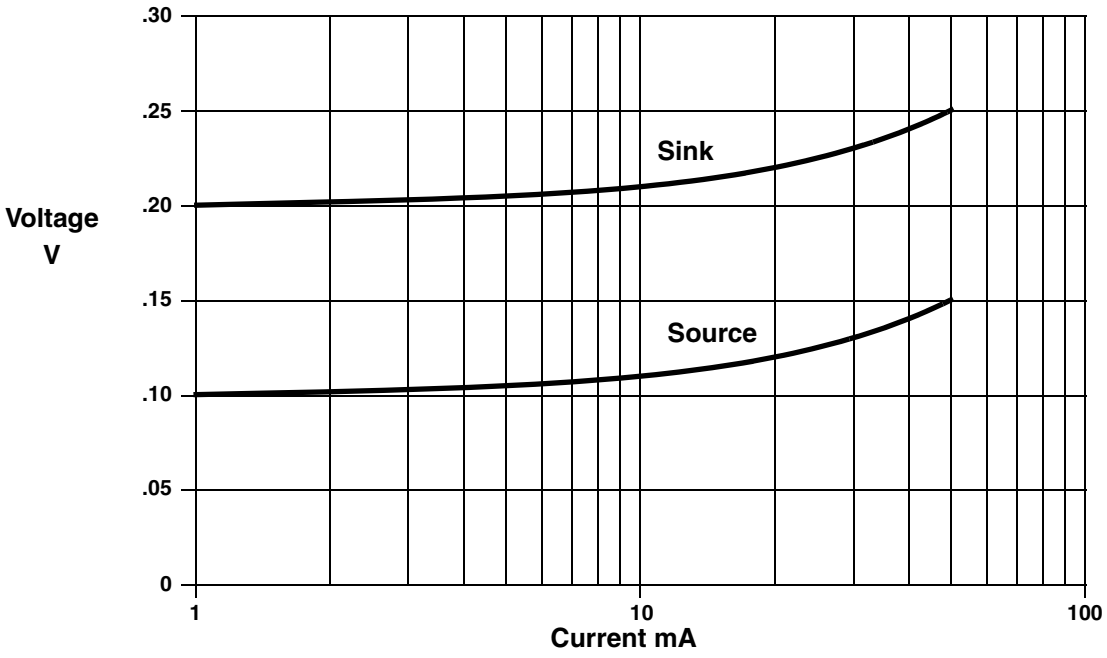


FIGURE 8 – Output Saturation Characteristics at +25°C

AUXILIARY AMPLIFIER

The chip includes an uncommitted op-amp with independent shutdown feature for use in any user-defined application. Some possibilities are:

- Signal conditioning of an isolated configuration feedback voltage
- Implementation of more sophisticated compensation networks for control loop optimization

The Auxiliary amplifier has a unity gain bandwidth greater than 1MHz and an open loop gain greater than 100dB. The ENAUX pin is active high such that a logic "1" enables the amplifier and logic "0" disables it. The amplifier has near rail-to-rail capability on both the input and output.

TYPICAL APPLICATIONS

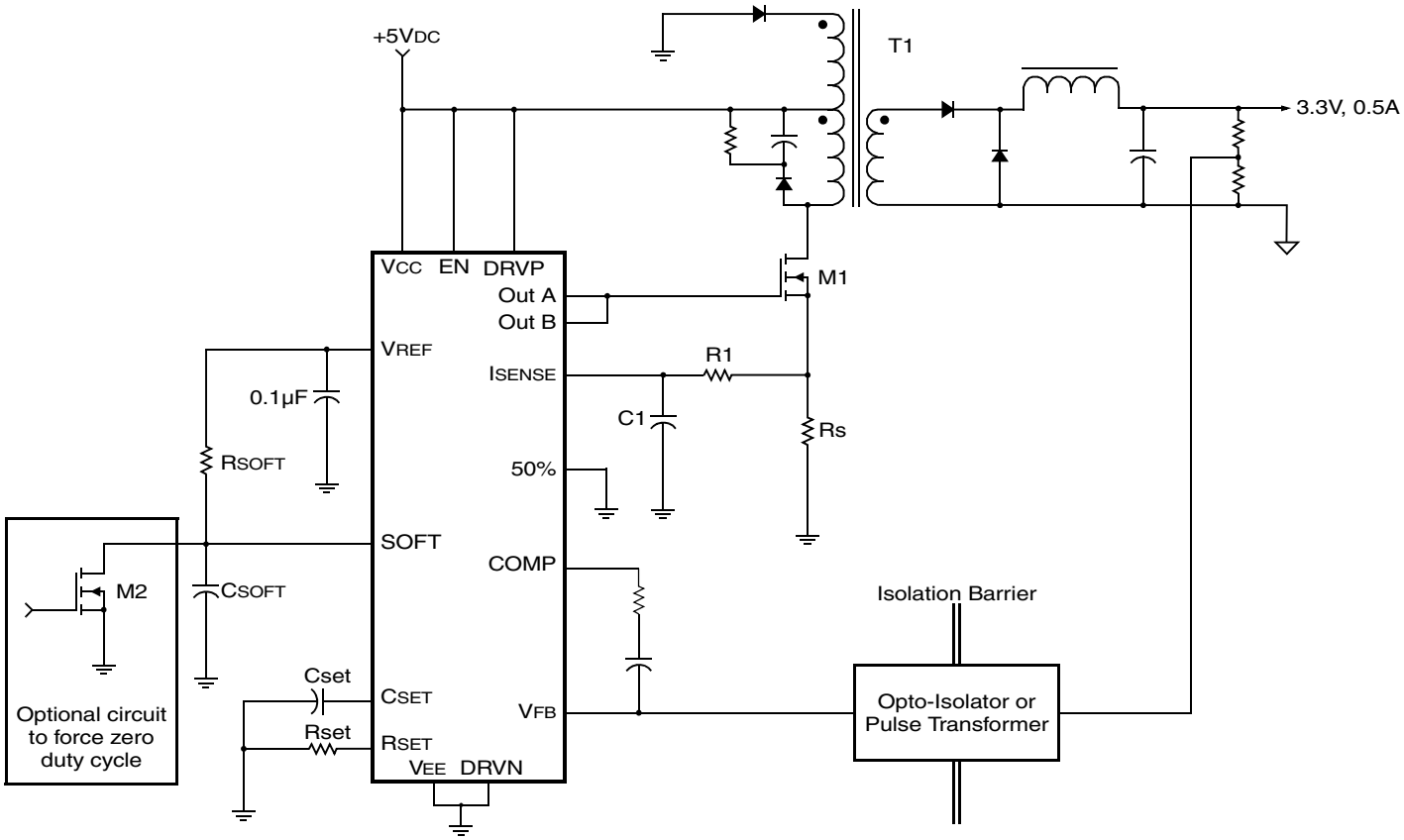


FIGURE 9 – Typical Forward Converter Application

A typical single output forward converter application is shown in Figure 9 to aid in the following operational description.

During normal operation, the oscillator jumpstarts each switching cycle by resetting the RS latch, causing the output stage to go high and turn on M1. Current begins to build linearly through T1 and M1 and a proportional voltage is developed across the small sense resistor Rs. Switching spikes are filtered by C1 and R1, and the resulting sawtooth waveform is passed into the PWM to serve as the current comparator input. Meanwhile, a portion of the output voltage is sensed and compared to the PWM's internal precision 2.5V reference. The difference is then amplified and level shifted to serve as the comparator threshold. When the voltage on the ISENSE pin exceeds this threshold, the comparator fires and resets the latch. The output then turns off until the beginning of the next oscillator cycle when the process repeats.

Like all current mode PWMs, the chip provides built in fault protection by limiting peak switch current on a cycle by cycle basis. When an overload condition occurs, the sensed current reaches the current trip threshold earlier in the switching cycle than it otherwise would and thus forces the PWM latch off until the start of the next cycle. The process repeats until the overload condition is removed and the PWM can return to a normal duty cycle. The chip is capable of operating in this mode indefinitely without sustaining damage.

There are two ways to set the current limit trip point. One is to simply tailor the sense resistor Rs:

$$I_{pk} = \frac{1.0Vdc}{R_s}$$

Some users may find the power is dissipated in Rs to be unacceptably high. In this case, the user can fix Rs at a small value and vary the current comparator threshold instead. Fortunately, the PWM chip provides a very convenient method for doing so. Because the error amplifier output is internally clamped to the SOFT pin, the user need simply apply the desired voltage level to the SOFT pin to arbitrarily lower the current comparator threshold.

Recalling that the EA output is level shifted and divided before being applied to the comparator input, the peak current limit is chosen by applying a voltage VSOFT such that:

$$I_{pk} = \frac{V_{soft} - 1.4}{3 \times R_s} \qquad 1.4V \le V_{soft} \le 4.4V$$

Clamping the EA output to the soft pin also makes implementing a softstart ciruit easy. Rsoft and Csoft are connected as in Figure 9 to provide the SOFT pin an asymptotically rising voltage. Because of the internal clamp on the EA output, the PWM duty cycle will increase only as fast as the chosen time constant will allow. In this way, excessive duty cycle and surge currents into the output capacitors are avoided. A transistor may be optionally connected across the softstart capacitor to force zero duty cycle on command. This is a particularly convenient method for implementing an externally controlled turn-on delay.

The discussion so far assumes the user operates the chip in the current mode: switch current is sensed and compared to the error between the output voltage and a precision reference. Alternatively, the user may wish to implement voltage mode control in which the control loop is dependent only on the output voltage. The PWM chip readily supports this configuration with the following modification:

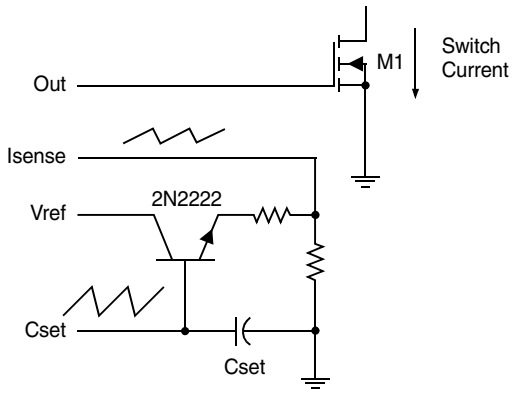


FIGURE 10 – Circuit for implementing voltage mode control.

A portion of the oscillator's sawtooth waveform is coupled to the ISENSE pin and becomes the input to the comparator stage. The operation is now identical to the current mode application: when the sawtooth voltage exceeds the amplified difference between the output and a voltage reference, the comparator fires and latches off the output until the start of the next cycle.

SELECTED APPLICATION EXAMPLES

The flexibility and performance of the chip makes it suitable for an enormous range of power converter applications – step-up, step-down, DC-DC, AC-DC, isolated/non-isolated, and many more. This section will cover two of the more popular power converter applications for which this chip is particularly well suited although many more can be envisioned.

5V Input, 3.3V Isolated Output (Single Ended Forward Converter)

The isolated step down DC/DC converter is a staple of many satellite and aerospace systems. A common bus distributes raw primary power to various system loads which must then convert the primary to one or more low voltage secondary outputs. These outputs are filtered, regulated, and ground isolated from the primary side to keep EMI and undesired subsystem interaction at a minimum. Figure 9 is one example of a circuit that very efficiently performs this conversion. The values here were chosen to work for a 5V input and 3.3V output but the circuit topology is general enough to support an infinite variety of applications. For example, output voltages can be adjusted by changing values of just a few components. A wider input voltage range can be supported by varying the transformer's turns ratios and by proper selection of M1. Thus, a very wide range of power converter applications can be satisfied by simple variations of the circuit.

At the start of each switching cycle, the PWM output goes high and turns on M1. Energy is coupled across T1's turns ratios to the secondary side where it is caught, rectified, and filtered to produce a clean DC voltage. A sampling network on the output side feeds back a portion of the output across the isolation barrier into the error amplifier negative input.

This feedback can be accomplished in a number of different ways: pulse transformers, optocouplers, or capacitive coupling are a few methods. The compensation network may need modification depending on the feedback method chosen. The additional winding and rectifier on T1 are used to reset the transformer core after the PWM latches off M1 to prevent staircase saturation of the core.

Note the chip is powered directly from the main power bus (via a zener and current limit resistor) without the need for additional bootstrap transformer windings. This is one of the main advantages this PWM chip provides over other products. This scheme could not be implemented with other chips which draw significantly more current. On the other hand, supplying bias to our PWM chip is about as simple as it gets.

5V to 1.8V Synchronous Buck Converter

A second application is a secondary side, non-isolated synchronous buck converter. The circuit takes a high voltage (5V in this case) and steps down to a lower voltage (5V to 1.8V in this example, although as pointed out above, these values are completely adjustable with proper component selection). The distinguishing feature of this implementation is the synchronous rectification scheme used to replace the standard Schottky rectifiers for more efficient power conversion of low voltage outputs.

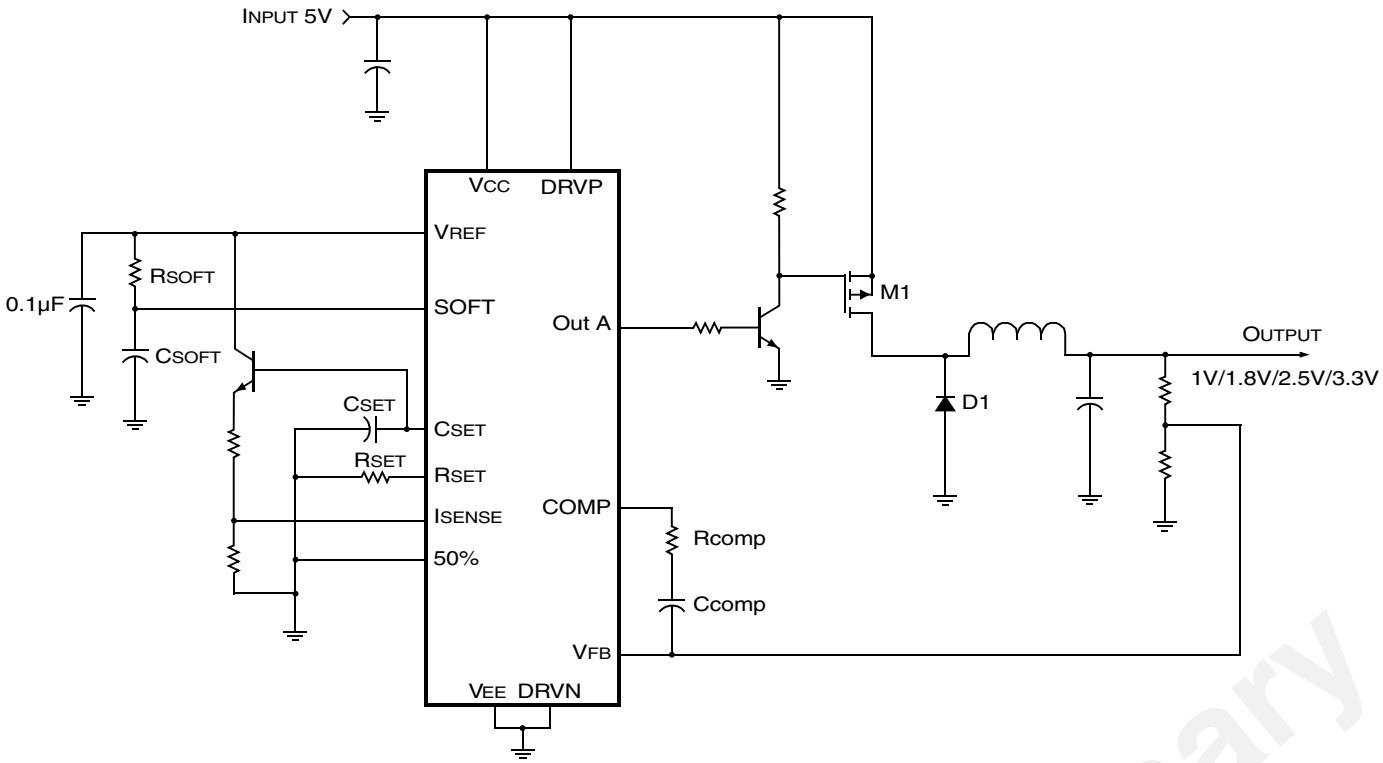


FIGURE 11 – Buck Converter

The circuit switches M1 twice per cycle, chopping the 5VDC input into a fixed frequency pulse train whose DC average is the desired output voltage. The LC filter then simply smoothes this pulse train to produce a clean DC output. The control loop regulates against operating point perturbations (temperature, line, load) by adjusting M1's duty cycle. The circuit is operated in the voltage mode since switch current is not referenced to circuit ground. Alternatively, a current transformer may be used to properly reference the ISENSE signal to permit current mode control. An inverter is needed in the output path to properly drive the P-channel MOSFET. For low current applications (less than -50mA output current), it may be possible to use the PWM's output drive stage as the switching elements and eliminate M1 and D1 altogether.

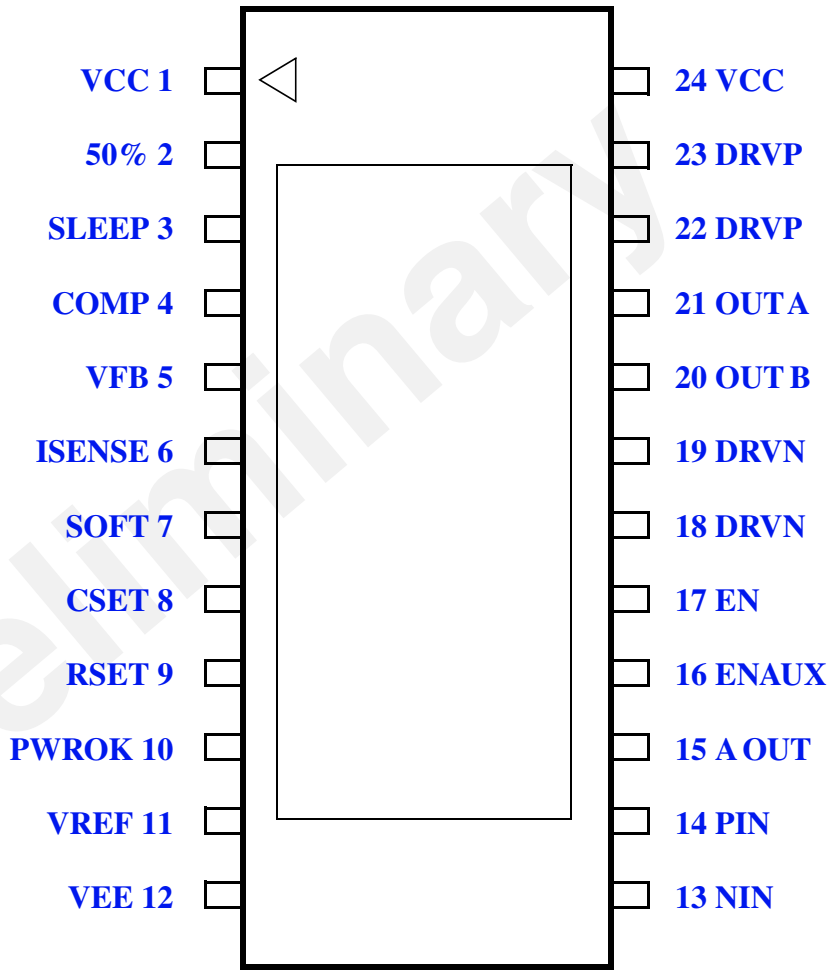


FIGURE 12 – Package Pin vs Function

CONFIGURATIONS AND ORDERING INFORMATION

MODEL NO.	SCREENING 1/	CASE
PWM5031-7	Class C	Flat Package
PWM5031-I	Class I	
PWM5031-S	Space Applications	
25A4524 (Die)	2/	Die Size – .125L x .117W inch

1. Level of screening – Class C = Commercial Flow, Commercial Temp. Range, 0°C to +70°C testing; Class I = Commercial Flow, Industrial Temp. Range, -40°C to +85°C testing; Space Applications = Military Temp. Range, Screened to the individual test methods of MIL-STD-883, -55°C to +125°C testing.
2. Each die shall be 100% visually inspected to assure conformance with the applicable die related requirements of MIL-STD-883, method 2010, cond A or cond B.

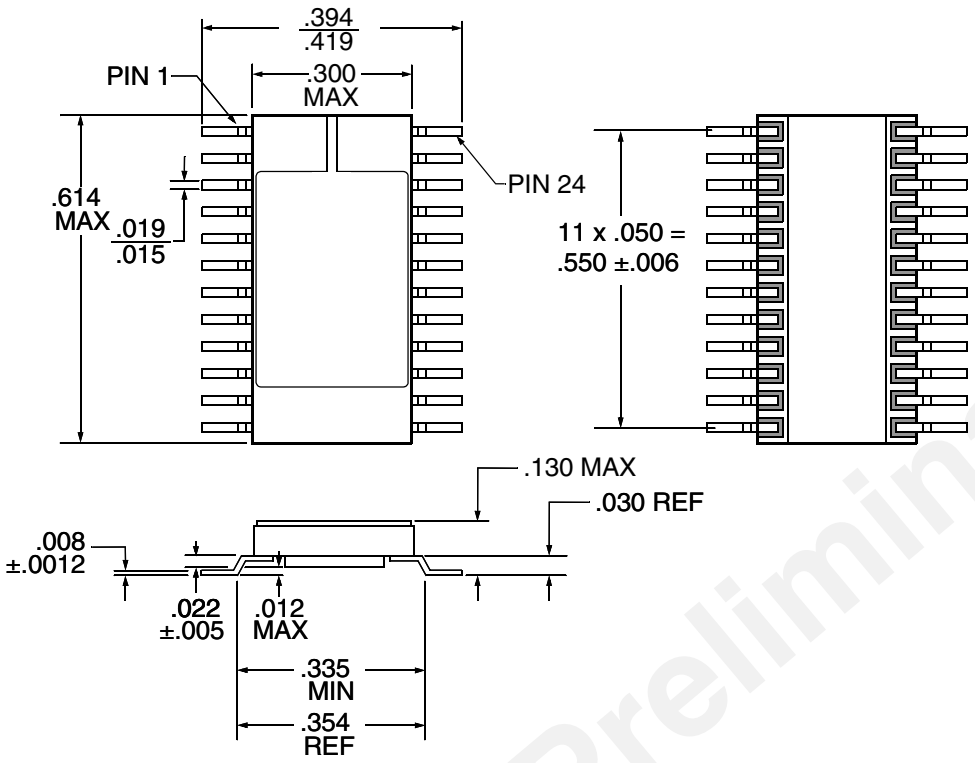


FIGURE 13 – Flat Package Configuration Outline

PLAINVIEW, NEW YORK
Toll Free: 800-THE-1553
Fax: 516-694-6715

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC
Tel: 321-951-4164
Fax: 321-951-4254

WEST COAST
Tel: 949-362-2260
Fax: 949-362-2266

CENTRAL
Tel: 719-594-8017
Fax: 719-594-8468

www.aeroflex.com info-ams@aeroflex.com