Obsolete Device

28C04A

4K (512 x 8) CMOS EEPROM

FEATURES

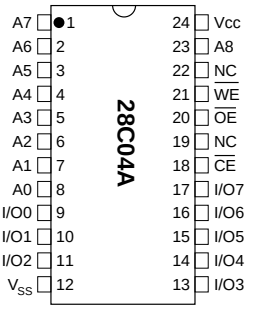
- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >200 years
- Endurance - Minimum 10^4 Erase/Write Cycles
  - Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Chip Clear Operation
- Enhanced Data Protection
  - V_{CC} Detector
  - Pulse Filter
  - Write Inhibit
- 5-Volt-Only Operation
- Organized 512x8 JEDEC standard pinout
  - 24-pin Dual-In-Line Package
  - 32-pin PLCC Package
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

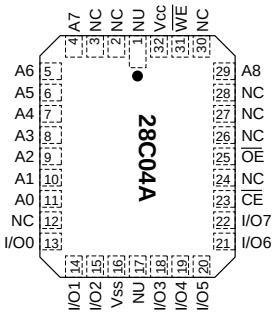
The Microchip Technology Inc. 28C04A is a CMOS 4K non-volatile electrically Erasable and Programmable Read Only Memory (EEPROM). The 28C04A is accessed like a static RAM for the read or write cycles without the need of external components. During a “byte write”, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C04A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPES

DIP

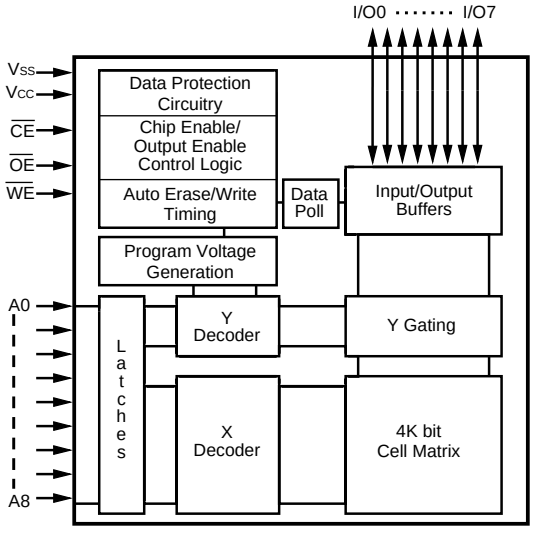


PLCC



• Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

V_{CC} and input voltages w.r.t. V_{SS} ..... -0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. V_{SS}..... -0.6V to +13.5V

Output Voltage w.r.t. V_{SS} ..... -0.6V to V_{CC}+0.6V

Storage temperature ..... -65°C to +125°C

Ambient temp. with power applied ..... -50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A8	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

			V_{CC} = +5V ±10% Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic '1' Logic '0'	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = -0.1V to V_{CC}+1
Input Capacitance		C_{IN}		10	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic '1' Logic '0'	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
Output Leakage		I_{LO}	-10	10	µA	V_{OUT} = -0.1V TO V_{CC} + 0.1V
Output Capacitance		C_{OUT}		12	pF	V_{IN} = 0V; T_{AMB} = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	I_{CC}		30	mA	f = 5 MHz (Note 1) V_{CC} = 5.5V
Power Supply Current, Standby	TTL input TTL input CMOS input	$I_{CC(S)TTL}$ $I_{CC(S)TTL}$ $I_{CC(S)CMOS}$		2 3 100	mA mA µA	$\overline{CE}$ = V_{IH} (0°C to +70°C) $\overline{CE}$ = V_{IH} (-40°C to +85°C) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1 $\overline{OE}$ = V_{CC} All inputs equal V_{CC} or V_{SS}

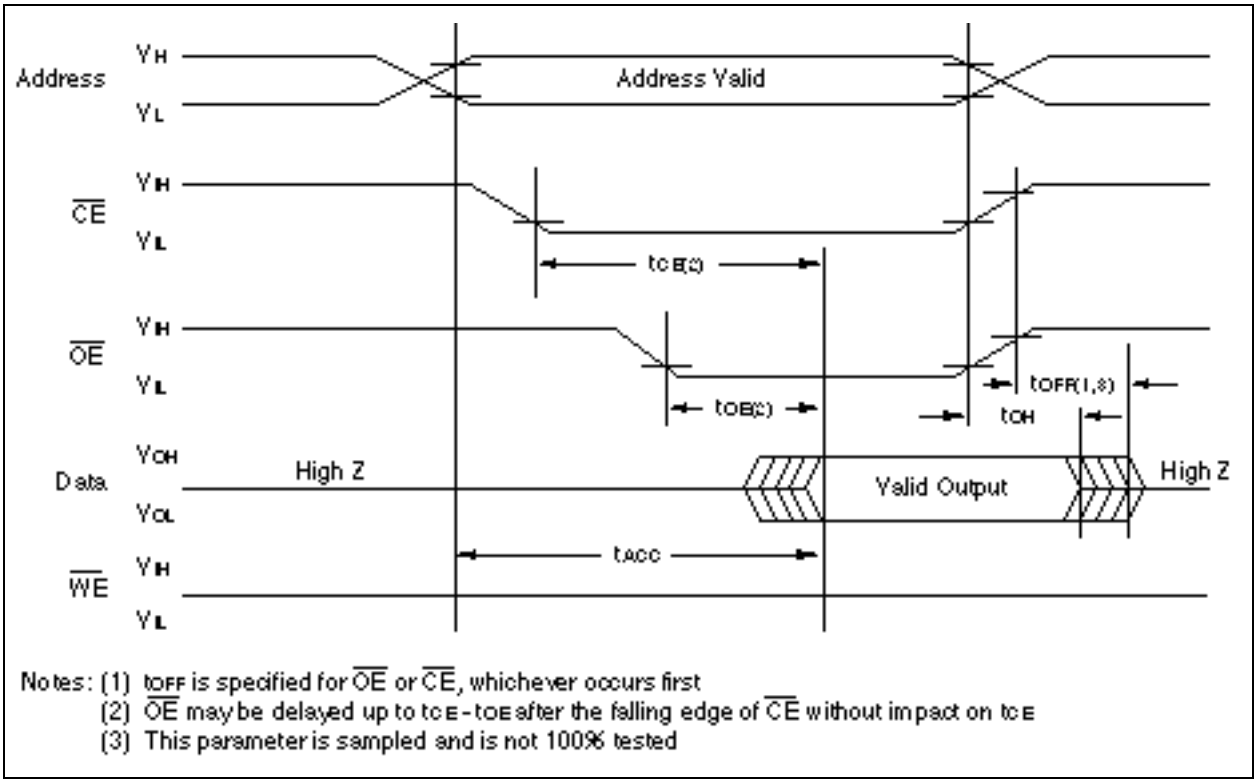
Note 1: AC power supply current above 5 MHz; 1 mA/MHz.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

	AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 20 ns Ambient Temperature: Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C								
Parameter	**Sym**	**28C04A-15**		**28C04A-20**		**28C04A-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ to $\overline{OE}$ High Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t_{OH}	0		0		0		ns	
Endurance	—	1M	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note)

Note: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V			
	Output Load:	1 TTL Load + 100 pF			
	Input Rise/Fall Times:	20 nsec			
	Ambient Temperature:	Commercial (C): Tamb= 0°C to 70°C Industrial (I): Tamb= -40°C to 85°C			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Write Cycle Time (28C04A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C04AF)	t_{WC}		200	µs	100 µs typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS

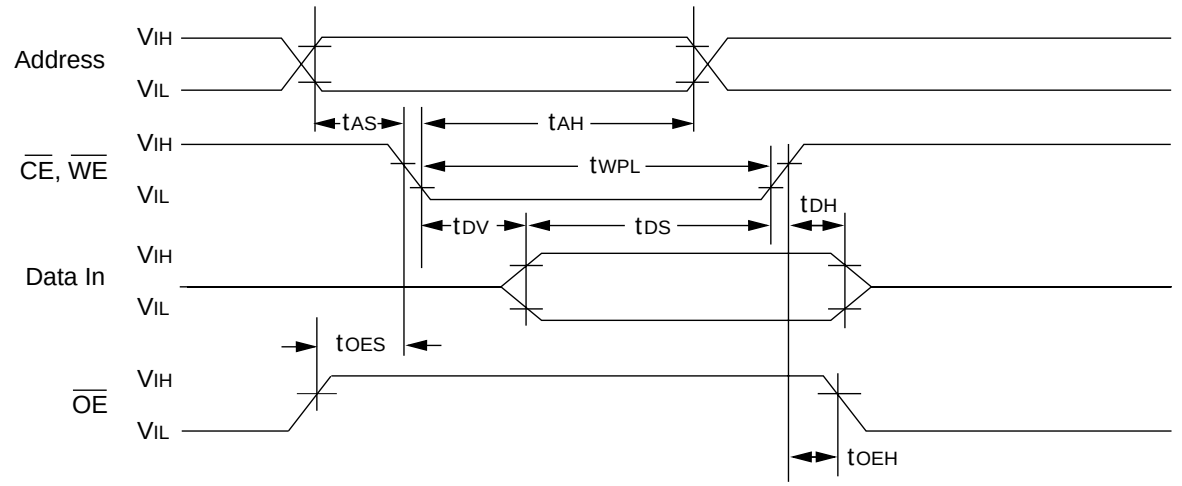


FIGURE 1-3: $\overline{\text{DATA}}$ POLLING WAVEFORMS

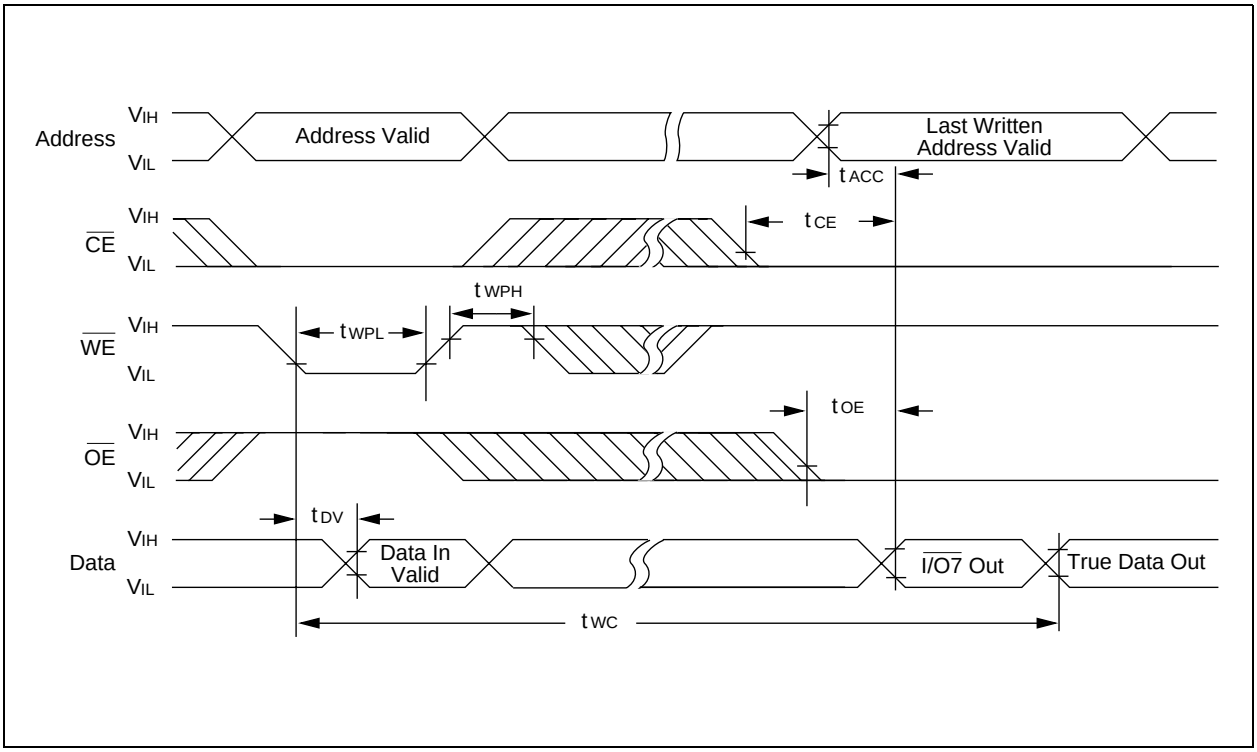
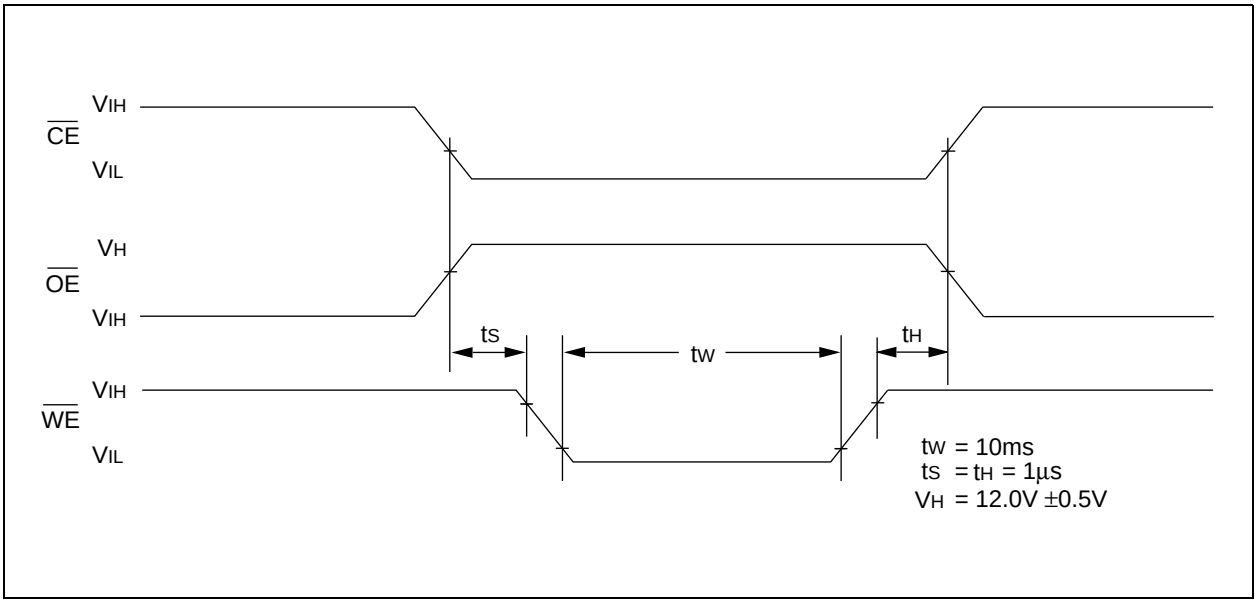


FIGURE 1-4: CHIP CLEAR WAVEFORMS



2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C04A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{IE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each “Write”			

X = Any TTL level.

2.1 Read Mode

The 28C04A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

2.2 Standby Mode

The 28C04A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

2.4 Write Mode

The 28C04A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

2.5 Data Polling

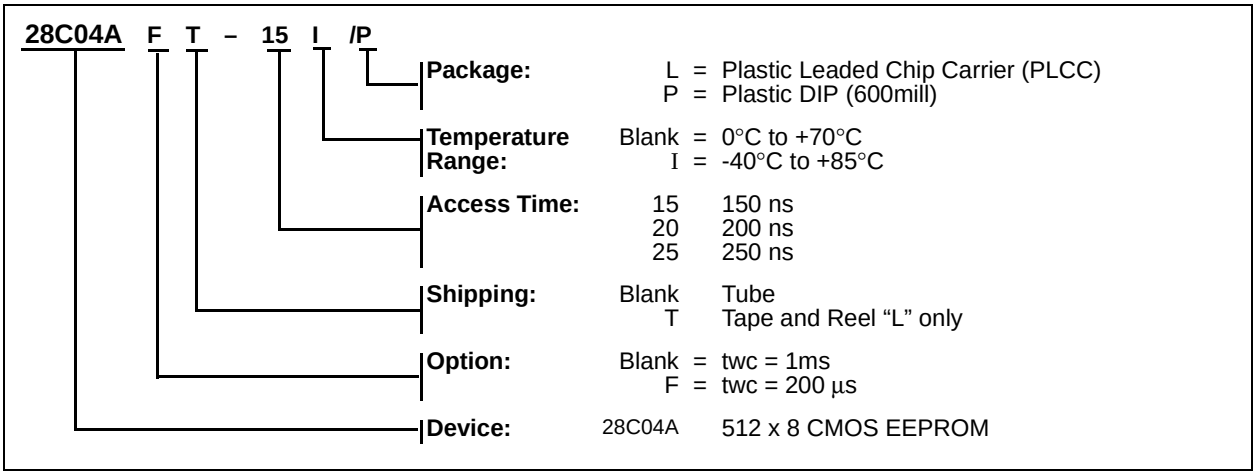
The 28C04A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data.

28C04A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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