SEE NEW DESIGN RECOMMENDATIONS

REFERENCE ONLY

2-MBIT SmartVoltage BOOT BLOCK FLASH MEMORY FAMILY

28F200BV-T/B, 28F200CV-T/B, 28F002BV-T/B

- **Intel SmartVoltage Technology**
  - **5 V or 12 V Program/Erase**
  - **3.3 V or 5 V Read Operation**
- **Very High-Performance Read**
  - **5 V: 60 ns Access Time**
  - **3 V: 110 ns Access Time**
- **Low Power Consumption**
  - **Max 60 mA Read Current at 5 V**
  - **Max 30 mA Read Current at 3.3 V–3.6 V**
- **x8/x16-Selectable Input/Output Bus**
  - **28F200 for High Performance 16- or 32-bit CPUs**
- **x8-Only Input/Output Architecture**
  - **28F002B for Space-Constrained 8-bit Applications**
- **Optimized Array Blocking Architecture**
  - **One 16-KB Protected Boot Block**
  - **Two 8-KB Parameter Blocks**
  - **96-KB and 128-KB Main Blocks**
  - **Top or Bottom Boot Locations**
- **Extended Temperature Operation**
  - **–40 °C to +85 °C**
- **Extended Block Erase Cycling**
  - **100,000 Cycles at Commercial Temp**
  - **10,000 Cycles at Extended Temp**
- **Automated Word/Byte Program and Block Erase**
  - **Command User Interface**
  - **Status Registers**
  - **Erase Suspend Capability**
- **SRAM-Compatible Write Interface**
- **Automatic Power Savings Feature**
- **Reset/Deep Power-Down Input**
  - **0.2 µA I_{CC} Typical**
  - **Provides Reset for Boot Operations**
- **Hardware Data Protection Feature**
  - **Absolute Hardware-Protection for Boot Block**
  - **Write Lockout during Power Transitions**
- **Industry-Standard Surface Mount Packaging**
  - **40-, 48-, 56-Lead TSOP**
  - **44-Lead PSOP**
- **Footprint Upgradeable to 4-Mbit and 8-Mbit Boot Block Flash Memories**
- **ETOX™ IV Flash Technology**

New Design Recommendations:

For new 2.7 V–3.6 V V_{CC} designs with this device, Intel recommends using the Smart 3 Advanced Boot Block. Reference *Smart 3 Advanced Boot Block 4-Mbit, 8-Mbit, 16-Mbit Flash Memory Family* datasheet, order number 290580.

For new 5 V V_{CC} designs with this device, Intel recommends using the 2-Mbit Smart 5 Boot Block. Reference *Smart 5 Flash Memory Family 2, 4, 8 Mbit* datasheet, order number 290599.

These documents are also available at Intel's website, http://www.intel.com/design/flcomp.

December 1997 Order Number: 290531-005

Intel Corporation
P.O. Box 5937
Denver, CO 8021-9808

or call 1-800-548-4725
or visit Intel's website at http://www.intel.com

 CG-041493

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REVISION HISTORY

Number	Description
-001	Initial release of datasheet.
-002	Status changed from Product Preview to Preliminary 28F200CV/CE/BE references and information added throughout. 2.7 V CE/BE specs added throughout. The following sections have been changed or rewritten: 1.1, 3.0, 3.2.1, 3.2.2, 3.3.1, 3.3.1.1, 3.3.2, 3.3.2.1, 3.3.3, 3.3.4, 3.6.2. Note 2 added to Figure 3 to clarify 28F008B pinout vs. 28F008SA. Sentence about program and erase WSM timeout deleted from Section 3.3.3, 3.3.4. Erroneous arrows leading out of error states deleted from flowcharts in Figs. 9, 10. Sections 5.1, 6.1 changed to "Applying V_{CC} Voltages." These sections completely changed to clarify V_{CC} ramp requirements. I_{PPD} 3.3 V Commercial spec changed from 10 to 5 µA. Capacitance tables added after commercial and extended DC Characteristics tables. Test and slew rate notes added to Figs. 12, 13, 19, 20, 21. Test configuration drawings (Fig. 14, 22) consolidated into one, with component values in table. (Component values also rounded off). t_{ELFL}, t_{ELFH}, t_{AVFL} changed from 7 to 5 ns for 3.3 V BV-60 commercial and 3.3 V TBV-80 extended, 10 to 5 ns for 3.3 V BV-80 and BV-120 commercial. t_{WHAX} and t_{EHAX} changed from 10 to 0 ns. t_{PHWL} changed from 1000 ns to 800 ns for 3.3 V BV-80, BV-120 commercial. t_{PHEL} changed from 1000 ns to 800 ns for 3.3 V BV-60, BV-80, and BV-120 commercial.
-003	Applying V_{CC} voltages (Sections 5.1 and 6.1) rewritten for clarity. Minor cosmetic changes/edits.
-004	Corrections: "This pin not available on 44-PSOP" inaccurate statement removed from pin description for WP# pin; Spec "t_{QWL}" corrected to "$t_{QVVL;}$" intelligent identifier values corrected; Intel386™ EX block diagram updated because new 386 specs require less glue logic. Max program times for parameter and 96-KB main block added. Specs t_{ELFL} and t_{ELFH} changed from 5 ns (max) to 0 ns (min). Specs t_{EHQZ} and t_{HQZ} improved. New specs t_{PLPH} and t_{PLQZ} added from Specification Update document (297612).
-005	Corrections: Figure 4, corrected pin designation 3 to "NC" from A_{17} on PA28F200. Corrected typographical errors in *Ordering Information*. Added *New Design Recommendations* section to cover page. Updated *Erase Suspend/Resume Flowchart*

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1.0 PRODUCT FAMILY OVERVIEW

This datasheet contains the specifications for the two branches of products in the SmartVoltage 2-Mbit boot block flash memory family. These -BV/CV suffix products offer 3.0 V–3.6 V operation and also operate at 5 V for high-speed access times. Throughout this datasheet, the 28F200 refers to all x8/x16 2-Mbit products, while 28F002B refers to all x8 2-Mbit boot block products. Section 1.0 provides an overview of the flash memory family including applications, pinouts and pin descriptions. Sections 2.0 and 3.0 describe the memory organization and operation for these products. Section 4.0 contains the family's operating specifications. Finally, Sections 5.0 and 6.0 provide ordering and document reference information.

1.1 New Features in the SmartVoltage Products

The SmartVoltage boot block flash memory family offers identical operation with the BX/BL 12 V program products, except for the differences listed below. All other functions are equivalent to current products, including signatures, write commands, and pinouts.

- WP# pin has replaced a DU (Don't Use) pin. Connect the WP# pin to control signal or to V_{CC} or GND (in this case, a logic-level signal can be placed on DU pin). Refer to Tables 2 and 9 to see how the WP# pin works.
- 5 V program/erase operation has been added. If switching V_{PP} for write protection, switch to GND (not 5 V) for complete write protection. To take advantage of 5 V write-capability, allow for connecting 5 V to V_{PP} and disconnecting 12 V from V_{PP} line.
- Enhanced circuits optimize low V_{CC} performance, allowing operation down to V_{CC} = 3.0 V.

If you are using BX/BL 12 V V_{PP} boot block products today, you should account for the differences listed above and also allow for connecting 5 V to V_{PP} and disconnecting 12 V from V_{PP} line, if 5 V writes are desired.

1.2 Main Features

Intel's SmartVoltage technology is the most flexible voltage solution in the flash industry, providing two discrete voltage supply pins: V_{CC} for read operation, and V_{PP} for program and erase operation. Discrete supply pins allow system designers to use the optimal voltage levels for their design. This product family, specifically the 28F200BV/CV, and 28F002BV provide program/erase capability at 5 V or 12 V. The 28F200BV/CV and 28F002BV allow reads with V_{CC} at 3.3 V ± 0.3 V or 5 V. Since many designs read from the flash memory a large percentage of the time, read operation using the 3.3 V ranges can provide great power savings. If read performance is an issue, however, 5 V V_{CC} provides faster read access times.

For program and erase operations, 5 V V_{PP} operation eliminates the need for in system voltage converters, while 12 V V_{PP} operation provides faster program and erase for situations where 12 V is available, such as manufacturing or designs where 12 V is in-system. For design simplicity, however, just hook up V_{CC} and V_{PP} to the same 5 V ± 10% source.

The 28F200/28F002B boot block flash memory family is a high-performance, 2-Mbit (2,097,152 bit) flash memory family organized as either 256 Kwords of 16 bits each (28F200 only) or 512 Kbytes of 8 bits each (28F200 and 28F002B).

Table 1. SmartVoltage Provides Total Voltage Flexibility

Product Name	Bus Width	V_{CC}		V_{PP}	
		3.3 V ± 0.3 V	**5 V ± 5% 5 V ± 10%**	**5 V ± 10%**	**12 V ± 5%**
28F002BV-T/B	x8	√	√	√	√
28F200BV-T/B	x8 or x16	√	√	√	√
28F200CV-T/B	x8 or x16	√	√	√	√

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Separately erasable blocks, including a hardware-lockable boot block (16,384 bytes), two parameter blocks (8,192 bytes each) and main blocks (one block of 98,304 bytes and one block of 131,072 bytes), define the boot block flash family architecture. See Figures 7 and 8 for memory maps. Each block can be independently erased and programmed 100,000 times at commercial temperature or 10,000 times at extended temperature.

The boot block is located at either the top (denoted by **-T** suffix) or the bottom (**-B** suffix) of the address map in order to accommodate different microprocessor protocols for boot code location. The hardware-lockable boot block provides complete code security for the kernel code required for system initialization. Locking and unlocking of the boot block is controlled by WP# and/or RP# (see Section 3.4 for details).

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the boot block flash memory products. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations, including verifications, thereby unburdening the microprocessor or microcontroller of these tasks. The Status Register (SR) indicates the status of the WSM and whether it successfully completed the desired program or erase operation.

Program and Erase Automation allows program and erase operations to be executed using an industry-standard two-write command sequence to the CUI. Data programming is performed in word (28F200 family) or byte (28F200 or 28F002B families) increments. Each byte or word in the flash memory can be programmed independently of other memory locations, unlike erases, which erase all locations within a block simultaneously.

The 2-Mbit SmartVoltage boot block flash memory family is also designed with an Automatic Power Savings (APS) feature which minimizes system battery current drain, allowing for very low power designs. To provide even greater power savings, the boot block family includes a deep power-down mode which minimizes power consumption by turning most of the flash memory's circuitry off. This mode is controlled by the RP# pin and its usage is discussed in Section 3.5, along with other power consumption issues.

Additionally, the RP# pin provides protection against unwanted command writes due to invalid system bus conditions that may occur during system reset and power-up/down sequences. For example, when the flash memory powers-up, it automatically defaults to the read array mode, but during a warm system reset, where power continues uninterrupted to the system components, the flash memory could remain in a non-read mode, such as erase. Consequently, the system Reset signal should be tied to RP# to reset the memory to normal read mode upon activation of the Reset signal. See Section 3.6.

The 28F200 provides both byte-wide or word-wide input/output, which is controlled by the BYTE# pin. Please see Table 2 and Figure 16 for a detailed description of BYTE# operations, especially the usage of the DQ_{15}/A_{-1} pin.

The 28F200 products are available in a ROM/EPROM-compatible pinout and housed in the 44-lead PSOP (Plastic Small Outline) package, the 48-lead TSOP (Thin Small Outline, 1.2 mm thick) package and the 56-lead TSOP as shown in Figures 4, 5 and 6, respectively. The 28F002 products are available in the 40-lead TSOP package as shown in Figure 3.

Refer to the *DC Characteristics*, Section 4.4 (commercial temperature) and Section 4.11 (extended temperature), for complete current and voltage specifications. Refer to the *AC Characteristics*, Section 4.5 (commercial temperature) and Section 4.12 (extended temperature), for read, write and erase performance specifications.

1.3 Applications

The 2-Mbit boot block flash memory family combines high-density, low-power, high-performance, cost-effective flash memories with blocking and hardware protection capabilities. Their flexibility and versatility reduce costs throughout the product life cycle. Flash memory is ideal for Just-In-Time production flow, reducing system inventory and costs, and eliminating component handling during the production phase.

When your product is in the end-user's hands, and updates or feature enhancements become necessary, flash memory reduces the update costs by allowing user-performed code changes instead of costly product returns or technician calls.

The 2-Mbit boot block flash memory family provides full-function, blocked flash memories suitable for a wide range of applications. These applications include extended PC BIOS and ROM-able applications storage, digital cellular phone program and data storage, telecommunication boot/firmware, printer firmware/font storage and various other embedded applications where program and data storage are required.

Reprogrammable systems, such as personal computers, are ideal applications for the 2-Mbit flash memory products. Increasing software sophistication greatens the probability that a code update will be required after the PC is shipped. For example, the emerging of “plug and play” standard in desktop and portable PCs enables auto-configuration of ISA and PCI add-in cards. However, since the plug and play specification continues to evolve, a flash BIOS provides a cost-effective capability to update existing PCs. In addition, the parameter blocks are ideal for storing the required auto-configuration parameters, allowing you to integrate the BIOS PROM and parameter storage EEPROM into a single component, reducing parts costs while increasing functionality.

The 2-Mbit flash memory products are also excellent design solutions for digital cellular phone and telecommunication switching applications requiring very low power consumption, high-performance, high-density storage capability, modular software designs, and a small form factor package. The 2-Mbit’s blocking scheme allows for easy segmentation of the embedded code with 16 Kbytes of hardware-protected boot code, four main blocks of program code and two parameter blocks of 8 Kbytes each for frequently updated data storage and diagnostic messages (e.g., phone numbers, authorization codes).

Intel’s boot block architecture provides a flexible voltage solution for the different design needs of various applications. The asymmetrically-blocked memory map allows the integration of several memory components into a single flash device. The boot block provides a secure boot PROM; the parameter blocks can emulate EEPROM functionality for parameter store with proper software techniques; and the main blocks provide code and data storage with access times fast enough to execute code in place, decreasing RAM requirements.

1.4 Pinouts

Intel’s SmartVoltage Boot Block architecture provides upgrade paths in every package pinout to the 4 or 8-Mbit density. The 28F002B 40-lead TSOP pinout for space-constrained designs is shown in Figure 3. The 28F200 44-lead PSOP pinout follows the industry-standard ROM/EPROM pinout, as shown in Figure 4. For designs that require x16 operation but have space concerns, refer to the 48-lead pinout in Figure 5. Furthermore, the 28F200 56-lead TSOP pinout shown in Figure 6 provides compatibility with BX/BL family product packages.

Pinouts for the corresponding 4-Mbit and 8-Mbit components are also provided for convenient reference. 2-Mbit pinouts are given on the chip illustration in the center, with 4-Mbit and 8-Mbit pinouts going outward from the center.

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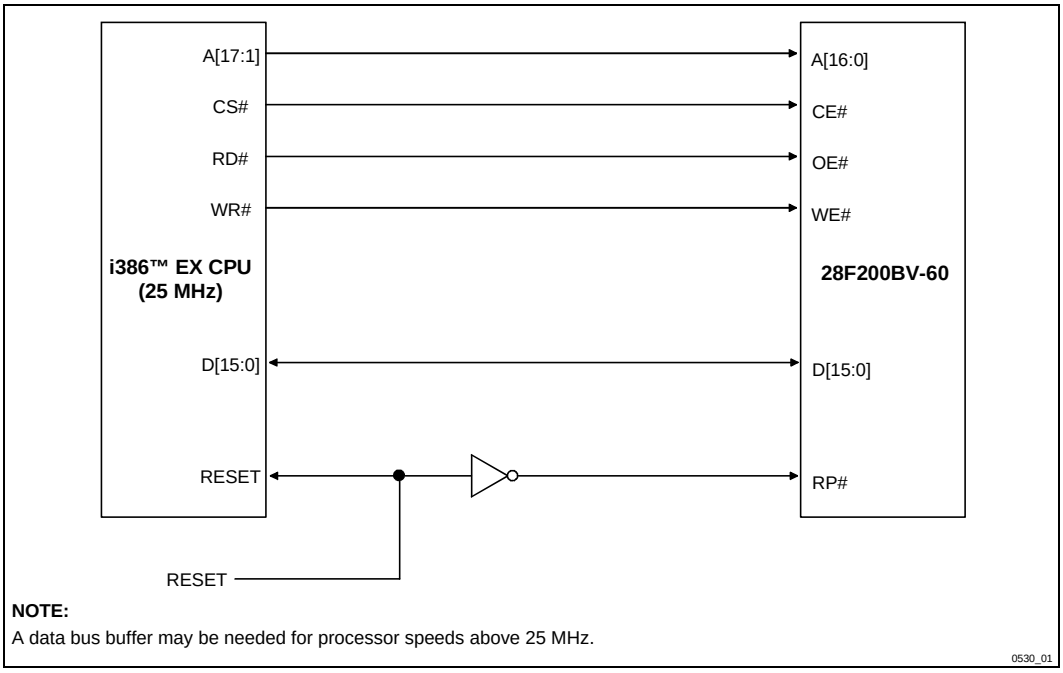


NOTE:
A data bus buffer may be needed for processor speeds above 25 MHz.

Figure 1. 28F200 Interface to Intel386™ EX Microprocessor

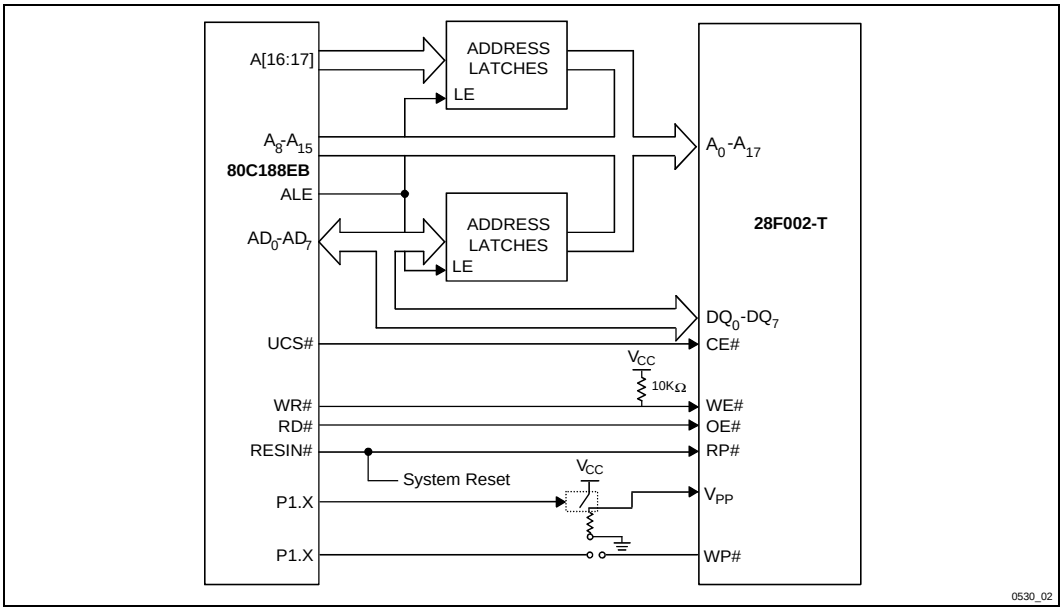


Figure 2. 28F002B Interface to Intel80C188EB 8-Bit Embedded Microprocessor

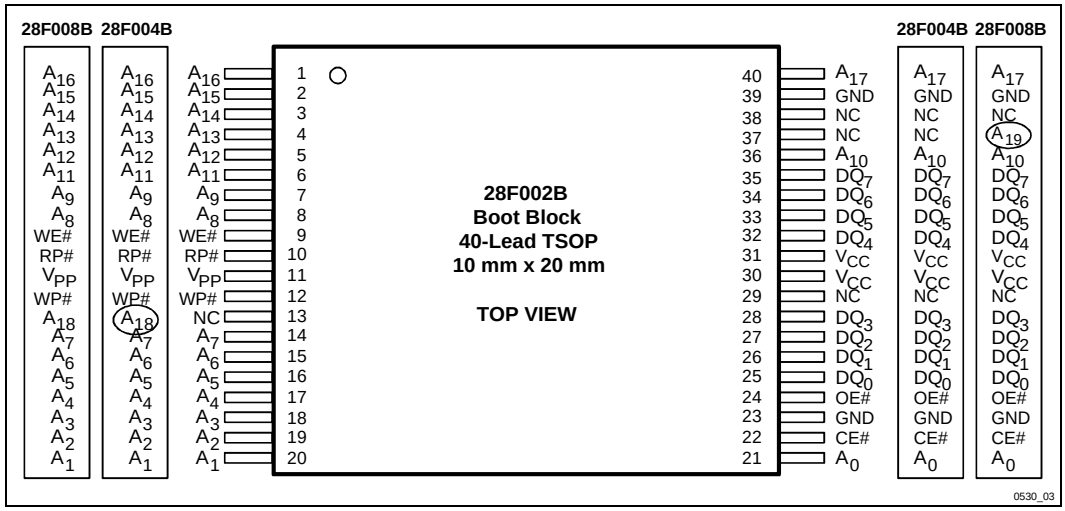
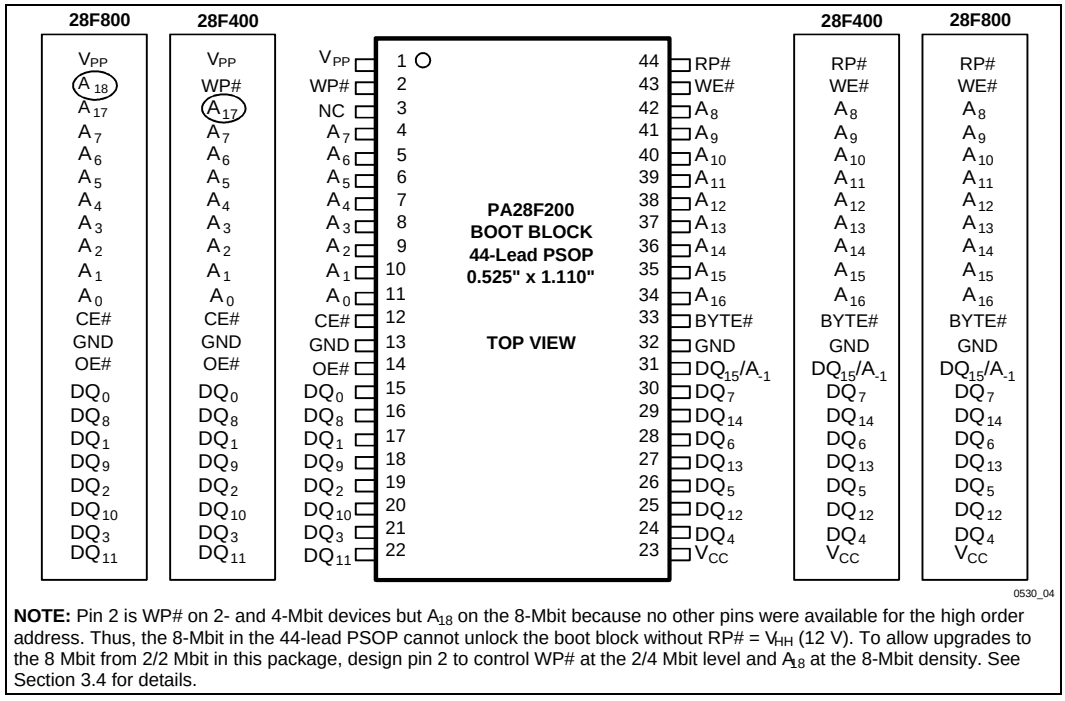


Figure 3. The 40-Lead TSOP Offers the Smallest Form Factor for Space-Constrained Applications



NOTE: Pin 2 is WP# on 2- and 4-Mbit devices but A_{18} on the 8-Mbit because no other pins were available for the high order address. Thus, the 8-Mbit in the 44-lead PSOP cannot unlock the boot block without RP# = V_{HH} (12 V). To allow upgrades to the 8 Mbit from 2/2 Mbit in this package, design pin 2 to control WP# at the 2/4 Mbit level and A_{18} at the 8-Mbit density. See Section 3.4 for details.

Figure 4. The 44-Lead PSOP Offers a Convenient Upgrade from JEDEC ROM Standards

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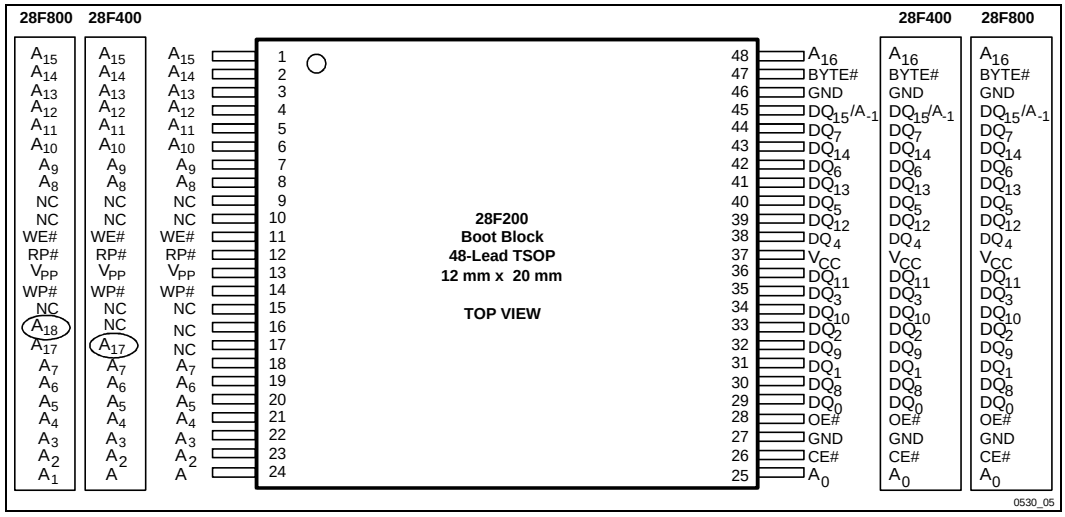

Figure 5. The 48-Lead TSOP Offers the Smallest Form Factor for x16 Operation

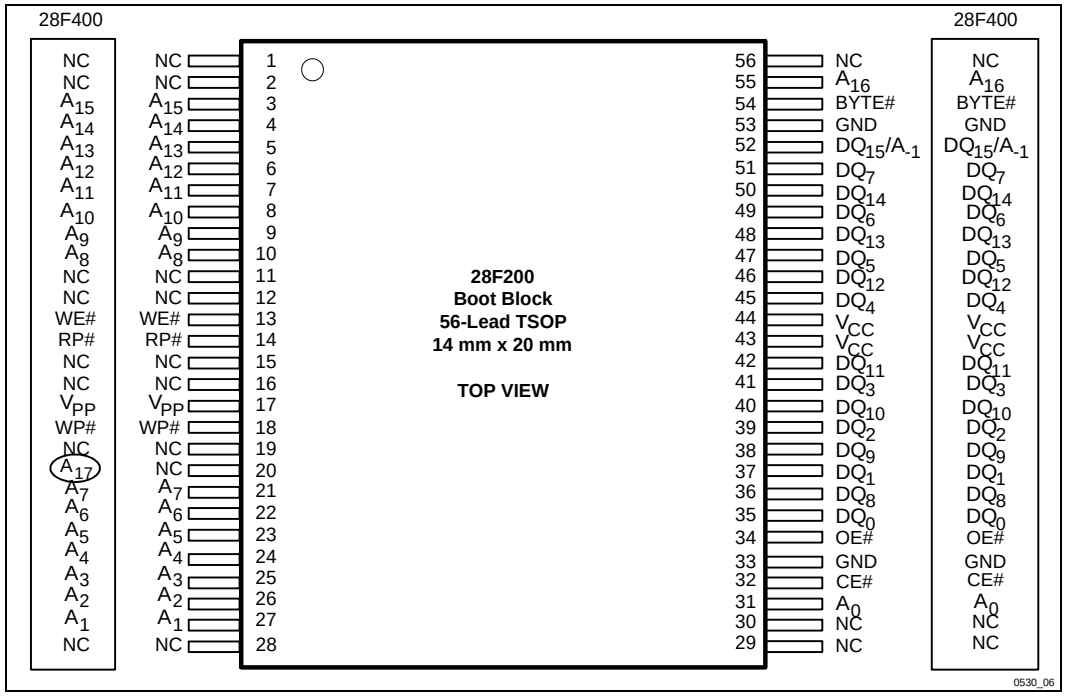

Figure 6. The 56-Lead TSOP Offers Compatibility between 2 and 4 Mbits

SEE NEW DESIGN RECOMMENDATIONS

1.5 Pin Descriptions

Table 2. 28F200/002 Pin Descriptions

Symbol	Type	Name and Function
A_0–A_{17}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle. **The 28F200 only has A_0– A_{16} pins, while the 28F002B has A_0– A_{17}.**
A_9	INPUT	**ADDRESS INPUT:** When A_9 is at V_{HH} the signature mode is accessed. During this mode, A_0 decodes between the manufacturer and device IDs. When BYTE# is at a logic low, only the lower byte of the signatures are read. DQ_{15}/A_{-1} is a don't care in the signature mode when BYTE# is low.
DQ_0–DQ_7	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched during the write cycle. Outputs array, Intelligent Identifier and status register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
DQ_8–DQ_{15}	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched during the write cycle. Outputs array data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled as in the byte-wide mode (BYTE# = "0"). In the byte-wide mode DQ_{15}/A_{-1} becomes the lowest order address for data output on DQ_0–DQ_7. **The 28F002B does not include these DQ_8–DQ_{15} pins.**
CE#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels. If CE# and RP# are high, but not at a CMOS high level, the standby current will increase due to current flow through the CE# and RP# input stages.
OE#	INPUT	**OUTPUT ENABLE:** Enables the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the Command Register and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Uses three voltage levels (V_{IL}, V_{IH}, and V_{HH}) to control two different functions: reset/deep power-down mode and boot block unlocking. It is backwards-compatible with the BX/BL/BV products. **When RP# is at logic low, the device is in reset/deep power-down mode**, which puts the outputs at High-Z, resets the Write State Machine, and draws minimum current. **When RP# is at logic high, the device is in standard operation**. When RP# transitions from logic-low to logic-high, the device defaults to the read array mode. **When RP# is at V_{HH}, the boot block is unlocked** and can be programmed or erased. This overrides any control from the WP# input.

SEE NEW DESIGN RECOMMENDATIONS

Table 2. 28F200/002 Pin Descriptions

Symbol	Type	Name and Function
WP#	INPUT	**WRITE PROTECT:** Provides a method for unlocking the boot block in a system without a 12 V supply. **When WP# is at logic low, the boot block is locked**, preventing program and erase operations to the boot block. If a program or erase operation is attempted on the boot block when WP# is low, the corresponding status bit (bit 4 for program, bit 5 for erase) will be set in the status register to indicate the operation failed. **When WP# is at logic high, the boot block is unlocked** and can be programmed or erased. **NOTE:** This feature is overridden and the boot block unlocked when RP# is at V_{HH}. See Section 3.4 for details on write protection.
BYTE#	INPUT	**BYTE# ENABLE: Not available on 28F002B**. Controls whether the device operates in the byte-wide mode (x8) or the word-wide mode (x16). BYTE# pin must be controlled at CMOS levels to meet the CMOS current specification in the standby mode. **When BYTE# is at logic low, the byte-wide mode is enabled**, where data is read and programmed on DQ_0–DQ_7 and DQ_{15}/A_{-1} becomes the lowest order address that decodes between the upper and lower byte. DQ_8–DQ_{14} are tri-stated during the byte-wide mode. **When BYTE# is at logic high, the word-wide mode is enabled**, where data is read and programmed on DQ_0–DQ_{15}.
V_{CC}		**DEVICE POWER SUPPLY:** 5.0 V ± 10%, 3.3 V ± 0.3 V, 2.7 V–3.6 V (BE/CE only)
V_{PP}		**PROGRAM/ERASE POWER SUPPLY:** For erasing memory array blocks or programming data in each block, a voltage either of 5 V ± 10% or 12 V ± 5% must be applied to this pin. When $V_{PP} < V_{PPLK}$ all blocks are locked and protected against Program and Erase commands.
GND		**GROUND:** For all internal circuitry.
NC		**NO CONNECT:** Pin may be driven or left floating.

2.0 PRODUCT DESCRIPTION

2.1 Memory Blocking Organization

This product family features an asymmetrically-blocked architecture providing system memory integration. Each erase block can be erased independently of the others up to 100,000 times for commercial temperature or up to 10,000 times for extended temperature. The block sizes have been chosen to optimize their functionality for common applications of nonvolatile storage. The combination of block sizes in the boot block architecture allow the integration of several memories into a single chip. For the address locations of the blocks, see the memory maps in Figures 4 and 5.

2.1.1 ONE 16-KB BOOT BLOCK

The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. The 16-Kbyte (16,384 bytes) boot block is located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map to accommodate different microprocessor protocols for boot code location. This boot block features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental modification. The protection of the boot block is controlled using a combination of the V_{PP}, RP#, and WP# pins, as is detailed in Section 3.4.

2.1.2 TWO 8-KB PARAMETER BLOCKS

The boot block architecture includes parameter blocks to facilitate storage of frequently updated small parameters that would normally require an EEPROM. By using software techniques, the byte-rewrite functionality of EEPROMs can be emulated. These techniques are detailed in Intel's application note *AP-604, Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM*. Each boot block component contains two parameter blocks of 8 Kbytes (8,192 bytes) each. The parameter blocks are not write-protectable.

2.1.3 ONE 96-KB + ONE 128-KB MAIN BLOCK

After the allocation of address space to the boot and parameter blocks, the remainder is divided into main blocks for data or code storage. Each 2-Mbit device contains one 96-Kbyte (98,304 byte) block and one 128-Kbyte (131,072 byte) block. See the memory maps for each device for more information.

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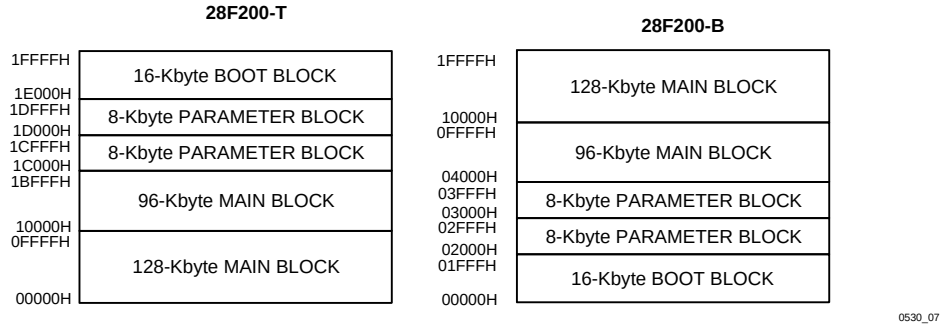
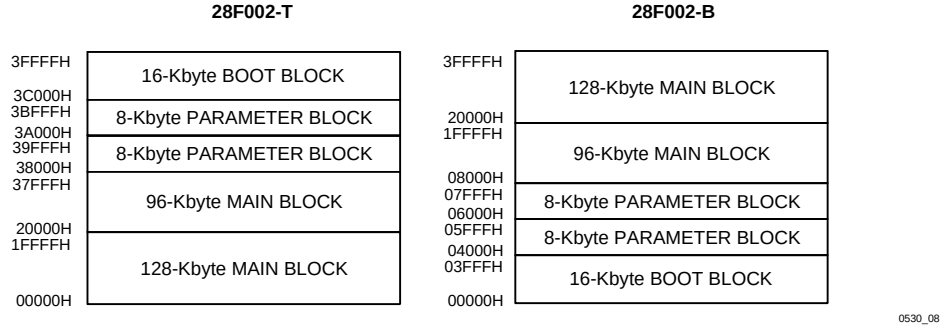


NOTE: In x8 operation, the least significant system address should be connected to A_1. Memory maps are shown for x16 operation.

Figure 7. Word-Wide x16-Mode Memory Maps



NOTE: These memory maps apply to the 28F002B or the 28F200 in x8 mode.

Figure 8. Byte-Wide x8-Mode Memory Maps

3.0 PRODUCT FAMILY PRINCIPLES OF OPERATION

Flash memory combines EPROM functionality with in-circuit electrical program and erase. The boot block flash family utilizes a Command User Interface (CUI) and automated algorithms to simplify program and erase operations. The CUI allows for 100% TTL-level control inputs, fixed power supplies during erasure and programming, and maximum EPROM compatibility.

When $V_{PP} < V_{PPLK}$, the device will only successfully execute the following commands: Read Array, Read Status Register, Clear Status Register and intelligent identifier mode. The device provides standard EPROM read, standby and output disable operations. Manufacturer identification and device identification data can be accessed through the CUI or through the standard EPROM A_9 high voltage access (V_{ID}) for PROM programming equipment.

The same EPROM read, standby and output disable functions are available when 5 V or 12 V is applied to the V_{PP} pin. In addition, 5 V or 12 V on V_{PP} allows program and erase of the device. All functions associated with altering memory contents: Program and Erase, Intelligent Identifier Read, and Read Status are accessed via the CUI.

The internal Write State Machine (WSM) completely automates program and erase, beginning operation signaled by the CUI and reporting status through the status register. The CUI handles the WE# interface to the data and address latches, as well as system status requests during WSM operation.

3.1 Bus Operations

Flash memory reads, erases and programs in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. These bus operations are summarized in Tables 3 and 4.

3.2 Read Operations

3.2.1 READ ARRAY

When RP# transitions from V_{IL} (reset) to V_{IH}, the device will be in the read array mode and will respond to the read control inputs (CE#, address inputs, and OE#) without any commands being written to the CUI.

When the device is in the read array mode, five control signals must be controlled to obtain data at the outputs.

- RP# must be logic high (V_{IH})
- WE# must be logic high (V_{IH})
- BYTE# must be logic high or logic low
- CE# must be logic low (V_{IL})
- OE must be logic low (V_{IL})

In addition, the address of the desired location must be applied to the address pins. Refer to Figures 15 and 16 for the exact sequence and timing of these signals.

If the device is not in read array mode, as would be the case after a program or erase operation, the Read Mode command (FFH) must be written to the CUI before reads can take place.

During system design, consideration should be taken to ensure address and control inputs meet required input slew rates of <10 ns as defined in Figures 12 and 13.

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Table 3. Bus Operations for Word-Wide Mode (BYTE# = V_{IH})

Mode	Notes	RP#	CE#	OE#	WE#	A_9	A_0	V_{PP}	$DQ_{0–15}$
Read	1,2,3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	High Z
Deep Power-Down	9	V_{IL}	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	0089 H
Intelligent Identifier (Device)	4,5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	See Table 5
Write	6,7,8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	D_{IN}

Table 4. Bus Operations for Byte-Wide Mode (BYTE# = V_{IL})

Mode	Notes	RP#	CE#	OE#	WE#	A_9	A_0	$A_{–1}$	V_{PP}	$DQ_{0–7}$	$DQ_{8–14}$
Read	1,2,3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	X	D_{OUT}	High Z
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	High Z	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	X	High Z	High Z
Deep Power-Down	9	V_{IL}	X	X	X	X	X	X	X	High Z	High Z
Intelligent Identifier (Mfr)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	X	89H	High Z
Intelligent Identifier (Device)	4,5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	X	See Table 5	High Z
Write	6,7,8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	X	D_{IN}	High Z

NOTES:

1. Refer to *DC Characteristics*.
2. X can be V_{IL}, V_{IH} for control pins and addresses, V_{PPLK} or V_{PPH} for V_{PP}.
3. See *DC Characteristics* for V_{PPLK}, V_{PPH1}, V_{PPH2}, V_{HH}, V_{ID} voltages.
4. Manufacturer and device codes may also be accessed via a CUI write sequence, A_9–A_{16} = X, A_1–A_{17} = X.
5. See Table 5 for device IDs.
6. Refer to Table 7 for valid D_{IN} during a write operation.
7. Command writes for block erase or word/byte program are only executed when V_{PP} = V_{PPH1} or V_{PPH2}.
8. To program or erase the boot block, hold RP# at V_{HH} or WP# at V_{IH}. See Section 3.4.
9. RP# must be at GND ± 0.2 V to meet the maximum deep power-down current specified.

3.2.2 INTELLIGENT IDENTIFIERS

To read the manufacturer and device codes, the device must be in intelligent identifier read mode, which can be reached using two methods: by writing the Intelligent Identifier command (90H) or by taking the A_9 pin to V_{ID}. Once in intelligent identifier read mode, A_0 = 0 outputs the manufacturer's identification code and A_0 = 1 outputs the device code. In byte-wide mode, only the lower byte of the above signatures is read (DQ_{15}/A_{-1} is a "don't care" in this mode). See Table 5 for product signatures. To return to read array mode, write a Read Array command (FFH).

Table 5. Intelligent Identifier Table

Product	Mfr. ID	Device ID	
		-T (Top Boot)	-B (Bottom Boot)
28F200	0089 H	2274 H	2275 H
28F002	89 H	7C H	7D H

3.3 Write Operations

3.3.1 COMMAND USER INTERFACE (CUI)

The Command User Interface (CUI) is the interface between the microprocessor and the internal chip controller. Commands are written to the CUI using standard microprocessor write timings. The available commands are Read Array, Read Intelligent Identifier, Read Status Register, Clear Status Register, Erase and Program (summarized in Tables 6 and 7). The three read modes are read array, intelligent identifier read, and status register read. For Program or Erase commands, the CUI informs the Write State Machine (WSM) that a program or erase has been requested. During the execution of a Program command, the WSM will control the programming sequences and the CUI will only respond to status reads. During an erase cycle, the CUI will respond to status reads and erase suspend. After the WSM has completed its task, it will set the WSM Status bit to a "1" (ready), which indicates that the CUI can respond to its full command set. Note that after the WSM has returned control to the CUI, the CUI will stay in the current command state until it receives another command.

3.3.1.1 Command Function Description

Device operations are selected by writing specific commands into the CUI. Tables 6 and 7 define the available commands.

Table 6. Command Codes and Descriptions

Code	Device Mode	Description
00	Invalid/ Reserved	Unassigned commands that should not be used. Intel reserves the right to redefine these codes for future functions.
FF	Read Array	Places the device in read array mode, so that array data will be output on the data pins.
40	Program Set-Up	Sets the CUI into a state such that the next write will latch the Address and Data registers on the rising edge and begin the program algorithm. The device then defaults to the read status mode, where the device outputs status register data when OE# is enabled. To read the array, issue a Read Array command. To cancel a program operation after issuing a Program Set-Up command, write all 1's (FFH for x8, FFFFH for x16) to the CUI. This will return to read status register mode after a standard program time without modifying array contents. If a program operation has already been initiated to the WSM this command cannot cancel that operation in progress.
10	Alternate Prog Set-Up	(See 40H/Program Set-Up)
20	Erase Set-Up	Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will set both the Program Status (SR.4) and Erase Status (SR.5) bits of the status register to a "1," place the device into the read status register state, and wait for another command without modifying array contents. This can be used to cancel an erase operation after the Erase Set-Up command has been issued. If an operation has already been initiated to the WSM this can not cancel that operation in progress.
D0	Erase Resume/ Erase Confirm	If the previous command was an Erase Set-Up command, then the CUI will latch address and data, and begin erasing the block indicated on the address pins. During erase, the device will respond only to the Read Status Register and Erase Suspend commands and will output status register data when OE# is toggled low. Status register data is updated by toggling either OE# or CE# low.
B0	Erase Suspend	Valid only while an erase operation is in progress and will be ignored in any other circumstance. Issuing this command will begin to suspend erase operation. The status register will indicate when the device reaches erase suspend mode. In this mode, the CUI will respond only to the Read Array, Read Status Register, and Erase Resume commands and the WSM will also set the WSM Status bit to a "1" (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input control pins except RP#, which will immediately shut down the WSM and the remainder of the chip, if it is made active. During a suspend operation, the data and address latches will remain closed, but the address pads are able to drive the address into the read path. See Section 3.3.4.1.
70	Read Status Register	Puts the device into the read status register mode, so that reading the device outputs status register data, regardless of the address presented to the device. The device automatically enters this mode after program or erase has completed. This is one of the two commands that is executable while the WSM is operating. See Section 3.3.2.

Table 6. Command Codes and Descriptions (Continued)

Code	Device Mode	Description
50	Clear Status Register	The WSM can only set the Program Status and Erase Status bits in the status register to "1;" it cannot clear them to "0." The status register operates in this fashion for two reasons. The first is to give the host CPU the flexibility to read the status bits at any time. Second, when programming a string of bytes, a single status register query after programming the string may be more efficient, since it will return the accumulated error status of the entire string. See Section 3.3.2.1.
90	Intelligent Identifier	Puts the device into the intelligent identifier read mode, so that reading the device will output the manufacturer and device codes. (A_0 = 0 for manufacturer, A_0 = 1 for device, all other address inputs are ignored). See Section 3.2.2.

Table 7. Command Bus Definitions

Command	Note	First Bus Cycle (1)			Second Bus Cycle (1)		
		Oper	Addr	Data	Oper	Addr	Data
Read Array	1	Write	X	FFH			
Intelligent Identifier	1, 2, 4	Write	X	90H	Read	IA	IID
Read Status Register	3	Write	X	70H	Read	X	SRD
Clear Status Register		Write	X	50H			
Word/Byte Program	1, 6, 7	Write	PA	40H/10H	Write	PA	PD
Block Erase/Confirm	1, 5	Write	BA	20H	Write	BA	D0H
Erase Suspend		Write	X	B0H			
Erase Resume		Write	X	D0H			

ADDRESS
BA= Block Address
IA= Identifier Address
PA= Program Address
X= Don't Care

DATA
SRD= Status Register Data
IID= Identifier Data
PD= Program Data

NOTES:
1. Bus operations are defined in Tables 3 and 4.
2. IA = Identifier Address: A_0 = 0 for manufacturer code, A_0 = 1 for device code.
3. SRD = Data read from status register.
4. IID = Intelligent Identifier Data. Following the Intelligent Identifier command, two read operations access manufacturer and device codes.
5. BA = Address within the block being erased.
6. PA = Address to be programmed. PD = Data to be programmed at location PA.
7. Either 40H or 10H commands is valid.
8. When writing commands to the device, the upper data bus [DQ_8–DQ_{15}] = X (28F200 only) which is either V_{IL} or V_{IH}, to minimize current draw.

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Table 8. Status Register Bit Definition

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS 1 = Ready (WSMS) 0 = Busy	Check Write State Machine bit first to determine Word/Byte program or Block Erase completion, before checking Program or Erase Status bits.
SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed	When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an Erase Resume command is issued.
SR.5 = ERASE STATUS (ES) 1 = Error In Block Erasure 0 = Successful Block Erase	When this bit is set to "1," WSM has applied the max number of erase pulses to the block and is still unable to verify successful block erasure.
SR.4 = PROGRAM STATUS (DWS) 1 = Error in Byte/Word Program 0 = Successful Byte/Word Program	When this bit is set to "1," WSM has attempted but failed to program a byte or word.
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	The V_{PP} Status bit does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP} level only after the Program or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPLK} and V_{PPH}.
SR.2–SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	These bits are reserved for future use and should be masked out when polling the status register.

3.3.2 STATUS REGISTER

The device status register indicates when a program or erase operation is complete, and the success or failure of that operation. To read the status register write the Read Status (70H) command to the CUI. This causes all subsequent read operations to output data from the status register until another command is written to the CUI. To return to reading from the array, issue a Read Array (FFH) command.

The status register bits are output on DQ_0–DQ_7, in both byte-wide (x8) or word-wide (x16) mode. In the word-wide mode the upper byte, DQ_8–DQ_{15}, outputs 00H during a Read Status command. In the byte-wide mode, DQ_8–DQ_{14} are tri-stated and DQ_{15}/A_{-1} retains the low order address function.

Important: The contents of the status register are latched on the falling edge of OE# or CE#, whichever occurs last in the read cycle. This prevents possible bus errors which might occur if status register contents change while being read. CE# or OE# must be toggled with each subsequent status read, or the status register will not indicate completion of a program or erase operation.

When the WSM is active, the SR.7 register will indicate the status of the WSM, and will also hold the bits indicating whether or not the WSM was successful in performing the desired operation.

3.3.2.1 Clearing the Status Register

The WSM sets status bits 3 through 7 to “1,” and clears bits 6 and 7 to “0,” but cannot clear status bits 3 through 5 to “0.” Bits 3 through 5 can only be cleared by the controlling CPU through the use of the Clear Status Register (50H) command, because these bits indicate various error conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence) before reading the status register to determine if an error occurred during that series. Clear the status register before beginning another command or sequence. Note, again, that a Read Array command must be issued before data can be read from the memory or intelligent identifier.

3.3.3 PROGRAM MODE

Programming is executed using a two-write sequence. The Program Set-Up command is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM will execute a sequence of internally timed events to:

1. Program the desired bits of the addressed memory word or byte.
2. Verify that the desired bits are sufficiently programmed.

Programming of the memory results in specific bits within a byte or word being changed to a “0.”

If the user attempts to program “1”s, there will be no change of the memory cell content and no error occurs.

The status register indicates programming status: while the program sequence is executing, bit 7 of the status register is a “0.” The status register can be polled by toggling either CE# or OE#. While programming, the only valid command is Read Status Register.

When programming is complete, the program status bits should be checked. If the programming operation was unsuccessful, bit 4 of the status register is set to a “1” to indicate a Program Failure. If bit 3 is set to a “1,” then V_{PP} was not within acceptable limits, and the WSM did not execute the programming sequence.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, reads from the memory array or intelligent identifier cannot be accomplished until the CUI is given the appropriate command.

3.3.4 ERASE MODE

To erase a block, write the Erase Set-Up and Erase Confirm commands to the CUI, along with the addresses identifying the block to be erased. These addresses are latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to “1.” Only one block can be erased at a time.

The WSM will execute a sequence of internally timed events to:

1. Program all bits within the block to “0.”
2. Verify that all bits within the block are sufficiently programmed to “0.”
3. Erase all bits within the block to “1.”
4. Verify that all bits within the block are sufficiently erased.

While the erase sequence is executing, bit 7 of the status register is a “0.”

When the status register indicates that erasure is complete, check the erase status bit to verify that the erase operation was successful. If the erase operation was unsuccessful, bit 5 of the status register will be set to a “1,” indicating an Erase Failure. If V_{PP} was not within acceptable limits after the Erase Confirm command is issued, the WSM will not execute an erase sequence; instead, bit 5 of the status register is set to a “1” to indicate an Erase Failure, and bit 3 is set to a “1” to identify that V_{PP} supply voltage was not within acceptable limits.

Clear the status register before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, reads from the memory array, status register, or intelligent identifier cannot be accomplished until the CUI is given the Read Array command.

3.3.4.1 Suspending and Resuming Erase

Since an erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from another block of the memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a predetermined point in the erase algorithm. The status register will indicate if/when the erase operation has been suspended.

At this point, a Read Array command can be written to the CUI in order to read data from blocks other than that which is being suspended. The only other valid command at this time is the Erase Resume command or Read Status Register command.

During erase suspend mode, the chip can go into a pseudo-standby mode by taking CE# to V_{IH}, which reduces active current draw.

To resume the erase operation, enable the chip by taking CE# to V_{IL}, then issuing the Erase Resume command, which continues the erase sequence to completion. As with the end of a standard erase operation, the status register must be read, cleared, and the next instruction issued in order to continue.

3.4 Boot Block Locking

The boot block family architecture features a hardware-lockable boot block so that the kernel code for the system can be kept secure while the parameter and main blocks are programmed and erased independently as necessary. Only the boot block can be locked independently from the other blocks. The truth table, Table 9, clearly defines the write protection methods.

3.4.1 $V_{PP} = V_{IL}$ FOR COMPLETE PROTECTION

For complete write protection of all blocks in the flash device, the V_{PP} programming voltage can be held low. When V_{PP} is below V_{PPLK}, any program or erase operation will result in a error in the status register.

3.4.2 WP# = V_{IL} FOR BOOT BLOCK LOCKING

When WP# = V_{IL}, the boot block is locked and any program or erase operation to the boot block will result in an error in the status register. All other blocks remain unlocked in this condition and can be programmed or erased normally. Note that this feature is overridden and the boot block unlocked when RP# = V_{HH}.

3.4.3 RP# = V_{HH} OR WP# = V_{IH} FOR BOOT BLOCK UNLOCKING

Two methods can be used to unlock the boot block:

1. WP# = V_{IH}
2. RP# = V_{HH}

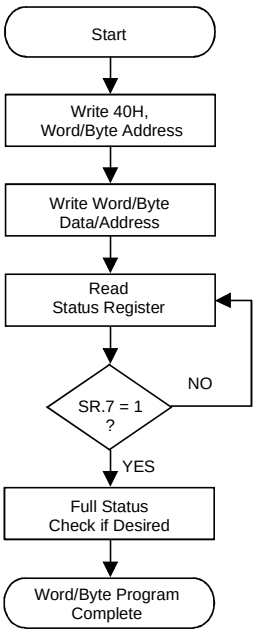
If both or either of these two conditions are met, the boot block will be unlocked and can be programmed or erased.

3.4.4 UPGRADE NOTE FOR 8-MBIT 44-PSOP PACKAGE

If upgradability to 8 Mbit is required, note that the 8-Mbit in the 44-PSOP does not have a WP# because no pins were available for the 8-Mbit upgrade address. Thus, in this density-package combination only, V_{HH} (12 V) on RP# is required to unlock the boot block. Unlocking with a logic-level signal is not possible. If this functionality is required, and 12 V is not available, consider using the 48-TSOP package, which has a WP# pin and can be unlocked with a logic-level signal. All other density-package combinations have WP# pins.

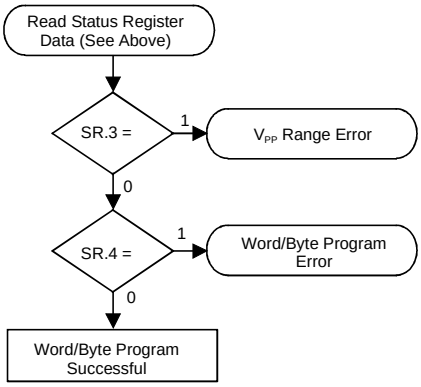
Table 9. Write Protection Truth Table

V_{PP}	RP#	WP#	Write Protection Provided
V_{IL}	X	X	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	X	All Blocks Locked (Reset)
$\geq V_{PPLK}$	V_{HH}	X	All Blocks Unlocked
$\geq V_{PPLK}$	V_{IH}	V_{IL}	Boot Block Locked
$\geq V_{PPLK}$	V_{IH}	V_{IH}	All Blocks Unlocked



Bus Operation	Command	Comments
Write	Setup Program	Data = 40H Addr = Word/Byte to Program
Write	Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update SRD
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent word/byte program operations. SR Full Status Check can be done after each word/byte program, or after a sequence of word/byte programs. Write FFH after the last program operation to reset device to read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = Word/Byte Program Error
SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine. SR.4 is only cleared by the Clear Status Register Command, in cases where multiple bytes are programmed before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

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Figure 9. Automated Word/Byte Programming Flowchart

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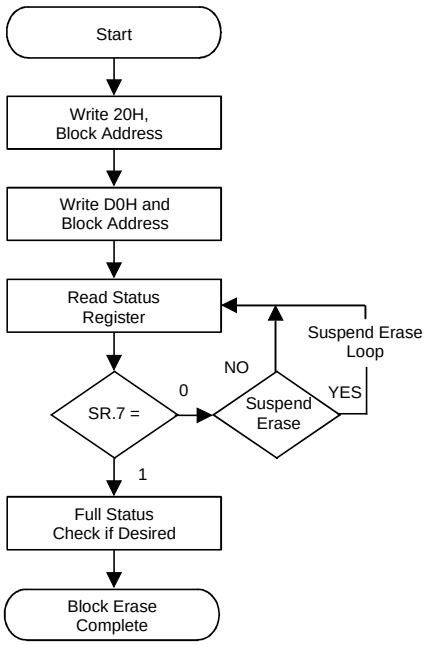
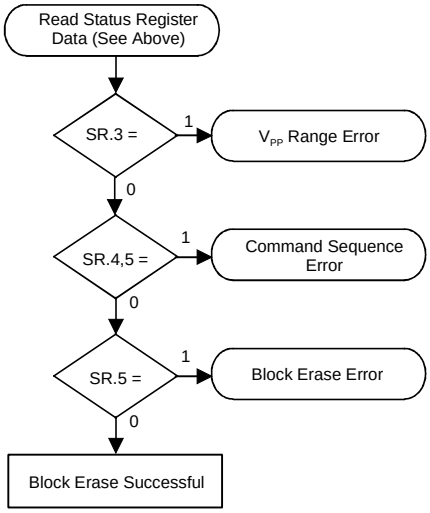


Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to Be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to Be Erased
Read		Status Register Data Toggle CE# or OE# to Update Status Register
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.
Full Status Check can be done after each block erase, or after a sequence of block erasures.
Write FFH after the last operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.5 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erase before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

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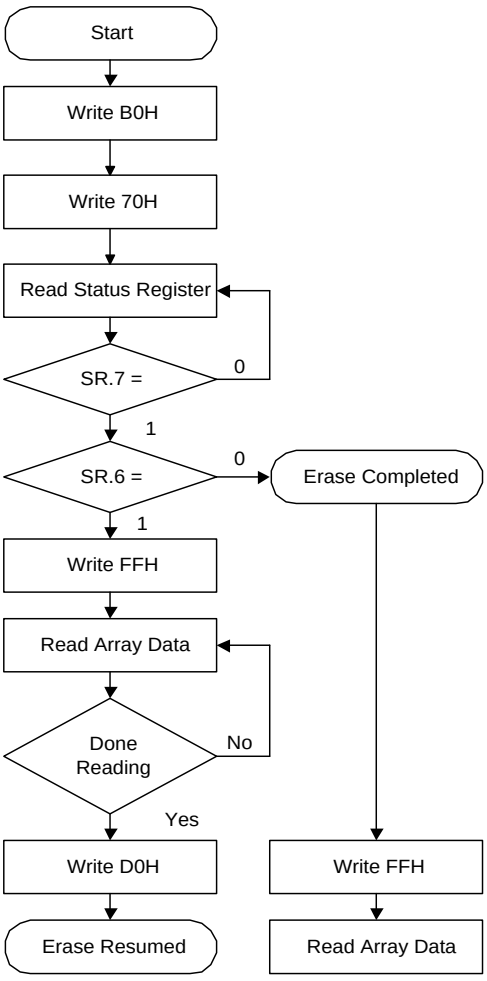
Figure 10. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Write	Read Status	Data=70H Addr=X
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being programmed.
Write	Erase Resume	Data = D0H Addr = X

Figure 11. Erase Suspend/Resume Flowchart

SEE NEW DESIGN RECOMMENDATIONS

3.5 Power Consumption

3.5.1 ACTIVE POWER

With CE# at a logic-low level and RP# at a logic-high level, the device is placed in the active mode. Refer to the DC Characteristics table for I_{CC} current values.

3.5.2 AUTOMATIC POWER SAVINGS (APS)

Automatic Power Savings (APS) provides low-power operation during active mode. Power Reduction Control (PRC) circuitry allows the device to put itself into a low current state when not being accessed. After data is read from the memory array, PRC logic controls the device's power consumption by entering the APS mode where typical I_{CC} current is less than 1 mA. The device stays in this static state with outputs valid until a new location is read.

3.5.3 STANDBY POWER

With CE# at a logic-high level (V_{IH}), and the CUI in read mode, the memory is placed in standby mode, which disables much of the device's circuitry and substantially reduces power consumption. Outputs (DQ_0–DQ_{15} or DQ_0–DQ_7) are placed in a high-impedance state independent of the status of the OE# signal. When CE# is at logic-high level during erase or program operations, the device will continue to perform the operation and consume corresponding active power until the operation is completed.

3.5.4 DEEP POWER-DOWN MODE

The SmartVoltage boot block family supports a low typical I_{CC} in deep power-down mode, which turns off all circuits to save power. This mode is activated by the RP# pin when it is at a logic-low (GND ± 0.2 V).

NOTE

Note: BYTE# pin must be at CMOS levels to meet the I_{CCD} specification.

During read modes, the RP# pin going low de-selects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state, requires a minimum access time of t_{PHQV} (see *AC Characteristics* table).

During erase or program modes, RP# low will abort either erase or program operations, but the memory contents are no longer valid as the data has been corrupted by the RP# function. As in the read mode above, all internal circuitry is turned off to achieve the power savings.

RP# transitions to V_{IL}, or turning power off to the device will clear the status register.

3.6 Power-Up/Down Operation

The device is protected against accidental block erasure or programming during power transitions. Power supply sequencing is not required, since the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers-up first. The CUI is reset to the read mode after power-up, but the system must drop CE# low or present a new address to ensure valid data at the outputs.

A system designer must guard against spurious writes when V_{CC} voltages are above V_{LKO} and V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until RP# is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset (RP# connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

3.6.1 RP# CONNECTED TO SYSTEM RESET

The use of RP# during system reset is important with automated program/erase devices because the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization would not occur because the flash memory may be providing status information instead of array data. Intel's Flash memories allow proper CPU initialization following a system reset by connecting the RP# pin to the same RESET# signal that resets the system CPU.

3.6.2 V_{CC}, V_{PP} AND RP# TRANSITIONS

The CUI latches commands as issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its default state upon power-up, after exit from deep power-down mode, or after V_{CC} transitions above V_{LKO} (lockout voltage), is read array mode.

After any word/byte program or block erase operation is complete and even after V_{PP} transitions down to V_{PPLK}, the CUI must be reset to read array mode via the Read Array command if accesses to the flash memory are desired.

Please refer to Intel's application note *AP-617 Additional Flash Data Protection Using V_{PP}, RP#, and WP#* for a circuit-level description of how to implement the protection discussed in Section 3.6.

3.7 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling methods. System designers should consider three supply current issues:

1. Standby current levels (I_{CCS})
2. Active current levels (I_{CCR})
3. Transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

3.7.1 V_{PP} TRACE ON PRINTED CIRCUIT BOARDS

Designing for in-system programming of the flash memory requires special consideration of the V_{PP} power supply trace by the printed circuit board designer. The V_{PP} pin supplies the flash memory cells current for programming and erasing. One should use similar trace widths and layout considerations given to the V_{CC} power supply trace. Adequate V_{PP} supply traces, and decoupling capacitors placed adjacent to the component, will decrease spikes and overshoots.

NOTE:

Table headings in the DC and AC characteristics tables (i.e., BV-60, BV-80, BV-120, TBV-80, TBE-120) refer to the specific products listed below. See Section 5.0 for more information on product naming and line items.

Abbreviation	Applicable Product Names
BV-60	E28F002BV-T60, E28F002BV-B60, PA28F200BV-T60, PA28F200BV-B60, E28F200CV-T60, E28F200CV-B60, E28F200BV-T60, E28F200BV-B60
BV-80	E28F002BV-T80, E28F002BV-B80, PA28F200BV-T80, PA28F200BV-B80, E28F200CV-T80, E28F200CV-B80, E28F200BV-T80, E28F200BV-B80
BV-120	E28F002BV-T120, E28F002BV-B120, PA28F200BV-T120, PA28F200BV-B120
TBV-80	TE28F002BV-T80, TE28F002BV-B80, TB28F200BV-T80, TB28F200BV-B80, TE28F200CV-T80, TE28F200CV-B80, TE28F200BV-T80, TE28F200BV-B80

4.0 ELECTRICAL SPECIFICATIONS

NOTICE: This datasheet contains preliminary information on new products in production. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

4.1 Absolute Maximum Ratings*

Commercial Operating Temperature

During Read ..... 0 °C to +70 °C

During Block Erase and Word/Byte Program ..... 0 °C to +70 °C

Temperature Under Bias ..... –10 °C to +80 °C

Extended Operating Temperature

During Read ..... –40 °C to +85 °C

During Block Erase and Word/Byte Program ..... –40 °C to +85 °C

Temperature Under Bias ..... –40 °C to +85 °C

Storage Temperature..... –65 °C to +125 °C

Voltage on Any Pin (except V_{CC}, V_{PP}, A_9 and RP#) with Respect to GND ..... –2.0 V to +7.0 V(2)

Voltage on Pin RP# or Pin A_9 with Respect to GND ..... –2.0 V to +13.5 V(2,3)

V_{PP} Program Voltage with Respect to GND during Block Erase and Word/Byte Program .. –2.0 V to +14.0 V(2,3)

V_{CC} Supply Voltage with Respect to GND ..... –2.0 V to +7.0 V(2)

Output Short Circuit Current.....100 mA (4)

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is –0.5 V on input/output pins. During transitions, this level may undershoot to –2.0 V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods <20 ns.
3. Maximum DC voltage on V_{PP} may overshoot to +14.0 V for periods <20 ns. Maximum DC voltage on RP# or A_9 may overshoot to 13.5 V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

4.2 Commercial Operating Conditions

Table 10. Commercial Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		0	+70	°C
V_{CC}	3.3 V V_{CC} Supply Voltage (± 0.3 V)		3.0	3.6	Volts
	5 V V_{CC} Supply Voltage (10%)	1	4.50	5.50	Volts
	5 V V_{CC} Supply Voltage (5%)	2	4.75	5.25	Volts

NOTES:

1. 10% V_{CC} specifications apply to the 60 ns, 80 ns and 120 ns product versions in their standard test configuration.
2. 5% V_{CC} specifications apply to the 60 ns version in its high-speed test configuration.

4.2.1 APPLYING V_{CC} VOLTAGES

When applying V_{CC} voltage to the device, a delay may be required before initiating device operation, depending on the V_{CC} ramp rate. If V_{CC} ramps slower than 1V/100 µs (0.01 V/µs) then no delay is required. If V_{CC} ramps faster than 1V/100 µs (0.01 V/µs), then a delay of 2 µs is required before initiating device operation. RP# = GND is recommended during power-up to protect against spurious write signals when V_{CC} is between V_{LKO} and V_{CCMIN}.

V_{CC} Ramp Rate	Required Timing
≤ 1V/100 µs	No delay required.
> 1V/100 µs	A delay time of 2 µs is required before any device operation is initiated, including read operations, command writes, program operations, and erase operations. This delay is measured beginning from the time V_{CC} reaches V_{CCMIN} (3.0 V for 3.3 ± 0.3 V operation; and 4.5 V for 5 V operation).

NOTES:

1. These requirements must be strictly followed to guarantee all other read and write specifications.
2. To switch between 3.3 V and 5 V operation, the system should first transition V_{CC} from the existing voltage range to GND, and then to the new voltage. Any time the V_{CC} supply drops below V_{CCMIN}, the chip may be reset, aborting any operations pending or in progress.
3. These guidelines must be followed for any V_{CC} transition from GND.

4.3 Capacitance

T_A = 25 °C, f = 1 MHz

Symbol	Parameter	Note	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance	1	6	8	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	1, 2	10	12	pF	V_{OUT} = 0 V

NOTES:

1. Sampled, not 100% tested.
2. For the 28F002B, address pin A_{10} follows the C_{OUT} capacitance numbers.

SEE NEW DESIGN RECOMMENDATIONS

4.4 DC Characteristics—Commercial

Sym	Parameter	Prod	BV-60 BV-80 BV-120				Unit	Test Conditions
		V_{CC}	3.3 ± 0.3 V		5 V ± 10%			
		Note	Typ	Max	Typ	Max		
I_{IL}	Input Load Current	1		± 1.0		± 1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		± 10		± 10	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3	0.4	1.5	0.8	2.0	mA	$V_{CC} = V_{CC}$ Max CE# = RP# = BYTE# = WP# = V_{IH}
			60	110	50	130	µA	$V_{CC} = V_{CC}$ Max CE# = RP# = V_{CC} ± 0.2 V
I_{CCD}	V_{CC} Deep Power-Down Current	1	0.2	8	0.2	8	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND RP# = GND ± 0.2 V
I_{CCR}	V_{CC} Read Current for Word or Byte	1,5,6	15	30	50	60	mA	**CMOS INPUTS** $V_{CC} = V_{CC}$ Max CE# = GND, OE# = V_{CC} f = 10 MHz (5 V), 5 MHz (3.3 V) I_{OUT} = 0 mA, Inputs = GND ± 0.2 V or V_{CC} ± 0.2 V
			15	30	55	65	mA	**TTL INPUTS** $V_{CC} = V_{CC}$ Max CE# = V_{IL}, OE# = V_{IH} f = 10 MHz (5 V), 5 MHz (3.3 V) I_{OUT} = 0 mA, Inputs = V_{IL} or V_{IH}
I_{CCW}	V_{CC} Program Current for Word or Byte	1,4	13	30	30	50	mA	$V_{PP} = V_{PPH}1$ (at 5 V) Program in Progress
			10	25	30	45	mA	$V_{PP} = V_{PPH}2$ (at 12 V) Program in Progress
I_{CCE}	V_{CC} Erase Current	1,4	13	30	18	35	mA	$V_{PP} = V_{PPH}1$ (at 5 V) Block Erase in Progress
			10	25	18	30	mA	$V_{PP} = V_{PPH}2$ (at 12 V) Block Erase in Progress

4.4 DC Characteristics—Commercial (Continued)

Sym	Parameter	Prod	BV-60 BV-80 BV-120				Unit	Test Conditions
		V_{CC}	3.3 ± 0.3 V		5 V ± 10%			
		Note	Typ	Max	Typ	Max		
I_{CCES}	V_{CC} Erase Suspend Current	1,2	3	8.0	5	10	mA	CE# = V_{IH} Block Erase Suspend
I_{PPS}	V_{PP} Standby Current	1	± 0.5	± 15	± 0.5	± 10	µA	$V_{PP} < V_{PPH}2$
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.2	5.0	0.2	5.0	µA	RP# = GND ± 0.2 V
I_{PPR}	V_{PP} Read Current	1	50	200	30	200	µA	$V_{PP} \geq V_{PPH}2$
I_{PPW}	V_{PP} Program Current for Word or Byte	1,4	13	30	13	25	mA	$V_{PP} = V_{PPH}1$ (at 5 V) Program in Progress
			8	25	8	20		$V_{PP} = V_{PPH}2$ (at 12 V) Program in Progress
I_{PPE}	V_{PP} Erase Current	1,4	13	30	10	20	mA	$V_{PP} = V_{PPH}1$ (at 5 V) Block Erase in Progress
			8	25	5	15		$V_{PP} = V_{PPH}2$ (at 12 V) Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1	50	200	30	200	µA	$V_{PP} = V_{PPH}$ Block Erase Suspend in Progress
$I_{RP\#}$	RP# Boot Block Unlock Current	1,4		500		500	µA	RP# = V_{HH}
I_{ID}	A_9 Intelligent Identifier Current	1,4		500		500	µA	$A_9 = V_{ID}$

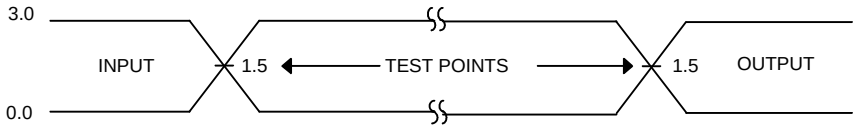
SEE NEW DESIGN RECOMMENDATIONS

4.4 DC Characteristics—Commercial (Continued)

Sym	Parameter	Prod	BV-60 BV-80 BV-120				Unit	Test Conditions
		V_{CC}	3.3 ± 0.3 V		5 V ± 10%			
		Note	Min	Max	Min	Max		
V_{ID}	A_9 Intelligent Identifier Voltage		11.4	12.6	11.4	12.6	V	
V_{IL}	Input Low Voltage		–0.5	0.8	–0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5V	2.0	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage			0.45		0.45	V	$V_{CC} = V_{CC}$ Min I_{OL} = 5.8 mA
$V_{OH}1$	Output High Voltage (TTL)		2.4		2.4		V	$V_{CC} = V_{CC}$ Min I_{OH} = –2.5 mA
$V_{OH}2$	Output High Voltage (CMOS)		0.85 × V_{CC}		0.85 × V_{CC}		V	$V_{CC} = V_{CC}$ Min I_{OH} = –2.5 mA
			V_{CC}– 0.4V		V_{CC}– 0.4V		V	$V_{CC} = V_{CC}$ Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lock-Out Voltage	3	0.0	1.5	0.0	1.5	V	Total Write Protect
$V_{PPH}1$	V_{PP} (Prog/Erase Operations)		4.5	5.5	4.5	5.5	V	V_{PP} at 5 V
$V_{PPH}2$	V_{PP} (Prog/Erase Operations)		11.4	12.6	11.4	12.6	V	V_{PP} at 12 V
V_{LKO}	V_{CC} Erase/Prog Lock Voltage	8	2.0		2.0		V	
V_{HH}	RP# Unlock Voltage		11.4	12.6	11.4	12.6	V	Boot Block Unlock

NOTES:

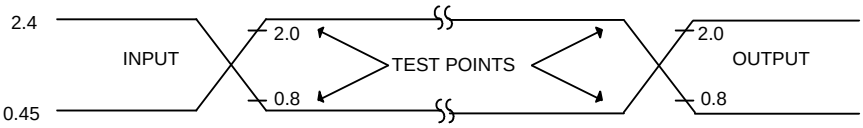
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0 V, T = +25 °C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device deselected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases and word/byte programs are inhibited when $V_{PP} = V_{PPLK}$, and not guaranteed in the range between $V_{PPH}1$ and V_{PPLK}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to less than 1 mA typical, in static operation.
6. CMOS Inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL Inputs are either V_{IL} or V_{IH}.
7. For the 28F002B, address pin A_{10} follows the C_{OUT} capacitance numbers.
8. For all BV/CV parts, V_{LKO} = 2.0 V for both 3.3 V and 5 V operations.



NOTE:
AC test inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Input timing begins, and output timing ends, at 1.5 V. Input rise and fall times (10% to 90%) <10 ns.

0530_12

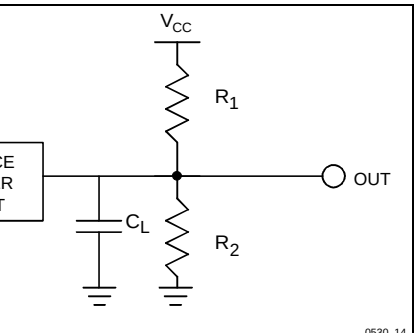
Figure 12. 3.3 V Inputs and Measurement Points



NOTE:
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}) . Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

0530_13

Figure 13. 5 V Inputs and Measurement Points



0530_14

NOTE: See table for component values.

Figure 14. Test Configuration

Test Configuration Component Values

Test Configuration	C_L (pF)	R_1 (Ω)	R_2 (Ω)
3.3 V Standard Test	50	990	770
5 V Standard Test	100	580	390
5 V High-Speed Test	30	580	390

NOTE: C_L includes jig capacitance.

SEE NEW DESIGN RECOMMENDATIONS

4.5 AC Characteristics—Commercial

Sym	Parameter	Prod	BV-60						Unit
		V_{CC}	3.3 ± 0.3 V(5)		5 V ± 5%(6)		5 V ± 10%(7)		
		Load	50 pF		30 pF		100 pF		
		Note	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time		110		60		70		ns
t_{AVQV}	Address to Output Delay			110		60		70	ns
t_{ELQV}	CE# to Output Delay	2		110		60		70	ns
t_{PHQV}	RP# to Output Delay			0.8		0.45		0.45	µs
t_{GLQV}	OE# to Output Delay	2		65		30		35	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		0		ns
t_{EHQZ}	CE# to Output in High Z	3		45		20		20	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		45		20		20	ns
t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	3	0		0		0		ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3	0		0		0		ns
t_{AVFL}	Address to BYTE# High or Low	3		5		5		5	ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3,4		110		60		70	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		45		20		25	ns
t_{PLPH}	Reset Pulse Width Low	8	150		60		60		ns
t_{PLQZ}	RP# Low to Output High-Z			150		60		60	ns

4.5 AC Characteristics—Commercial (Continued)

Sym	Parameter	Prod	BV-80				BV-120				Unit
		V_{CC}	3.3 ± 0.3V(5)		5V ± 10%(7)		3.3 ± 0.3V(5)		5V ± 10%(7)		
		Load	50 pF		100 pF		50 pF		100 pF		
		Notes	Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time		150		80		180		120		ns
t_{AVQV}	Address to Output Delay			150		80		180		120	ns
t_{ELQV}	CE# to Output Delay	2		150		80		180		120	ns
t_{PHQV}	RP# to Output Delay			0.8		0.45		0.8		0.45	µs
t_{GLQV}	OE# to Output Delay	2		90		40		90		40	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		0		0		ns
t_{EHQZ}	CE# to Output in High Z	3		45		20		45		25	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		45		20		45		20	ns
t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	3	0		0		0		0		ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3	0		0		0		0		ns
t_{AVFL}	Address to BYTE# High or Low	3		5		5		5		5	ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3,4		150		80		180		120	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		60		30		60		30	ns
t_{PLPH}	Reset Pulse Width Low	8	150		60		150		60		ns
t_{PLQZ}	RP# Low to Output High-Z			150		60		150		60	ns

NOTES:

1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to t_{CE}–t_{OE} after the falling edge of CE# without impact on t_{CE}.
3. Sampled, but not 100% tested.
4. t_{FLQV}, BYTE# switching low to valid output delay will be equal to t_{AVQV}, measured from the time DQ_{15}/A_{-1} becomes valid.
5. See *Test Configuration* (Figure 14), 3.3 V Standard Test component values.
6. See *Test Configuration* (Figure 14), 5 V High-Speed Test component values.
7. See *Test Configuration* (Figure 14), 5 V Standard Test component values.
8. The specification t_{PLPH} is the minimum time that RP# must be held low in order to product a valid reset of the device.

SEE NEW DESIGN RECOMMENDATIONS

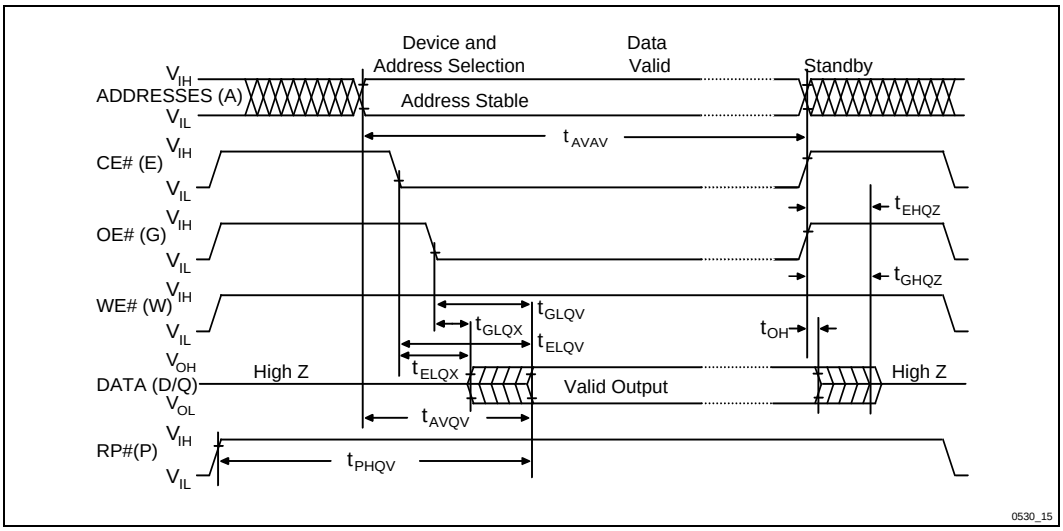


Figure 15. AC Waveforms for Read Operations

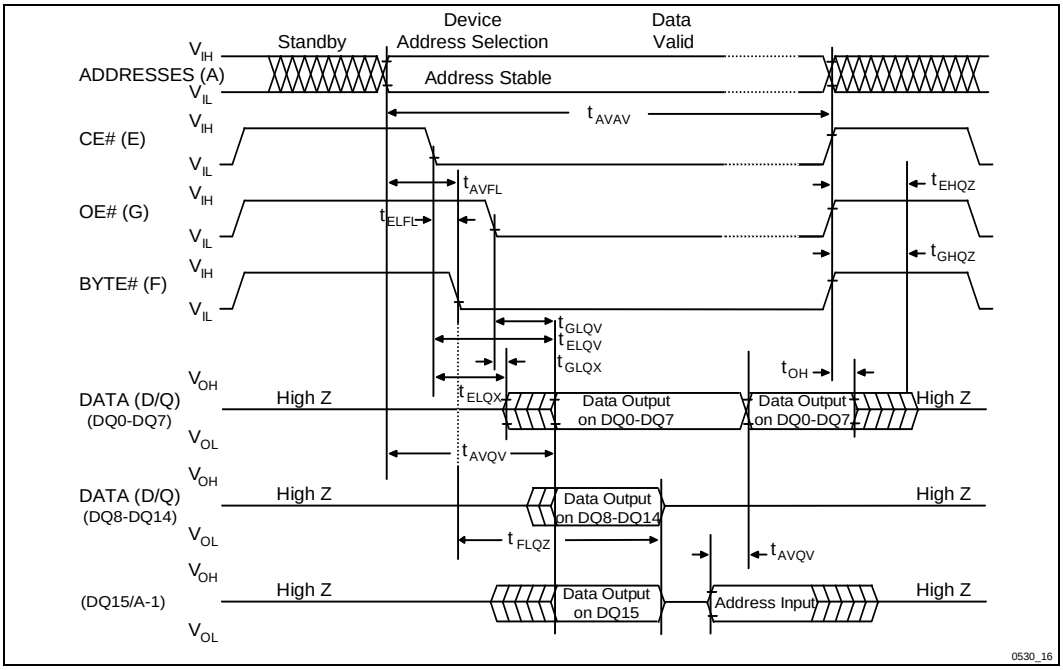


Figure 16. BYTE# Timing Diagram for Read Operations

4.6 AC Characteristics—WE#-Controlled Write Operations[1]—Commercial

Sym	Parameter	Prod	BV-60						Unit
		V_{CC}	3.3 ± 0.3 V[9]		5 V ± 5%[10]		5 V ± 10%[10]		
		Load	50 pF		30 pF		100 pF		
		Note	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		110		60		70		ns
t_{PHWL}	RP# Setup to WE# Going Low		0.8		0.45		0.45		µs
t_{ELWL}	CE# Setup to WE# Going Low		0		0		0		ns
t_{PHHWH}	Boot Block Lock Setup to WE# Going High	6,8	200		100		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	5,8	200		100		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	90		50		50		ns
t_{DVWH}	Data Setup to WE# Going High	4	90		50		50		ns
t_{WLWH}	WE# Pulse Width		90		50		50		ns
t_{WHDX}	Data Hold Time from WE# High	4	0		0		0		ns
t_{WHAX}	Address Hold Time from WE# High	3	0		0		0		ns
t_{WHEH}	CE# Hold Time from WE# High		0		0		0		ns
t_{WHWL}	WE# Pulse Width High		20		10		20		ns
t_{WHQV1}	Duration of Word/Byte Program	2,5	6		6		6		µs
t_{WHQV2}	Duration of Erase (Boot)	2,5,6	0.3		0.3		0.3		s
t_{WHQV3}	Duration of Erase (Parameter)	2,5	0.3		0.3		0.3		s
t_{WHQV4}	Duration of Erase (Main)	2,5	0.6		0.6		0.6		s
t_{QVVL}	V_{PP} Hold from Valid SRD	5,8	0		0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		0		ns
t_{PHBR}	Boot-Block Lock Delay	7,8		200		100		100	ns

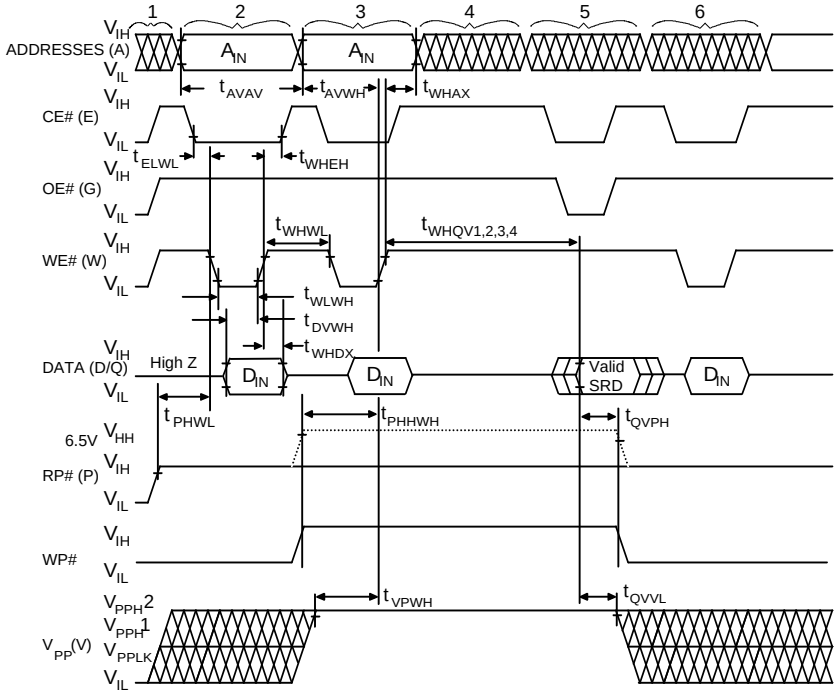
SEE NEW DESIGN RECOMMENDATIONS

4.6 AC Characteristics—WE#-Controlled Write Operations[1]—Commercial (Continued)

Sym	Parameter	Prod	BV-80				BV-120				Unit
		V_{CC}	3.3 ±0.3V[9]		5V±10%[11]		3.3 ± 0.3V[9]		5V±10%[11]		
		Load	50 pF		100 pF		50 pF		100 pF		
		Notes	Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		150		80		180		120		ns
t_{PHWL}	RP# Setup to WE# Going Low		0.8		0.45		0.8		0.45		µs
t_{ELWL}	CE# Setup to WE# Going Low		0		0		0		0		ns
t_{PHHWH}	Boot Block Lock Setup to WE# Going High	6,8	200		100		200		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	5,8	200		100		200		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	120		50		150		50		ns
t_{DVWH}	Data Setup to WE# Going High	4	120		50		150		50		ns
t_{WLWH}	WE# Pulse Width		120		50		150		50		ns
t_{WHDX}	Data Hold Time from WE# High	4	0		0		0		0		ns
t_{WHAX}	Address Hold Time from WE# High	3	0		0		0		0		ns
t_{WHEH}	CE# Hold Time from WE# High		0		0		0		0		ns
t_{WHWL}	WE# Pulse Width High		30		30		30		30		ns
t_{WHQV1}	Word/Byte Program Time	2,5	6		6		6		6		µs
t_{WHQV2}	Erase Duration (Boot)	2,5,6	0.3		0.3		0.3		0.3		s
t_{WHQV3}	Erase Duration (Param)	2,5	0.3		0.3		0.3		0.3		s
t_{WHQV4}	Erase Duration (Main)	2,5	0.6		0.6		0.6		0.6		s
t_{QVVL}	V_{PP} Hold from Valid SRD	5,8	0		0		0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		0		0		ns
t_{PHBR}	Boot-Block Lock Delay	7,8		200		100		200		100	ns

NOTES:

1. Read timing characteristics during program and erase operations are the same as during read-only operations. Refer to *AC Characteristics* during read mode.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled internally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}. (Table 7)
4. Refer to command definition table for valid D_{IN}. (Table 7)
5. Program/erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
6. For boot block program/erase, RP# should be held at V_{HH} or WP# should be held at V_{IH} until operation completes successfully.
7. Time t_{PHBR} is required for successful locking of the boot block.
8. Sampled, but not 100% tested.
9. See *Test Configuration* (Figure 14), 3.3 V Standard Test component values.
10. See *Test Configuration* (Figure 14), 5 V High-Speed Test component values.
11. See *Test Configuration* (Figure 14), 5 V Standard Test component values.



NOTES:

1. V_{CC} Power-Up and Standby.
2. Write program or Erase Set-Up Command.
3. Write Valid Address and Data (Program) or Erase Confirm Command.
4. Automated Program or Erase Delay.
5. Read Status Register Data.
6. Write Read Array Command.

0530_17

Figure 17. AC Waveforms for Write Operations (WE#–Controlled Writes)

SEE NEW DESIGN RECOMMENDATIONS

4.7 AC Characteristics—CE#-Controlled Write Operations[1, 12]—Commercial

Sym	Parameter	Prod	BV-60						Unit
		V_{CC}	3.3 ± 0.3 V[9]		5 V ± 5%[10]		5 V ± 10%[11]		
		Load	50 pF		30 pF		100 pF		
		Note	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		110		60		70		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		0.8		0.45		0.45		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		0		0		ns
t_{PHHEH}	Boot Block Lock Setup to CE# Going High	6,8	200		100		100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	5,8	200		100		100		ns
t_{AVEH}	Address Setup to CE# Going High	3	90		50		50		ns
t_{DVEH}	Data Setup to CE# Going High	4	90		50		50		ns
t_{ELEH}	CE# Pulse Width		90		50		50		ns
t_{EHDX}	Data Hold Time from CE# High	4	0		0		0		ns
t_{EHAX}	Address Hold Time from CE# High	3	0		0		0		ns
t_{EHWH}	WE # Hold Time from CE# High		0		0		0		ns
t_{EHEL}	CE# Pulse Width High		20		10		20		ns
t_{EHQV1}	Duration of Word/Byte Programming Operation	2,5	6		6		6		µs
t_{EHQV2}	Erase Duration (Boot)	2,5,6	0.3		0.3		0.3		s
t_{EHQV3}	Erase Duration (Param)	2,5	0.3		0.3		0.3		s
t_{EHQV4}	Erase Duration(Main)	2,5	0.6		0.6		0.6		s
t_{QVVL}	V_{PP} Hold from Valid SRD	5,8	0		0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		0		ns
t_{PHBR}	Boot-Block Lock Delay	7,8		200		100		100	ns

4.7 AC Characteristics—CE#-Controlled Write Operations[1, 12]—Commercial (Continued)

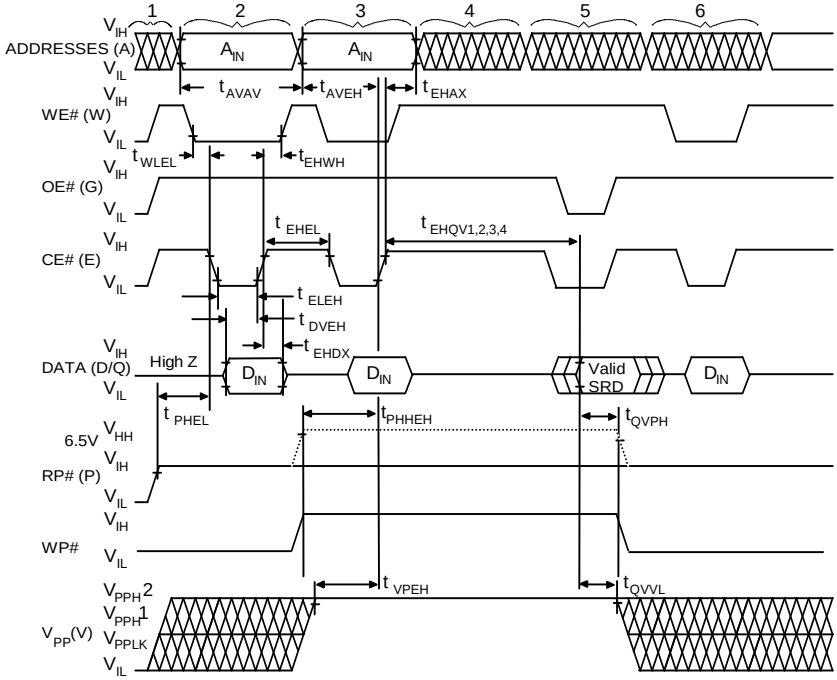
Sym	Parameter	Prod	BV-80				BV-120				Unit
		V_{CC}	3.3 ± 0.3V[9]		5V±10%[11]		3.3 ± 0.3V[9]		5V±10%[11]		
		Load	50 pF		100 pF		50 pF		100 pF		
		Notes	Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		150		80		180		120		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		0.8		0.45		0.8		0.45		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		0		0		0		ns
t_{PHHEH}	Boot Block Lock Setup to CE# Going High	6,8	200		100		200		100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	5,8	200		100		200		100		ns
t_{AVEH}	Address Setup to CE# Going High	3	120		50		150		50		ns
t_{DVEH}	Data Setup to CE# Going High	4	120		50		150		50		ns
t_{ELEH}	CE# Pulse Width		120		50		150		50		ns
t_{EHDX}	Data Hold Time from CE# High	4	0		0		0		0		ns
t_{EHAX}	Address Hold Time from CE# High	3	0		0		0		0		ns
t_{EHWH}	WE # Hold Time from CE# High		0		0		0		0		ns
t_{EHEL}	CE# Pulse Width High		30		30		30		30		ns
t_{EHQV1}	Duration of Word/Byte Programming Operation	2,5	6		6		6		6		µs
t_{EHQV2}	Erase Duration (Boot)	2,5,6	0.3		0.3		0.3		0.3		s
t_{EHQV3}	Erase Duration (Param)	2,5	0.3		0.3		0.3		0.3		s
t_{EHQV4}	Erase Duration(Main)	2,5	0.6		0.6		0.6		0.6		s
t_{QVVL}	V_{PP} Hold from Valid SRD	5,8	0		0		0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		0		0		ns
t_{PHBR}	Boot-Block Lock Delay	7,8		200		100		200		100	ns

SEE NEW DESIGN RECOMMENDATIONS

NOTES:

See *AC Characteristics—WE#-Controlled Write Operations* for notes 1 through 11.

12. Chip-Enable controlled writes: write operations are driven by the valid combination of CE# and WE# in systems where CE# defines the write pulse-width (within a longer WE# timing waveform), all set-up, hold and inactive WE# times should be measured relative to the CE# waveform.



NOTES:

1. V_{CC} Power-Up and Standby.
2. Write program or Erase Set-Up Command.
3. Write Valid Address and Data (Program) or Erase Confirm Command.
4. Automated Program or Erase Delay.
5. Read Status Register Data.
6. Write Read Array Command.

0530_18

Figure 18. Alternate AC Waveforms for Write Operations (CE#–Controlled Writes)

4.8 Erase and Program Timings—Commercial

T_A = 0 °C to +70 °C

	V_{PP}	5 V ± 10%				12 V ± 5%				
	V_{CC}	3.3 ± 0.3 V		5 V ± 10%		3.3 ± 0.3 V		5 V ± 10%		
Parameter		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Boot/Parameter Block Erase Time		0.84	7	0.8	7	0.44	7	0.34	7	s
Main Block Erase Time		2.4	14	1.9	14	1.3	14	1.1	14	s
Main Block Program Time (Byte)		1.7		1.8		1.6		1.2		s
Main Block Program Time (Word)		1.1		0.9		0.8		0.6		s
Byte Program Time		10		10		8		8		µs
Word Program Time		13		13		8		8		µs

NOTES:

1. All numbers are sampled, not 100% tested.
2. Max erase times are specified under worst case conditions. The max erase times are tested at the same value independent of V_{CC} and V_{PP}. See Note 3 for typical conditions.
3. Typical conditions are +25 °C with V_{CC} and V_{PP} at the center of the specified voltage range. Production programming using V_{CC} = 5.0 V, V_{PP} = 12.0 V typically results in a 60% reduction in programming time.
4. Contact your Intel representative for information regarding maximum byte/word program specifications.

4.9 Extended Operating Conditions

Table 11. Extended Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		–40	+85	°C
V_{CC}	3.3 V V_{CC} Supply Voltage (± 0.3 V)	1	3.0	3.6	Volts
	5 V V_{CC} Supply Voltage (10%)	2	4.50	5.50	Volts

NOTES:

1. AC specifications are valid at both voltage ranges. See *DC Characteristics* tables for voltage range-specific specifications.
2. 10% V_{CC} specifications apply to 80 ns and 120 ns versions in their standard test configuration.

SEE NEW DESIGN RECOMMENDATIONS

4.9.1 APPLYING V_{CC} VOLTAGES

When applying V_{CC} voltage to the device, a delay may be required before initiating device operation, depending on the V_{CC} ramp rate. If V_{CC} ramps slower than 1V/100 µs (0.01 V/µs) then no delay is required. If V_{CC} ramps faster than 1V/100 µs (0.01 V/µs), then a delay of 2 µs is required before initiating device operation. RP# = GND is recommended during power-up to protect against spurious write signals when V_{CC} is between V_{LKO} and V_{CCMIN}.

V_{CC} Ramp Rate	Required Timing
≤ 1V/100 µs	No delay required.
> 1V/100 µs	A delay time of 2 µs is required before any device operation is initiated, including read operations, command writes, program operations, and erase operations. This delay is measured beginning from the time V_{CC} reaches V_{CCMIN} (3.0 V for 3.3 ± 0.3 V operation; and 4.5 V for 5 V operation).

NOTES:

1. These requirements must be strictly followed to guarantee all other read and write specifications.
2. To switch between 3.3 V and 5 V operation, the system should first transition V_{CC} from the existing voltage range to GND, and then to the new voltage. Any time the V_{CC} supply drops below V_{CCMIN}, the chip may be reset, aborting any operations pending or in progress.
3. These guidelines must be followed for any V_{CC} transition from GND.

4.10 Capacitance

T_A = 25 °C, f = 1 MHz

Symbol	Parameter	Note	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance	1	6	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	1	10	12	pF	V_{OUT} = 0V

NOTE:

1. Sampled, not 100% tested.

4.11 DC Characteristics—Extended Temperature Operations

Sym	Parameter	Prod	TBV-80		TBV-80 TBE-120		Unit	Test Conditions
		V_{CC}	3.3 ± 0.3 V		5 V ± 10%			
		Notes	Typ	Max	Typ	Max		
I_{IL}	Input Load Current	1		± 1.0		± 1.0	µA	$V_{CC} = V_{CC}$Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		± 10		± 10	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3	60	110	70	150	µA	**CMOS Levels** $V_{CC} = V_{CC}$ Max CE# = RP# = WP# = V_{CC} ± 0.2 V
			0.4	1.5	0.8	2.5	mA	**TTL Levels** $V_{CC} = V_{CC}$ Max CE# = RP# = BYTE# = V_{IH}
I_{CCD}	V_{CC} Deep Power-Down Current	1	0.2	8	0.2	8	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND RP# = GND ± 0.2 V
I_{CCR}	V_{CC} Read Current for Word or Byte	1,5,6	15	30	50	65	mA	**CMOS INPUTS** $V_{CC} = V_{CC}$ Max CE = V_{IL} f = 10 MHz (5 V) 5 MHz (3.3 V) I_{OUT} = 0 mA Inputs = GND ± 0.2 V or V_{CC} ± 0.2 V
			15	30	55	70	mA	**TTL INPUTS** $V_{CC} = V_{CC}$ Max CE# = V_{IL} f = 10 MHz (5 V) 5 MHz (3.3 V) I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}

SEE NEW DESIGN RECOMMENDATIONS

4.11 DC Characteristics—Extended Temperature Operations (Continued)

Sym	Parameter	Prod	TBV-80		TBV-80 TBE-120		Unit	Test Conditions
		V_{CC}	3.3 ± 0.3 V		5 V ± 10%			
		Note	Typ	Max	Typ	Max		
I_{CCW}	V_{CC} Program Current for Word or Byte	1,4	13	30	30	50	mA	$V_{PP} = V_{PPH}1$ (at 5 V) Program in Progress
			10	25	30	45	mA	$V_{PP} = V_{PPH}2$ (at 12 V) Program in Progress
I_{CCE}	V_{CC} Erase Current	1,4	13	30	22	45	mA	$V_{PP} = V_{PPH}1$ (at 5 V) Block Erase in Progress
			10	25	18	40	mA	$V_{PP} = V_{PPH}2$ (at 12 V) Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2	3	8.0	5	12.0	mA	CE# = V_{IH} Block Erase Suspend $V_{PP} = V_{PPH}1$ (at 5 V)
I_{PPS}	V_{PP} Standby Current	1	± 5	± 15	± 5	± 15	µA	$V_{PP} < V_{PPH}2$
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.2	10	0.2	10	µA	RP# = GND ± 0.2 V
I_{PPR}	V_{PP} Read Current	1	50	200	50	200	µA	$V_{PP} \geq V_{PPH}2$
I_{PPW}	V_{PP} Program Current for Word or Byte	1,4	13	30	13	30	mA	$V_{PP} = V_{PPH}1$ (at 5 V)
			8	25	8	25	mA	$V_{PP} = V_{PPH}2$ (at 12 V)
I_{PPE}	V_{PP} Erase Current	1,4	13	30	15	25	mA	$V_{PP} = V_{PPH}1$ (at 5 V) Block Erase in Progress
			8	25	10	20	mA	$V_{PP} = V_{PPH}2$ (at 12 V) Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1	50	200	50	200	µA	$V_{PP} = V_{PPH}$ Block Erase Suspend in Progress
$I_{RP\#}$	RP# Boot Block Unlock Current	1,4		500		500	µA	RP# = V_{HH} V_{PP} = 12 V
I_{ID}	A_9 Intelligent Identifier Current	1,4		500		500	µA	$A_9 = V_{ID}$

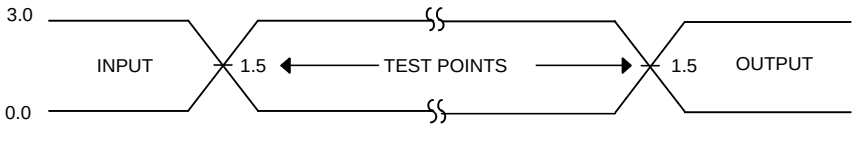
4.11 DC Characteristics—Extended Temperature Operations (Continued)

Sym	Parameter	Prod	TBV-80		TBV-80 TBE-120		Unit	Test Conditions
		V_{CC}	3.3 ± 0.3 V		5 V ± 10%			
		Notes	Typ	Max	Typ	Max		
V_{ID}	A_9 Intelligent Identifier Voltage		11.4	12.6	11.4	12.6	V	
V_{IL}	Input Low Voltage		–0.5	0.8	–0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{CC} ± 0.5V	2.0	V_{CC} ± 0.5V	V	
V_{OL}	Output Low Voltage			0.45		0.45	V	$V_{CC} = V_{CC}$ Min I_{OL} = 5.8 mA (5 V) 2 mA (3.3 V) V_{PP} = 12V
$V_{OH}1$	Output High Voltage (TTL)		2.4		2.4		V	$V_{CC} = V_{CC}$ Min I_{OH} = –2.5 mA
$V_{OH}2$	Output High Voltage (CMOS)		0.85 × V_{CC}		0.85 × V_{CC}		V	$V_{CC} = V_{CC}$ Min I_{OH} = –2.5 mA
			V_{CC}– 0.4V		V_{CC}– 0.4V		V	$V_{CC} = V_{CC}$ Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lock-Out Voltage	3	0.0	1.5	0.0	1.5	V	Complete Write Protection
$V_{PPH}1$	V_{PP} during Program/Erase Operations		4.5	5.5	4.5	5.5	V	V_{PP} at 5 V
$V_{PPH}2$			11.4	12.6	11.4	12.6	V	V_{PP} at 12 V
V_{LKO}	V_{CC} Program/Erase Lock Voltage	8	2.0		2.0		V	
V_{HH}	RP# Unlock Voltage		11.4	12.6	11.4	12.6	V	V_{PP} = 12 V Boot Block Program/ Erase

SEE NEW DESIGN RECOMMENDATIONS

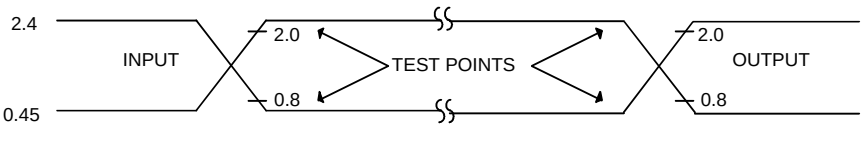
NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0 V, T = +25 °C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with device de-selected. If device is read while in erase suspend, current draw is sum of I_{CCES} and I_{CCR}.
3. Block erases and word/byte programs inhibited when $V_{PP} = V_{PPLK}$, and not guaranteed in the range between $V_{PPH}1$ and V_{PPLK}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to less than 1 mA typical, in static operation.
6. CMOS Inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL Inputs are either V_{IL} or V_{IH}.
7. For the 28F002B address pin A_{10} follows the C_{OUT} capacitance numbers.
8. For all BV/CV parts, V_{LKO} = 2.0 V for 3.3 V and 5.0 V operations.



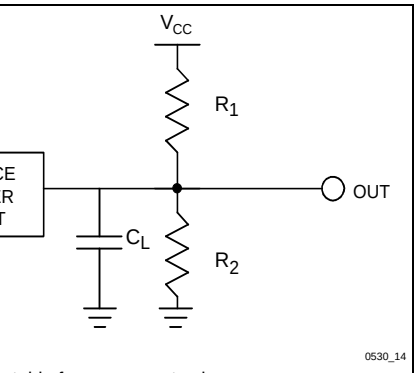
NOTE:
AC test inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Input timing begins, and output timing ends, at 1.5 V. Input rise and fall times (10% to 90%) <10 ns.

Figure 19. 3.3 V Input Range and Measurement Points



NOTE:
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) < 10 ns.

Figure 20. 5 V Input Range and Measurement Points



NOTE: See table for component values.

Figure 21. Test Configuration

Test Configuration Component Values

Test Configuration	C_L (pF)	R_1 (Ω)	R_2 (Ω)
3.3 V Standard Test	50	990	770
5 V Standard Test	100	580	390

NOTE: C_L includes jig capacitance.

SEE NEW DESIGN RECOMMENDATIONS

4.12 AC Characteristics—Read Only Operations[1]—Extended Temperature

Symbol	Parameter	Prod	TBV-80		TBV-80 TBE-120		Unit
		V_{CC}	3.3 ± 0.3 V[5]		5 V ± 10%[6]		
		Load	50 pF		100 pF		
		Notes	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time		110		80		ns
t_{AVQV}	Address to Output Delay			110		80	ns
t_{ELQV}	CE# to Output Delay	2		110		80	ns
t_{PHQV}	RP# to Output Delay			0.8		0.45	µs
t_{GLQV}	OE# to Output Delay	2		65		40	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
t_{EHQZ}	CE# to Output in High Z	3		45		25	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		45		25	ns
t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	3	0		0		ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3	0		0		ns
t_{AVFL}	Address to BYTE# High or Low	3		5		5	ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3,4		110		80	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		45		30	ns
t_{PLPH}	Reset Pulse Width	7	150		60		ns
t_{PLQZ}	RP# Low to Output High-Z			150		60	ns

NOTES:

1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to t_{CE}–t_{OE} after the falling edge of CE# without impact on t_{CE}.
3. Sampled, but not 100% tested.
4. t_{FLQV}, BYTE# switching low to valid output delay will be equal to t_{AVQV}, measured from the time DQ_{15}/A_{-1} becomes valid.
5. See *Test Configuration* (Figure 21), 3.6 V and 3.3 ± 0.3 V Standard Test component values.
6. See *Test Configuration* (Figure 21), 5 V Standard Test component values.
7. The specification t_{PLPH} is the minimum time that RP# must be held low in order to product a valid reset of the device.

SEE NEW DESIGN RECOMMENDATIONS

4.13 AC Characteristics—WE#-Controlled Write Operations[1]— Extended Temperature

Sym	Parameter	Prod	TBV-80		TBV-80 TBE-120		Unit
		V_{CC}	3.3 ±0.3 V[9]		5 V±10%[10]		
		Load	50 pF		100 pF		
		Notes	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		110		80		ns
t_{PHWL}	RP# High Recovery to WE# Going Low		0.8		0.45		µs
t_{ELWL}	CE# Setup to WE# Going Low		0		0		ns
t_{PHHWH}	Boot Block Lock Setup to WE# Going High	6,8	200		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	5,8	200		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	90		60		ns
t_{DVWH}	Data Setup to WE# Going High	4	70		60		ns
t_{WLWH}	WE# Pulse Width		90		60		ns
t_{WHDX}	Data Hold Time from WE# High	4	0		0		ns
t_{WHAX}	Address Hold Time from WE# High	3	0		0		ns
t_{WHEH}	CE# Hold Time from WE# High		0		0		ns
t_{WHWL}	WE# Pulse Width High		20		20		ns
t_{WHQV1}	Word/Byte Program Time	2,5,8	6		6		µs
t_{WHQV2}	Erase Duration (Boot)	2,5,6,8	0.3		0.3		s
t_{WHQV3}	Erase Duration (Param)	2,5,8	0.3		0.3		s
t_{WHQV4}	Erase Duration (Main)	2,5,8	0.6		0.6		s
t_{QVVL}	V_{PP} Hold from Valid SRD	5,8	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		ns
t_{PHBR}	Boot-Block Lock Delay	7,8		200		100	ns

NOTES:

1. Read timing characteristics during program and erase operations are the same as during read-only operations. Refer to *AC Characteristics* during read mode.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled internally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}. (Table 7)
4. Refer to command definition table for valid D_{IN}. (Table 7)
5. Program/erase durations are measured to valid SRD data (successful operation, SR.7 = 1)
6. For boot block program/erase, RP# should be held at V_{HH} or WP# should be held at V_{IH} until operation completes successfully.
7. Time t_{PHBR} is required for successful locking of the boot block.
8. Sampled, but not 100% tested.
9. See *Test Configuration* (Figure 21), 3.6 V and 3.3 ± 0.3 V Standard Test component values.
10. See *Test Configuration* (Figure 21), 5 V Standard Test component values.

SEE NEW DESIGN RECOMMENDATIONS

4.14 AC Characteristics—CE#-Controlled Write Operations[1, 11]— Extended Temperature

Sym	Parameter	Prod	TBV-80		TBV-80 TBE-120		Unit
		V_{CC}	3.3 ±0.3 V[9]		5 V±10%[10]		
		Load	50 pF		100 pF		
		Notes	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		110		80		ns
t_{PHEL}	RP# High Recovery to CE# Going Low		0.8		0.45		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		0		ns
t_{PHHEH}	Boot Block Lock Setup to CE# Going High	6,8	200		100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	5,8	200		100		ns
t_{AVEH}	Address Setup to CE# Going High		90		60		ns
t_{DVEH}	Data Setup to CE# Going High	3	70		60		ns
t_{ELEH}	CE# Pulse Width	4	90		60		ns
t_{EHDX}	Data Hold Time from CE# High		0		0		ns
t_{EHAX}	Address Hold Time from CE# High	4	0		0		ns
t_{EHWH}	WE# Hold Time from CE# High	3	0		0		ns
t_{EHEL}	CE# Pulse Width High		20		20		ns
t_{EHQV1}	Word/Byte Program Time	2,5	6		6		µs
t_{EHQV2}	Erase Duration (Boot)	2,5,6	0.3		0.3		s
t_{EHQV3}	Erase Duration (Param)	2,5	0.3		0.3		s
t_{EHQV4}	Erase Duration (Main)	2,5	0.6		0.6		s
t_{QVVL}	V_{PP} Hold from Valid SRD	5,8	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD	6,8	0		0		ns
t_{PHBR}	Boot-Block Lock Delay	7,8		200		100	ns

NOTES:

See *AC Characteristics—WE#-Controlled Write Operations* for notes 1 through 10.

11. Chip-Enable controlled writes: write operations are driven by the valid combination of CE# and WE# in systems where CE# defines the write pulse-width (within a longer WE# timing waveform), all set-up, hold and inactive WE# times should be measured relative to the CE# waveform.

4.15 Erase and Program Timings—Extended Temperature

T_A = –40 °C to +85 °C

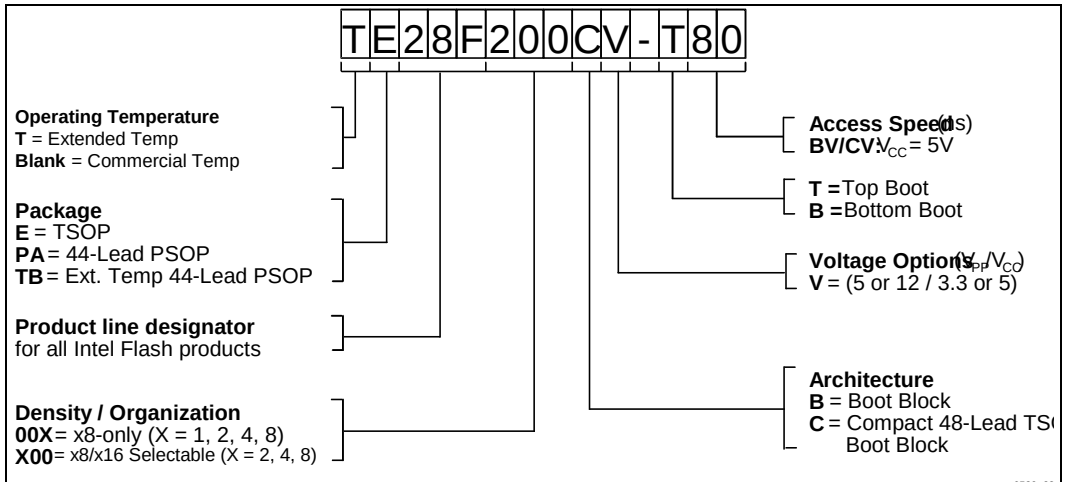
	V_{PP}	5 V ± 10%				12 V ± 5%				
	V_{CC}	3.3 ± 0.3 V		5 V ± 10%		3.3 ± 0.3 V		5 V ± 10%		
Parameter		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Boot/Parameter Block Erase Time		0.84	7	0.8	7	0.44	7	0.34	7	s
Main Block Erase Time		2.4	14	1.9	14	1.3	14	1.1	14	s
Main Block Program Time (Byte)		1.7		1.4		1.6		1.2		s
Main Block Program Time (Word)		1.1		0.9		0.8		0.6		s
Byte Program Time		10		10		8		8		µs
Word Program Time		13		13		8		8		µs

NOTES:

1. All numbers are sampled, not 100% tested.
2. Max erase times are specified under worst case conditions. The max erase times are tested at the same value independent of V_{CC} and V_{PP}. See Note 3 for typical conditions.
3. Typical conditions are +25 °C with V_{CC} and V_{PP} at the center of the specified voltage range. Production programming using V_{CC} = 5.0 V, V_{PP} = 12.0 V typically results in a 60% reduction in programming time.
4. Contact your Intel representative for information regarding maximum byte/word program specifications.

SEE NEW DESIGN RECOMMENDATIONS

5.0 ORDERING INFORMATION



VALID COMBINATIONS:

	40-Lead TSOP	44-Lead PSOP	48-Lead TSOP	56-Lead TSOP
Commercial	E28F002BVT60	PA28F200BVT60	E28F200CVT60	E28F200BVT60
	E28F002BVB60	PA28F200BVB60	E28F200CVB60	E28F200BVB60
	E28F002BVT80	PA28F200BVT80	E28F200CVT80	E28F200BVT80
	E28F002BVB80	PA28F200BVB80	E28F200CVB80	E28F200BVB80
	E28F002BVT120	PA28F200BVT120		
	E28F002BVB120	PA28F200BVB120		
Extended	TE28F002BVT80	TB28F200BVT80	TE28F200CVT80	TE28F200BVT80
	TE28F002BVB80	TB28F200BVB80	TE28F200CVB80	TE28F200BVB80

Summary of Line Items

	V_{CC}			V_{PP}		40-Ld	44-Ld	48-Ld	56-Ld	0 °C –	–40 °C –
Name	**2.7 V**	**3.3 V**	**5 V**	**5 V**	**12 V**	**TSOP**	**PSOP**	**TSOP**	**TSOP**	**+70 °C**	**+85 °C**
28F002BV		√	√	√	√	√				√	√
28F200BV		√	√	√	√		√		√	√	√
28F200CV		√	√	√	√			√		√	√

SEE NEW DESIGN RECOMMENDATIONS

6.0 ADDITIONAL INFORMATION

Related Intel Information(1,2)

Order Number	Document
290530	*4-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet*
290539	*8-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet*
290599	*Smart 5 Boot Block Flash Memory Family 2, 4, 8 Mbit Datasheet*
290580	*Smart 3 Advanced Boot Block 4-Mbit, 8-Mbit, 16-Mbit Flash Memory Family Datasheet*
292200	*AP-642 Designing for Upgrade to Smart 3 Advanced Boot Block Flash Memory*
292172	*AP-617 Additional Flash Data Protection Using V_{PP}, RP#, and WP#*
292148	*AP-604 Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM*
292194	*AB-65 Migrating SmartVoltage Boot Block Flash Designs to Smart 5 Flash*
297612	*28F200BV/CV 28F002BV Specification Update*

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.

SEE NEW DESIGN RECOMMENDATIONS