

## 2N5018 2N5019

# p-channel JFETs designed for . . .

- Analog Switches
- Commutators
- Choppers

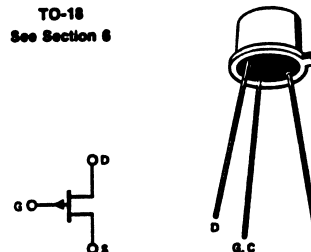
### BENEFITS

- Low Insertion Loss  
 $r_{DS(on)} < 75 \Omega$  (2N5018)
- No Offset or Error Voltages Generated by Closed Switch  
 Purely Resistive

### \*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . . . .	30 V
Gate Current . . . . .	.50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C) . . . . .	500 mW
Storage Temperature Range . . . . .	-65 to +200°C
Lead Temperature (1/16" from case for 60 seconds) . . . . .	300°C

TO-18  
 See Section 6



### \*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	2N5018		2N5019		Unit	Test Conditions
	Min	Max	Min	Max		
1 BV <sub>GSS</sub> Gate-Source Breakdown Voltage	30		30		V	I <sub>G</sub> = 1 μA, V <sub>DS</sub> = 0
2 I <sub>GSS</sub> Gate Reverse Current		2		2	nA	V <sub>GS</sub> = 15 V, V <sub>DS</sub> = 0
3 I <sub>D(off)</sub> Drain Cutoff Current		-10		-10	μA	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 12 V (2N5018)
4 I <sub>DGO</sub> Drain Reverse Current		-2		-2	nA	V <sub>DS</sub> = 7 V (2N5019)
5 I <sub>DSS</sub> Saturation Drain Current	-10		-5		mA	V <sub>GS</sub> = 7 V (2N5019)
6 V <sub>GS(off)</sub> Gate-Source Cutoff Voltage		10		5	V	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -1 μA
7 I <sub>DSS</sub> Saturation Drain Current	-10		-5		mA	V <sub>GS</sub> = 7 V (2N5019)
8 V <sub>DS(on)</sub> Drain-Source ON Voltage		-0.5		-0.5	V	V <sub>GS</sub> = 0, I <sub>D</sub> = -6 mA (2N5018), I <sub>D</sub> = -3 mA (2N5019)
9 r <sub>DS(on)</sub> Static Drain-Source ON Resistance		75		150	Ω	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0
10 r <sub>ds(on)</sub> Drain-Source ON Resistance		75		150	Ω	I <sub>D</sub> = 0, V <sub>GS</sub> = 0
11 C <sub>iss</sub> Common-Source Input Capacitance		45		45	pF	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0
12 C <sub>rss</sub> Common-Source Reverse Transfer Capacitance		10		10	pF	V <sub>DS</sub> = 0, V <sub>GS</sub> = 12 V (2N5018), V <sub>GS</sub> = 7 V (2N5019)
13 t <sub>d(on)</sub> Turn-ON Delay Time		15		15	ns	V <sub>DD</sub> = -6 V, V <sub>GS(on)</sub> = 0
14 t <sub>r</sub> Rise Time		20		75	ns	V <sub>GS(off)</sub> = 12 V, I <sub>D(on)</sub> = -6 mA, R <sub>L</sub> = 910 Ω
15 t <sub>d(off)</sub> Turn-OFF Delay Time		15		25	ns	V <sub>GS(off)</sub> = 7 V, I <sub>D(on)</sub> = -3 mA, R <sub>L</sub> = 1.8K Ω
16 t <sub>f</sub> Fall Time		50		100	ns	V <sub>GS(off)</sub> = 7 V, I <sub>D(on)</sub> = -3 mA, R <sub>L</sub> = 1.8K Ω

\*JEDEC registered data.

NOTE:

- Due to symmetrical geometry these units may be operated with source and drain leads interchanged.

