



# Small Signal MOSFET Bare Die - 2N7000

Rev 1.0  
02/26/18

N-Channel Enhancement Mode Field Effect Transistor in bare die form

## Features:

- High Density Cell Design for Low  $R_{DS(ON)}$
- Voltage Controlled Small Signal Switch
- Rugged and Reliable with Gold Back Metal
- High Reliability tested grades for Military + Space

## Ordering Information:

The following part suffixes apply:

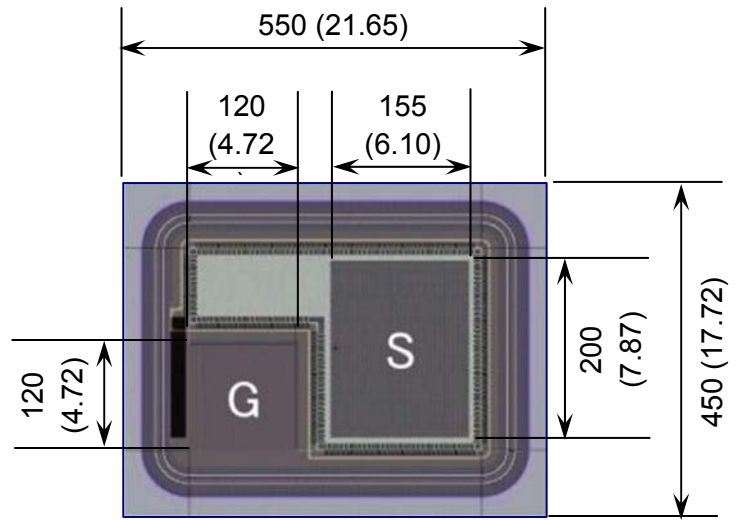
- No suffix - MIL-STD-750 /2072 Visual Inspection
- "H" - MIL-STD-750 /2072 Visual Inspection  
+ MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-750 /2072 Visual Inspection  
+ MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

[www.siliconsupplies.com/quality/bare-die-lot-qualification](http://www.siliconsupplies.com/quality/bare-die-lot-qualification)

## Die Dimensions in $\mu\text{m}$ (mils)



**G = GATE S = SOURCE**

**DIE BACK = DRAIN**

## Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- With additional electrical selection – On request
- Sawn as pairs or adjacent pair pick – On request
- Assembled in metal or ceramic package – On request

## Mechanical Specification

Die Size (Excluding Saw Street)	550 x 450 22 x 18	$\mu\text{m}$ mils
Gate Pad Size	120 x 120 4.72 x 4.72	$\mu\text{m}$ mils
Source Pad Size	155 x 200 6.10 x 7.87	$\mu\text{m}$ mils
Die Thickness	140 ( $\pm 20$ ) 5.51 ( $\pm 0.79$ )	$\mu\text{m}$ mils
Top Metal Composition	Al-Si 4.6 $\mu\text{m}$	
Back Metal Composition	Au 0.9 $\mu\text{m}$	





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## Absolute Maximum Ratings<sup>1</sup> $T_J = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	VALUE	UNIT
Drain-to-Source Voltage	$V_{DSS}$	60	V
Drain-Gate Voltage ( $R_{GS} \leq 1M\Omega$ )	$V_{DGR}$	60	V
Gate-Source Voltage - Continuous	$V_{GSS}$	$\pm 20$	V
Gate-Source Voltage – Non Repetitive ( $t_p < 50\mu s$ )		$\pm 40$	
Maximum Drain Current - Continuous	$I_D$	200	mA
Maximum Drain Current - Pulsed		500	
Maximum Power Dissipation Derated above $25^\circ\text{C}^2$	$P_D$	400	mW
		3.2	$\text{mW}/^\circ\text{C}$
Junction & Storage Temperature	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
<b>THERMAL CHARACTERISTICS</b>			
Thermal Resistance, Junction to Ambient <sup>2</sup>	$R_{\theta JA}$	312.5	$^\circ\text{C}/\text{W}$

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.
2. Power dissipation & thermal characterisation in TO-92 package. Performance at die level dependent on assembly method and substrate choice.

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS<sup>3</sup></b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 10\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 48V, V_{GS} = 0$	-	-	1	$\mu A$
		$V_{DS} = 48V, V_{GS} = 0, T_J = 125^\circ\text{C}$	-	-	1	mA
Gate-Body Leakage, Forward	$I_{GSSF}$	$V_{GS} = 15V, V_{DS} = 0V$	-	-	10	nA
Gate-Body Leakage, Reverse	$I_{GSSR}$	$V_{GS} = -15V, V_{DS} = 0V$	-	-	-10	nA
<b>ON CHARACTERISTICS<sup>3</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1mA$	0.8	2.1	3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 500mA$	-	1.2	5	$\Omega$
		$V_{GS} = 10V, I_D = 500mA, T_J = 125^\circ\text{C}$	-	1.9	9	
		$V_{GS} = 4.5V, I_D = 75mA$	-	1.8	5.3	
Drain-Source On-Voltage	$V_{DS(ON)}$	$V_{GS} = 10V, I_D = 500mA$	-	0.6	2.5	V
		$V_{GS} = 4.5V, I_D = 75mA$	-	0.14	0.4	V
On-State Drain Current	$I_{D(ON)}$	$V_{GS} = 4.5V, V_{DS} = 10V$	75	600	-	mA
Forward Transconductance	$g_{FS}$	$V_{DS} = 10V, I_D = 200mA$	100	320	-	mS
<b>DYNAMIC CHARACTERISTICS<sup>4</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1MHz$	-	20	50	pF
Output Capacitance	$C_{oss}$		-	11	25	
Reverse Transfer Capacitance	$C_{rss}$		-	4	5	
Turn-On Time	$t_{on}$	$V_{DD} = 15V, R_L = 25\Omega, I_D = 500mA, V_{GS} = 10V, R_{GEN} = 25\Omega$	-	-	10	ns
Turn-Off Time	$t_{off}$		-	-	10	

3. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Not production testing in die form, characterized by chip design & tested in package LAT.





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## Typical Electrical Characteristics

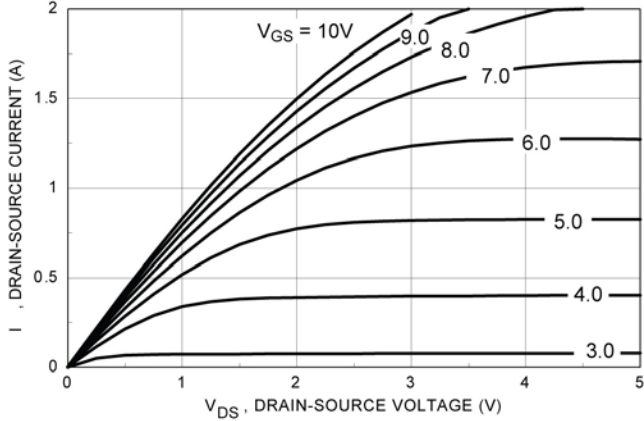


Fig 1 – On-Region Characteristics

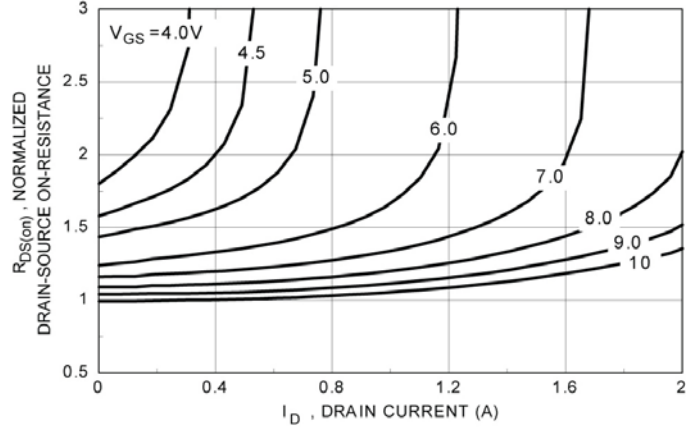


Fig 2 – On-Resistance Variation with Gate Voltage and Drain Current

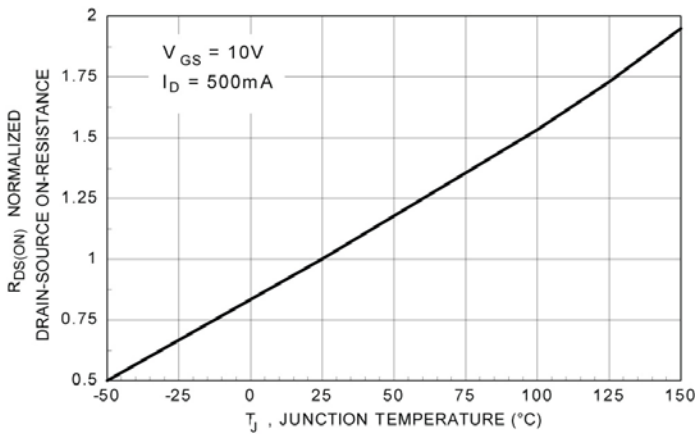


Fig 3 – On-Resistance Variation with Temperature

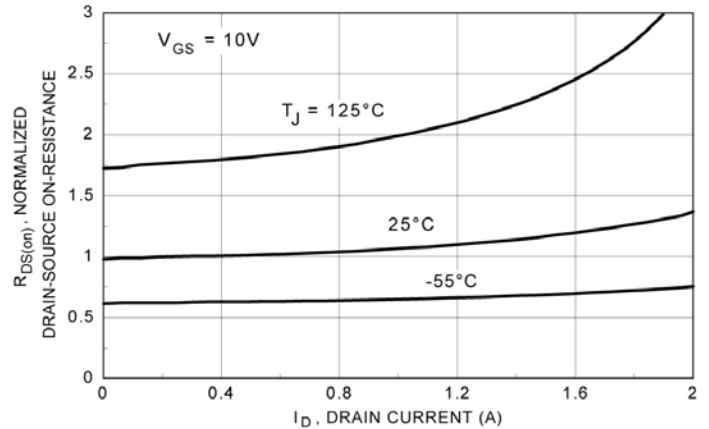


Fig 4 – On-Resistance Variation with Drain Current and Temperature

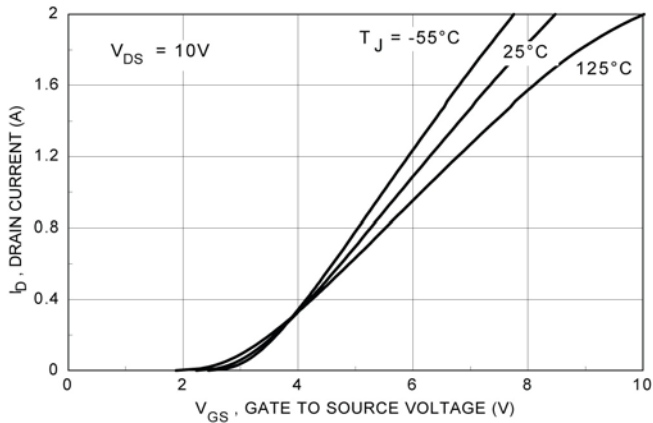


Fig 5 – Transfer Characteristics

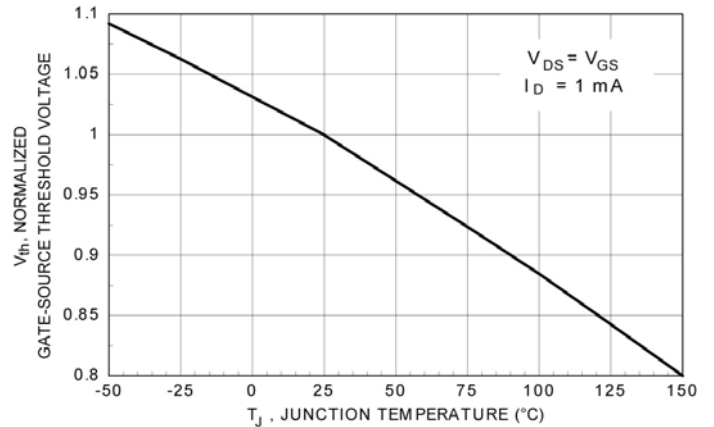


Fig 6 – Gate Threshold variation with Temperature





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## Typical Electrical Characteristics continued

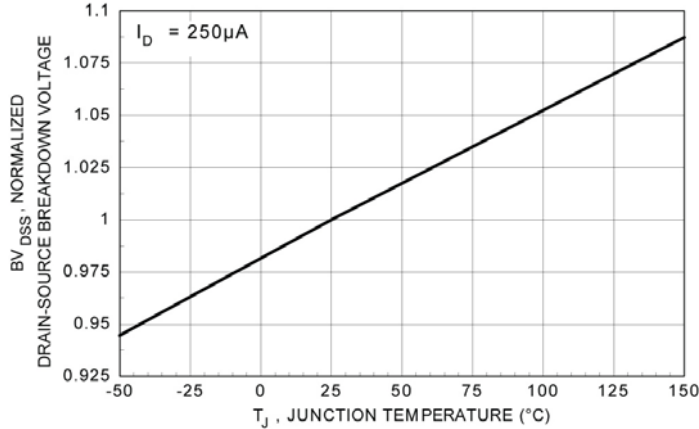


Fig 7 – Gate Threshold variation with Temperature

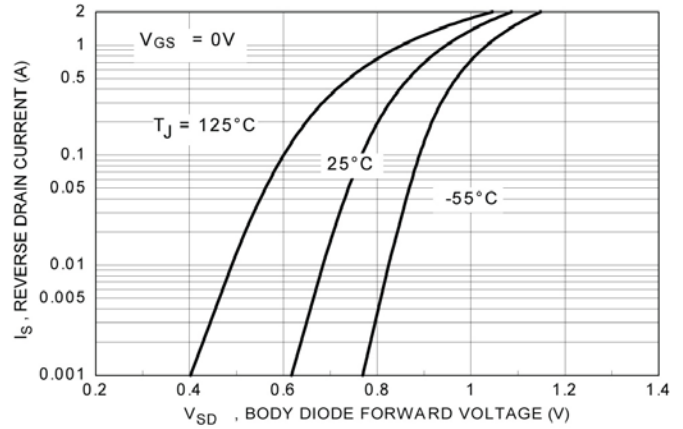


Fig 8 – Body Diode Forward Voltage variation with Temperature

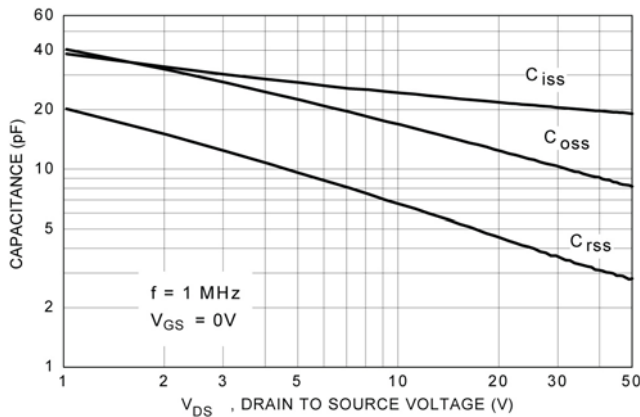


Fig 9 – Capacitance Characteristics

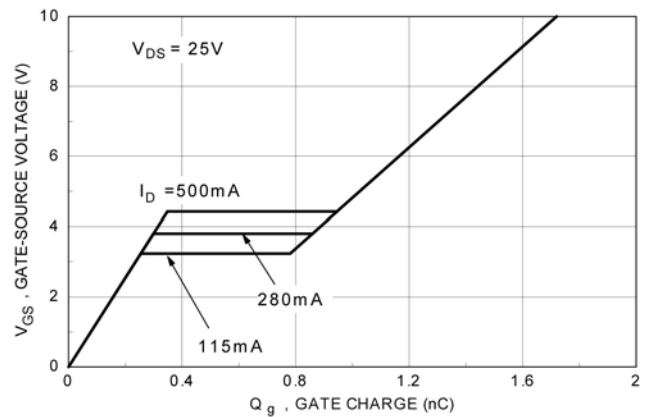


Fig 10 – Gate Charge Characteristics

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