



## N-Channel Enhancement-Mode Vertical DMOS FETs

### Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{ISS}$  and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ High input impedance and high gain

### Applications

- ▶ Motor controls
- ▶ Converters
- ▶ Amplifiers
- ▶ Switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### Ordering Information

Part Number	Package Option	Packing
2N7002-G	TO-236AB (SOT-23)	3000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package.  
Contact factory for Wafer / Die availability.  
Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

### Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSS}$
Drain-to-gate voltage	$BV_{DGS}$
Gate-to-source voltage	$\pm 30V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

### Typical Thermal Characteristics

Package	$\theta_{ja}$
TO-236AB (SOT-23)	$203^{\circ}C/W$

\* Mounted on FR4 board; 25mm x 25mm x 1.57mm

### General Description

The Supertex 2N7002 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Product Summary

$BV_{DSX}/BV_{DGS}$ (V)	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)
60V	$7.5\Omega$	500mA

### Pin Configuration



### Product Marking

**702W** W = Code for week sealed  
\_\_\_\_\_ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-236AB (SOT-23)

### Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup>	$I_D$ (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	$I_{DR}$ <sup>†</sup>	$I_{DRM}$
TO-236AB	115mA	800mA	0.36W	115mA	800mA

**Notes:**

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .

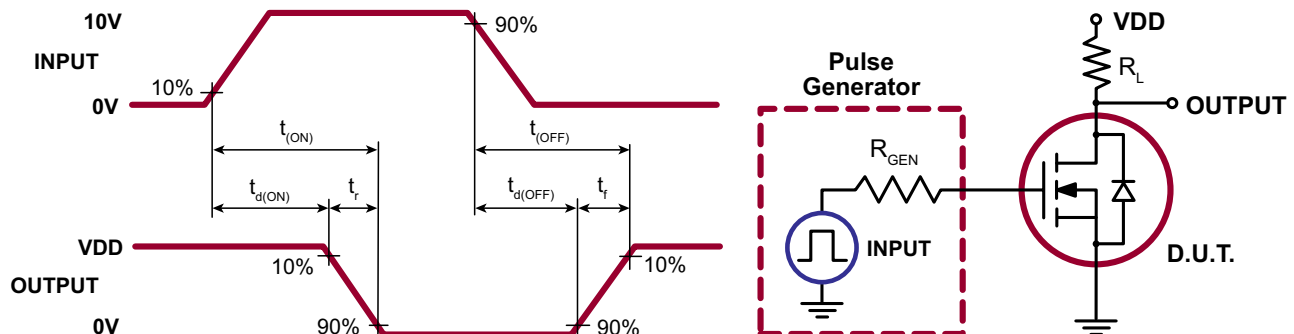
### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-Source breakdown voltage	60	-	-	V	$V_{GS} = 0V, I_D = 10\mu A$
$V_{GS(th)}$	Gate threshold voltage	1.0	-	2.5	V	$V_{GS} = V_{DS}, I_D = 250\mu A$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-5.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 250\mu A$
$I_{GSS}$	Gate body leakage current	-	-	$\pm 100$	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate voltage drain current	-	-	1.0	$\mu A$	$V_{GS} = 0V, V_{DS} = \text{Max rating}$
		-	-	500		$V_{GS} = 0V, V_{DS} = 0.8\text{Max rating}, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state Drain current	500	-	-	mA	$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source on-state resistance	-	-	7.5	$\Omega$	$V_{GS} = 5.0V, I_D = 50mA$
		-	-	7.5		$V_{GS} = 10V, I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/ $^\circ\text{C}$	$V_{GS} = 10V, I_D = 500mA$
$G_{FS}$	Forward transconductance	80	-	-	mmho	$V_{DS} = 25V, I_D = 500mA$
$C_{ISS}$	Input capacitance	-	-	50	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$
$C_{OSS}$	Common Source output capacitance	-	-	25		
$C_{RSS}$	Reverse transfer capacitance	-	-	5.0		
$t_{(ON)}$	Turn-on time	-	-	20	ns	$V_{DD} = 30V, I_D = 200mA, R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-off time	-	-	20		
$V_{SD}$	Diode forward voltage drop	-	1.2	-	V	$V_{GS} = 0V, I_{SD} = 200mA$
$t_{rr}$	Reverse recovery time	-	400	-	ns	$V_{GS} = 0V, I_{SD} = 800mA$

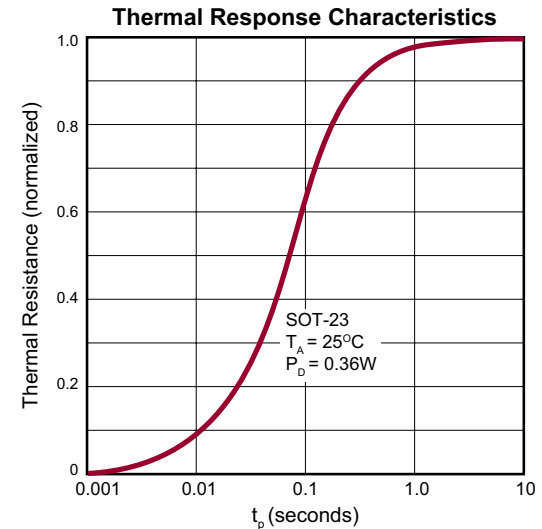
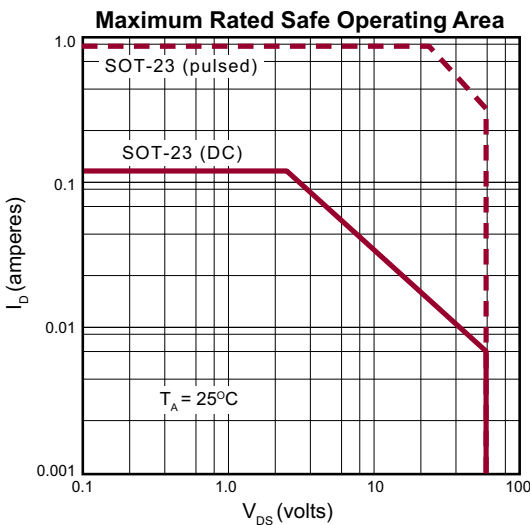
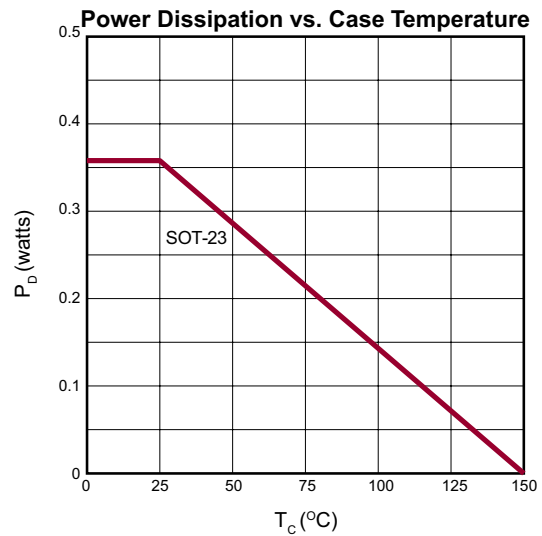
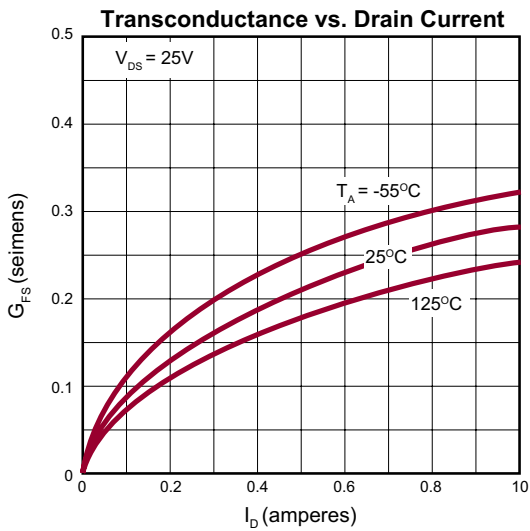
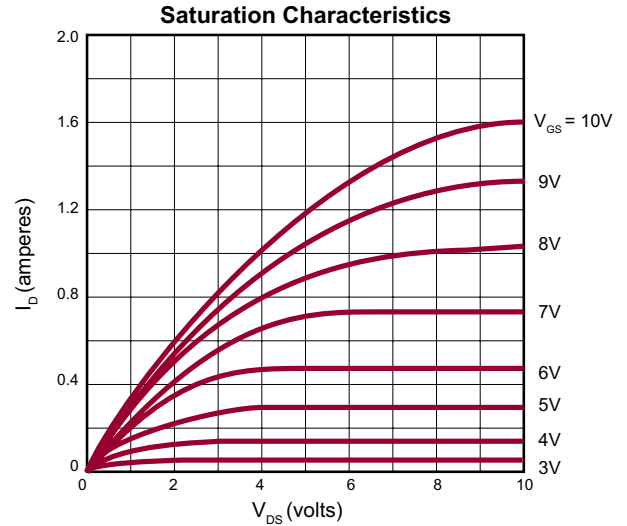
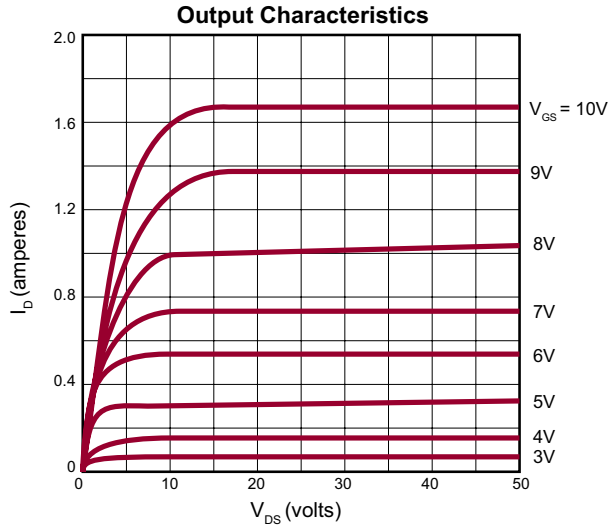
**Notes:**

1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

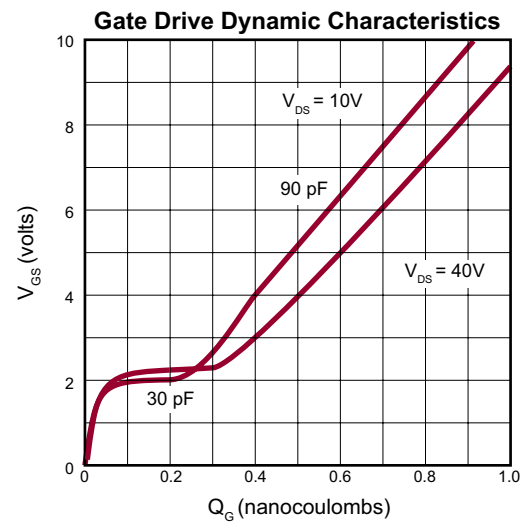
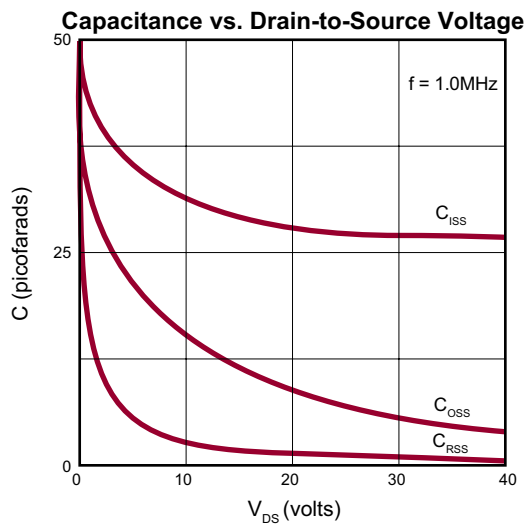
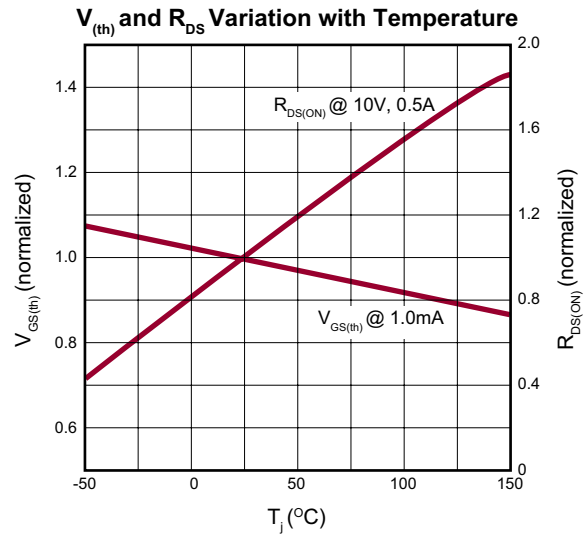
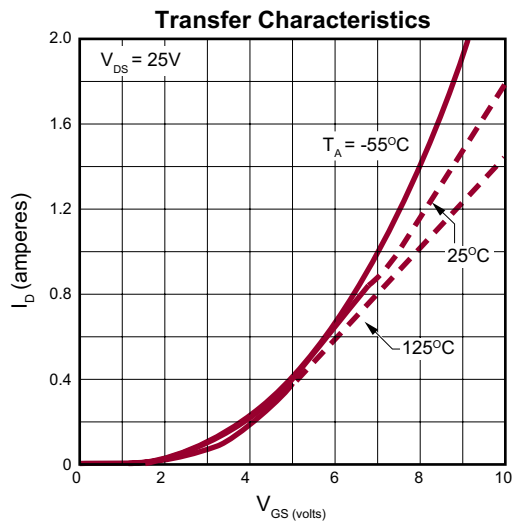
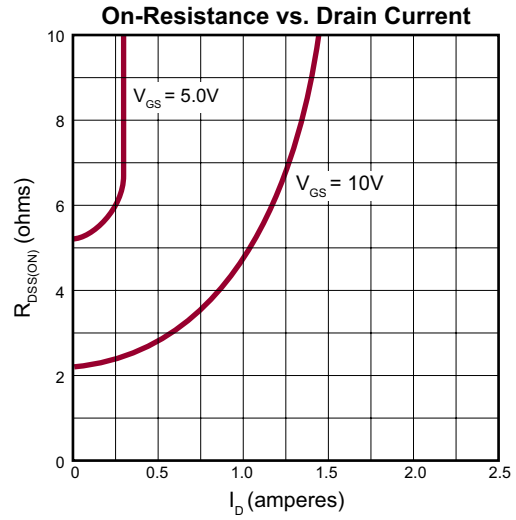
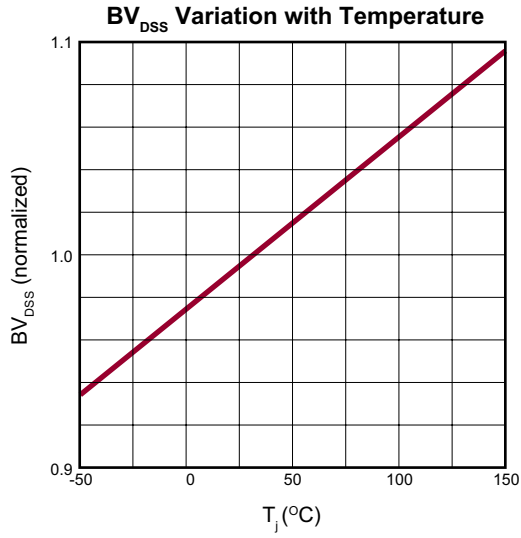
### Switching Waveforms and Test Circuit



# Typical Performance Curves

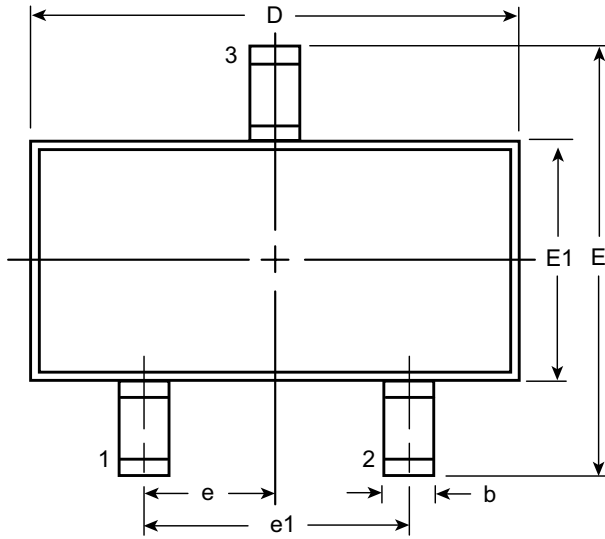


Typical Performance Curves (cont.)

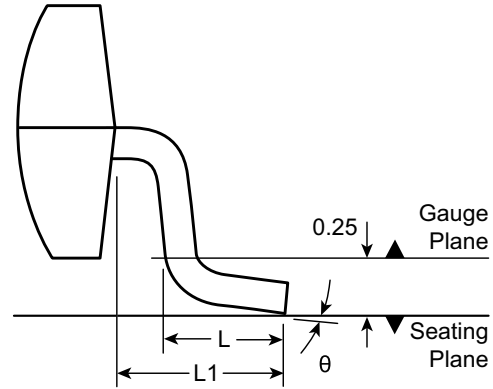


### 3-Lead TO-236AB (SOT-23) Package Outline (K1)

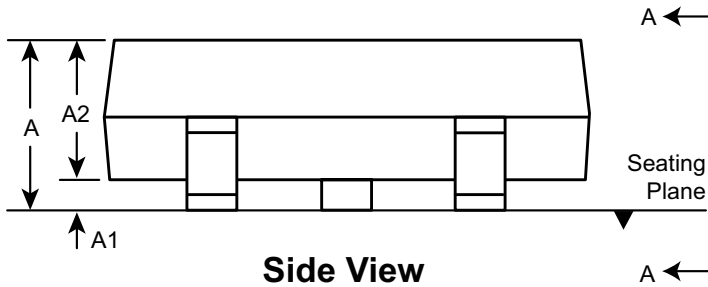
2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



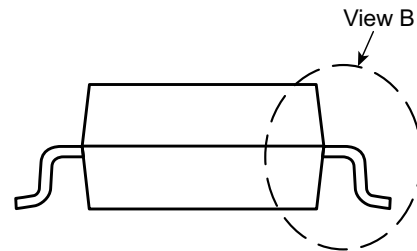
**Top View**



**View B**



**Side View**



**View A - A**

Symbol	A	A1	A2	b	D	E	E1	e	e1	L	L1	$\theta$	
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20 <sup>†</sup>	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.

<sup>†</sup> This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO236ABK1, Version C041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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