

**Silicon PNP Power Transistors**

**2SA1860**

**DESCRIPTION**

- With TO-3PML package
- Complement to type 2SC4886

**APPLICATIONS**

- Audio and general purpose

**PINNING**

PIN	DESCRIPTION
1	Emitter
2	Collector
3	Base

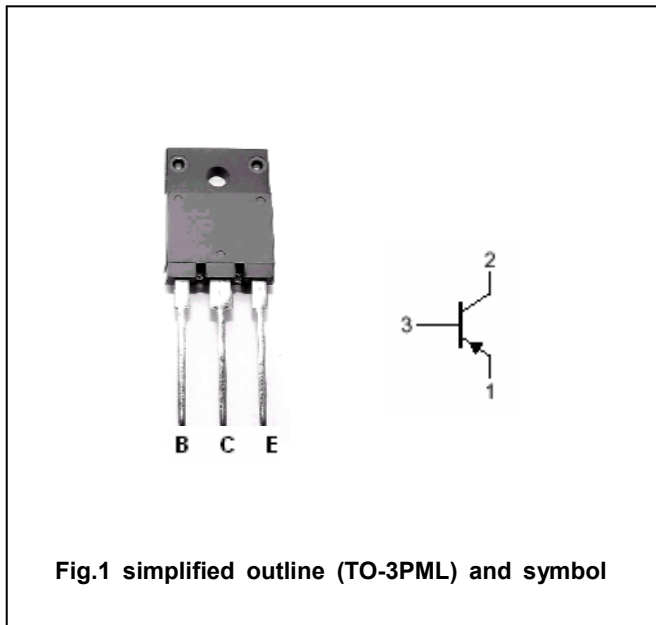


Fig.1 simplified outline (TO-3PML) and symbol

**Absolute maximum ratings(Tc=25°C)**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V <sub>CBO</sub>	Collector-base voltage	Open emitter	-150	V
V <sub>CEO</sub>	Collector-emitter voltage	Open base	-150	V
V <sub>EBO</sub>	Emitter-base voltage	Open collector	-5	V
I <sub>C</sub>	Collector current		-14	A
I <sub>B</sub>	Base current		-3	A
P <sub>C</sub>	Collector power dissipation	T <sub>C</sub> =25°C	80	W
T <sub>j</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature		-55~150	°C

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## CHARACTERISTICS

T<sub>j</sub>=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>(BR)CEO</sub>	Collector-emitter breakdown voltage	I <sub>C</sub> =-25mA; I <sub>B</sub> =0	-150			V
V <sub>CEsat</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =-5 A; I <sub>B</sub> =-0.5 A			-2.0	V
I <sub>CBO</sub>	Collector cut-off current	V <sub>CB</sub> =-150V; I <sub>E</sub> =0			-100	μA
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =-5V; I <sub>C</sub> =0			-100	μA
h <sub>FE</sub>	DC current gain	I <sub>C</sub> =-5A ; V <sub>CE</sub> =-4V	50		180	
f <sub>T</sub>	Transition frequency	I <sub>C</sub> =-2A ; V <sub>CE</sub> =-12V		50		MHz
C <sub>OB</sub>	Output capacitance	I <sub>E</sub> =0; V <sub>CB</sub> =-10V; f=1MHz		400		pF

## Switching times

t <sub>on</sub>	Turn-on time	I <sub>C</sub> =-5A; R <sub>L</sub> =12Ω I <sub>B1</sub> =-I <sub>B2</sub> =-0.5A V <sub>CC</sub> =-60V		0.25		μs
t <sub>s</sub>	Storage time			0.85		μs
t <sub>f</sub>	Fall time			0.20		μs

◆ h<sub>FE</sub> classifications

O	P	Y
50-100	70-140	90-180

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PACKAGE OUTLINE

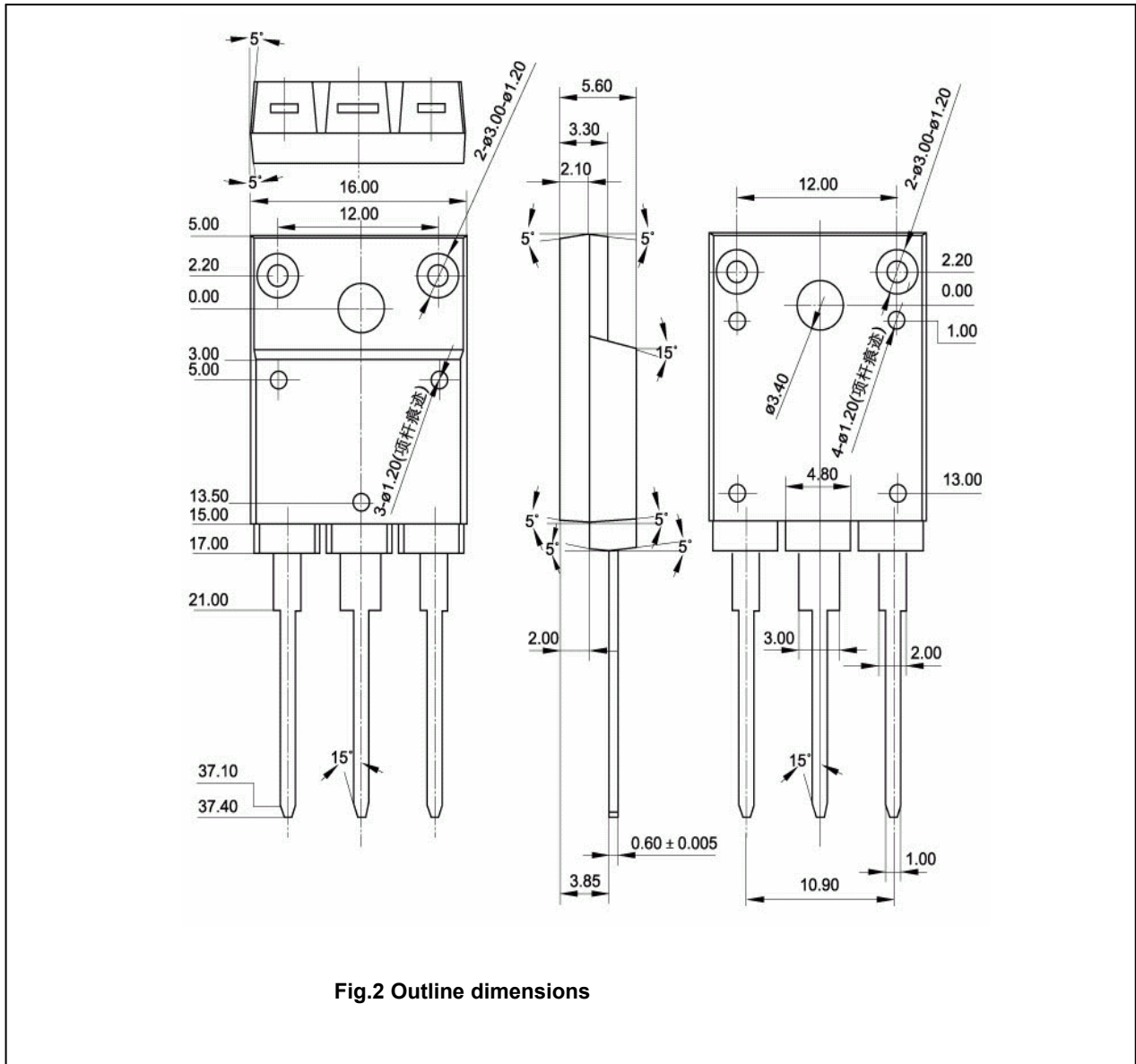


Fig.2 Outline dimensions

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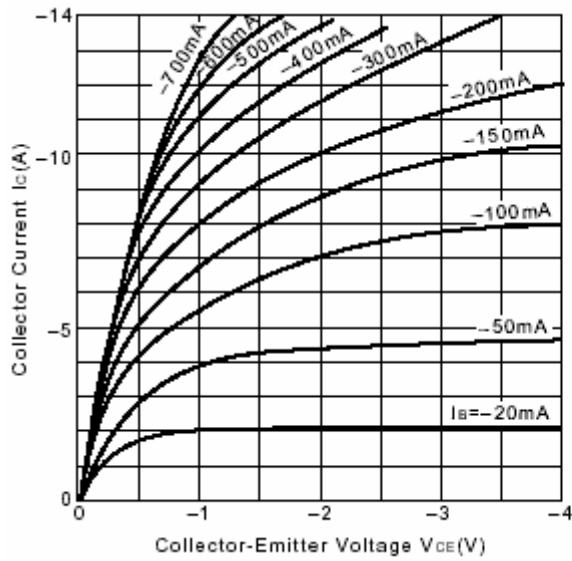


Fig.3 Static Characteristic

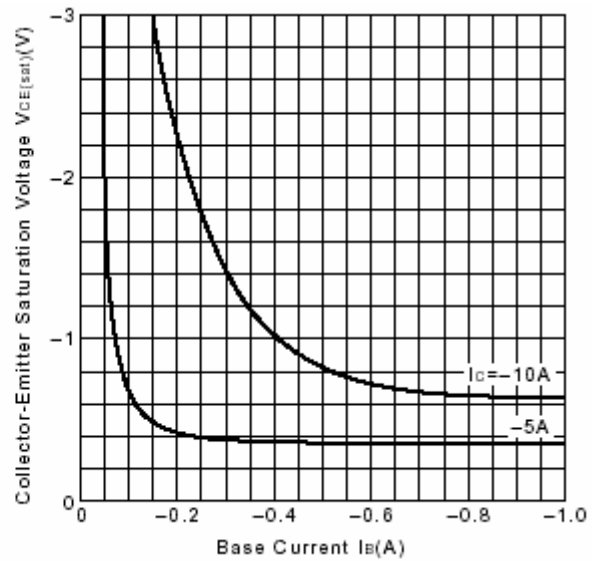


Fig.4  $V_{CE(sat)}-I_B$  Characteristics

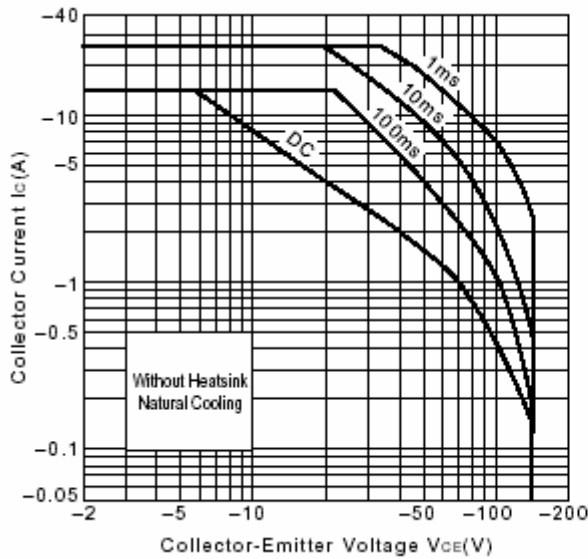


Fig.5 Safe Operating Area

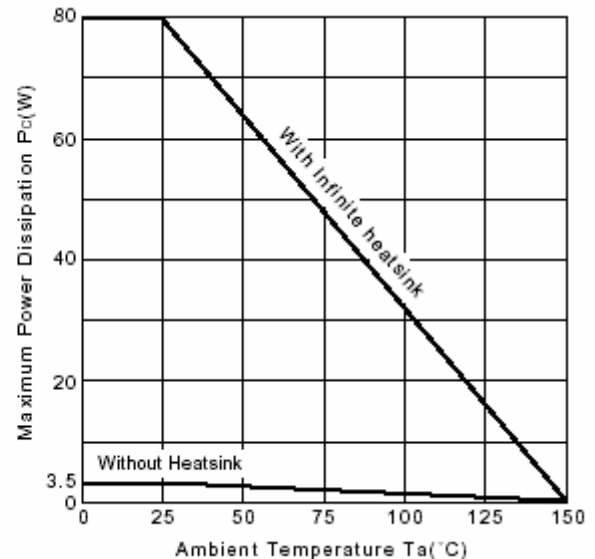


Fig.6  $P_c-T_a$  Derating

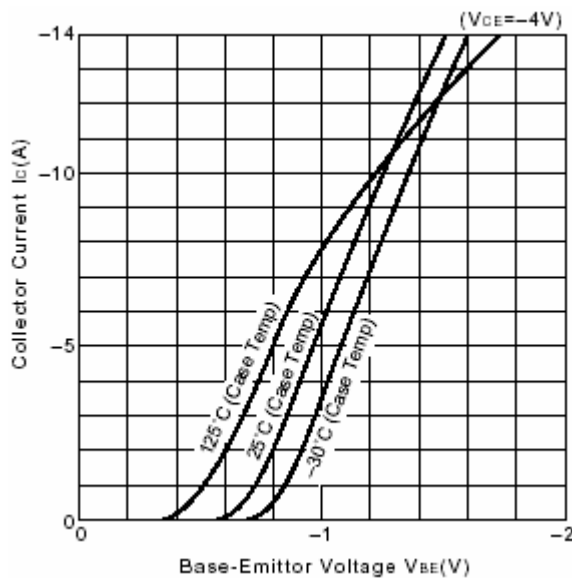


Fig.7  $I_C-V_{BE}$

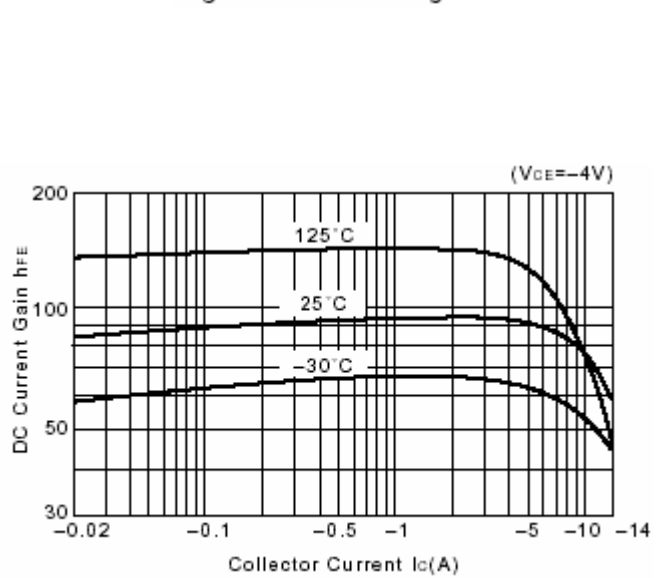


Fig.8 DC current Gain