

Silicon NPN Power Transistors

2SC1783

DESCRIPTION

- With TO-3 package
- High power dissipation
- High speed ,high current

APPLICATIONS

- For power amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

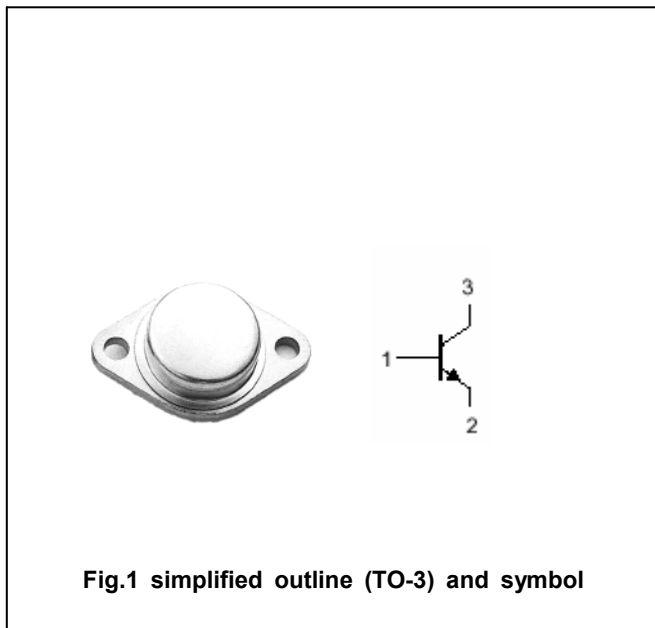


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	180	V
V_{CEO}	Collector-emitter voltage	Open base	120	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		10	A
P_C	Collector power dissipation	$T_C=25\text{ }^\circ\text{C}$	100	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =50mA ; I _B =0	120			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA ; I _C =0	6			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =5A; I _B =0.5A			1.5	V
V _{BEsat}	Base-emitter saturation voltage	I _C =5A; I _B =0.5A			2.0	V
I _{CBO}	Collector cut-off current	V _{CB} =180V; I _E =0			100	μA
I _{EBO}	Emitter cut-off current	V _{EB} =6V; I _C =0			100	μA
h _{FE}	DC current gain	I _C =3A ; V _{CE} =4V	30			
C _{OB}	Collector output capacitance	I _E =0 ; V _{CB} =10V; f=1MHz		165		pF
f _T	Transition frequency	I _C =1A ; V _{CE} =10V		10		MHz

PACKAGE OUTLINE

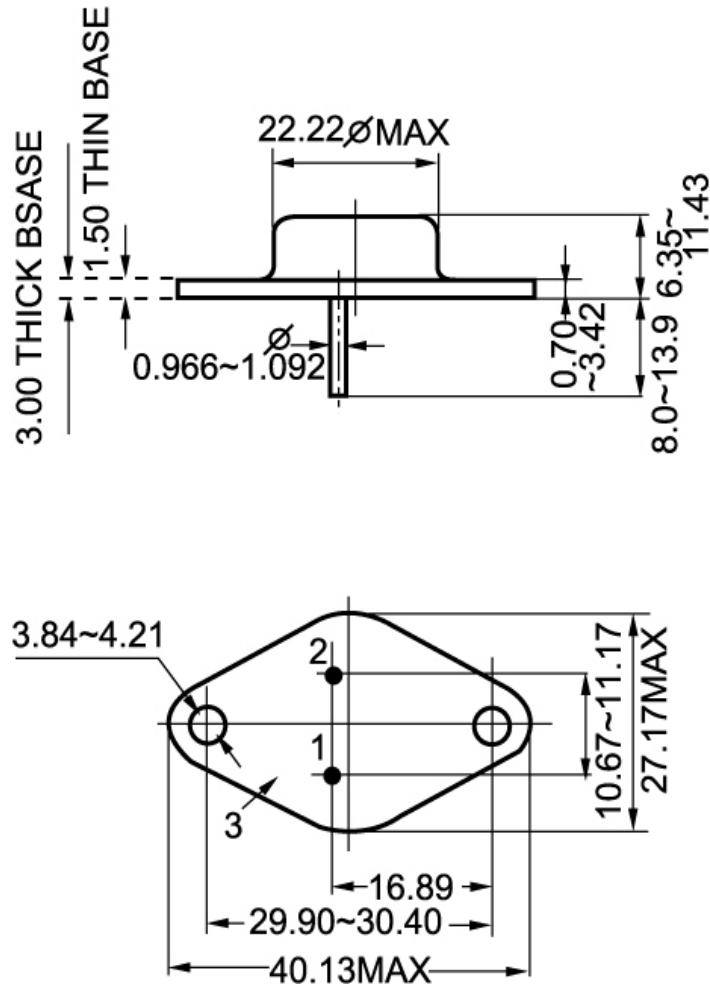


Fig.2 outline dimensions (unindicated tolerance:±0.1mm)