Silicon NPN Power Transistors 2SD1650

DESCRIPTION

- With TO-3PML package
- Built-in damper diode
- High breakdown voltage
- High speed switching

APPLICATIONS

- For color TV horizontal output applications

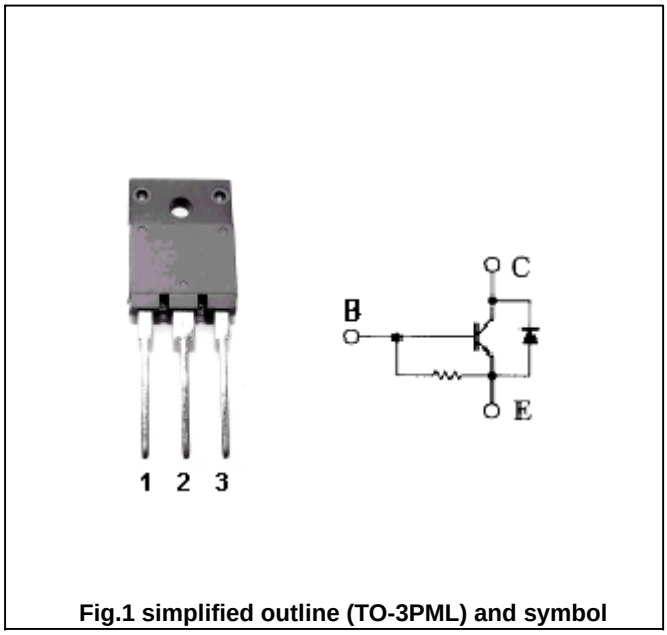

Fig.1 simplified outline (TO-3PML) and symbol

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

ABSOLUTE MAXIMUM RATINGS AT Tc=25℃

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{CEO}	Collector-emitter voltage	Open base	800	
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		3.5	A
P_C	Collector power dissipation	T_C=25℃	50	W
T_j	Junction temperature		150	℃
T_{stg}	Storage temperature		-55~150	℃

Silicon NPN Power Transistors 2SD1650

CHARACTERISTICS

Tj=25℃ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CEO}	Collector-emitter sustaining voltage	I_C=0.1A , I_B=0	800			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=2.5A ;I_B=0.8A		5.0	8.0	V
V_{BEsat}	Emitter-base saturation voltage	I_C=2.5A ;I_B=0.8A			1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=800V; I_E=0			10	μA
I_{CES}	Collector cut-off current	V_{CES}=1500V; R_{BE}=∞			1.0	mA
I_{EBO}	Emitter cut-off current	V_{EB}=4V; I_C=0	40		130	mA
h_{FE}	DC current gain	I_C=0.5A ; V_{CE}=5V	8			
f_T	Transition frequency	I_C=0.5A ; V_{CE}=10V		3		MHz
V_F	Diode forward voltage	I_F=3.5A			2.0	V

Silicon NPN Power Transistors 2SD1650

PACKAGE OUTLINE

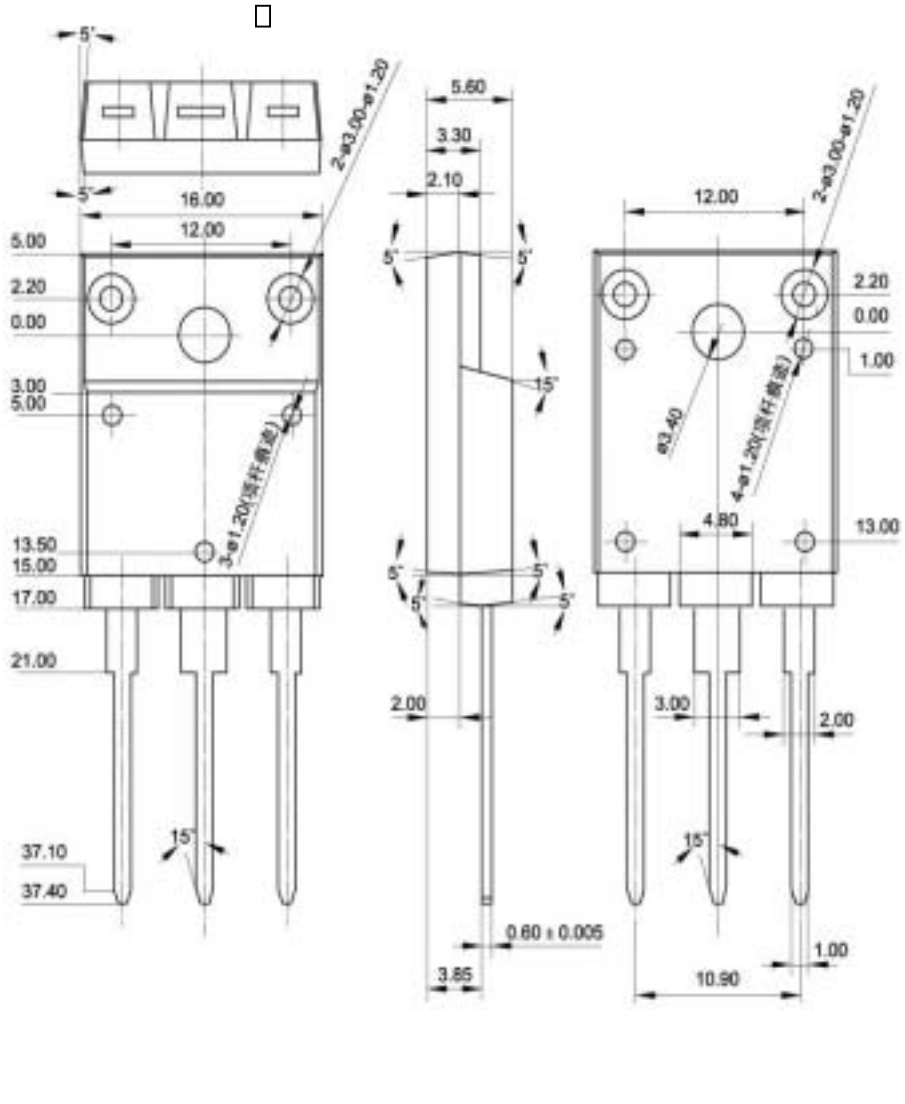

Fig.2 Outline dimensions (unindicated tolerance:±0.15 mm)