# TOSHIBA

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

# 2SJ347

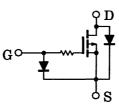
## High Speed Switching Applications Analog Switch Applications

- Low threshold voltage:  $V_{th} = -0.5 \sim -1.5 \text{ V}$
- High speed
- Small package
- Complementary to 2SK1830

## Marking

#### Equivalent Circuit





## Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V <sub>DS</sub>	-20	V
Gate-source voltage	V <sub>GSS</sub>	-7	V
DC drain current	I <sub>D</sub>	-50	mA
Drain power dissipation	PD	100	mW
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature range	T <sub>stg</sub>	-55~150	°C

#### 1.6±0.2 0.8±0.1 +0.1 0.2-0.05 1.6±0.2 0.5 $1.0 \pm 0.1$ 0.5 $0.15 \pm 0.05$ 0.7±0. $0 \sim 0.1$ 1. GATE 2. SOURCE 3. DRAIN SSM JEDEC \_\_\_\_ JEITA \_\_\_\_ TOSHIBA 2-2H1B

Weight: 2.4 mg (typ.)

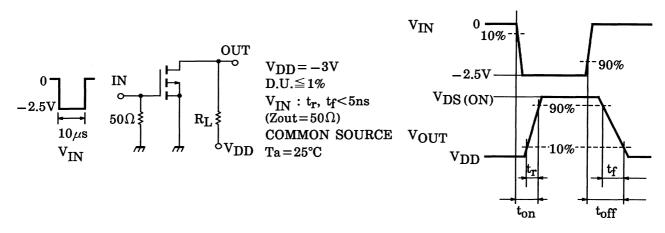
## **Electrical Characteristics (Ta = 25°C)**

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gateate leakage current		I <sub>GSS</sub>	$V_{GS} = -7 \text{ V},  V_{DS} = 0$		_	-1	μA
Drain-source breakdown voltage		V (BR) DSS	$I_D = -100 \ \mu A, \ V_{GS} = 0$	-20	_	_	V
Drain cut-off current		I <sub>DSS</sub>	$V_{DS} = -20 V, V_{GS} = 0$		_	-1	μA
Gate threshould v	oltage	V <sub>th</sub>	$V_{DS} = -3 V$ , $I_D = -0.1 mA$	-0.5	_	-1.5	V
Forward transfer admittance		Y <sub>fs</sub>	$V_{DS} = -3 V, I_D = -10 mA$	15	_	_	mS
Drain-source ON resistance		R <sub>DS (ON)</sub>	$I_D = -10$ mA, $V_{GS} = -2.5$ V	_	20	40	Ω
Input capacitance		C <sub>iss</sub>	$V_{DS}=-3~V,~V_{GS}=0,~f=1~MHz$		10.4	_	pF
Reverse transfer capacitance		C <sub>rss</sub>	$V_{DS}=-3~V,~V_{GS}=0,~f=1~MHz$	_	2.8	_	pF
Output capacitance		C <sub>oss</sub>	$V_{DS}=-3~V,~V_{GS}=0,~f=1~MHz$	_	8.4	_	pF
Switching time	Turn-on time	t <sub>on</sub>	$V_{DD} = -3 \text{ V}, \text{ I}_{D} = -10 \text{ mA}, V_{GS} = 0$ ~-2.5 V	_	0.15	_	μs
	Turn-off time	t <sub>off</sub>	$V_{DD} = -3 \text{ V}, \text{ I}_{D} = -10 \text{ mA}, V_{GS} = 0$ ~-2.5 V	_	0.13	_	

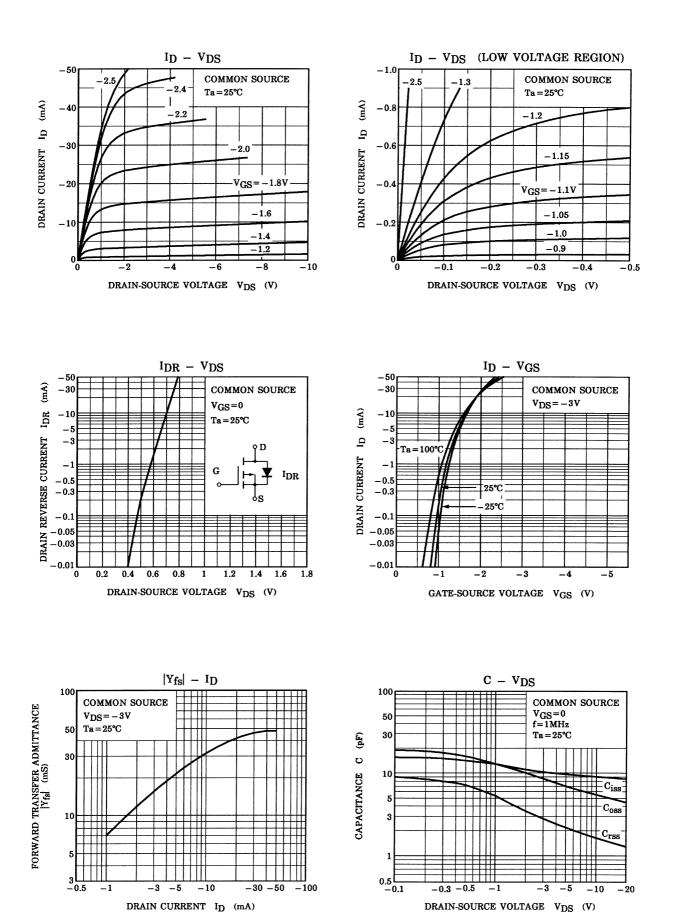
Unit: mm

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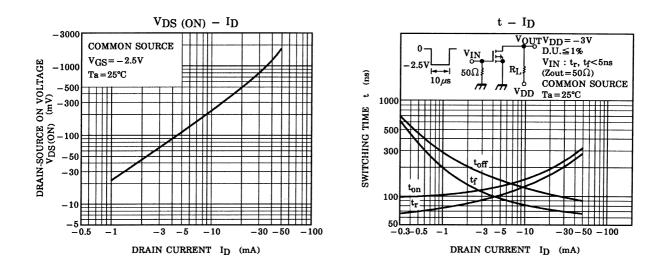
# Switching Time Test Circuit

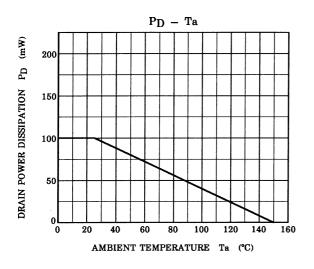


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2003-03-27





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