
2SJ387(L), 2SJ387(S)

Silicon P-Channel MOS FET

HITACHI

Application

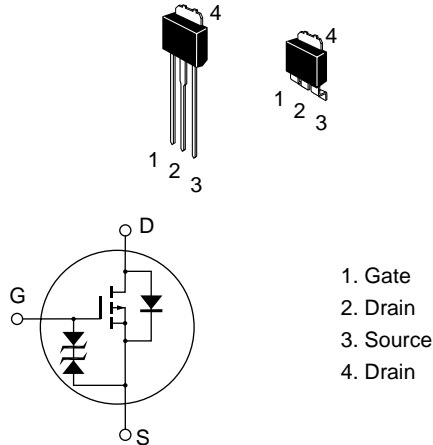
High speed power switching

Features

- Low on-resistance
- Low drive current
- 2.5 V Gate drive device can be driven from 3 V Source
- Suitable for Switching regulator, DC - DC converter

Outline

DPAK-2



2SJ387(L), 2SJ387(S)

Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|-------------------------------------|-------------|------|
| Drain to source voltage | V _{DSS} | -20 | V |
| Gate to source voltage | V _{GSS} | ±10 | V |
| Drain current | I _D | -10 | A |
| Drain peak current | I _{D(pulse)} ^{*1} | -40 | A |
| Body to drain diode reverse drain current | I _{DR} | -10 | A |
| Channel dissipation | Pch ^{*2} | 20 | W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | -55 to +150 | °C |

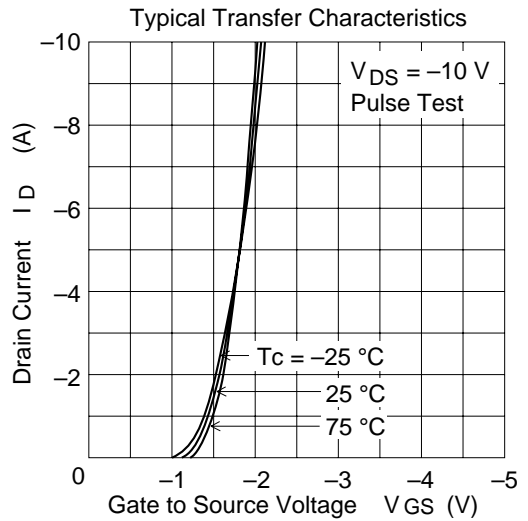
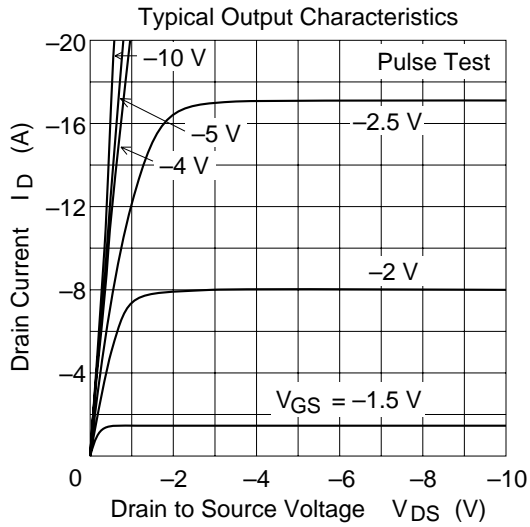
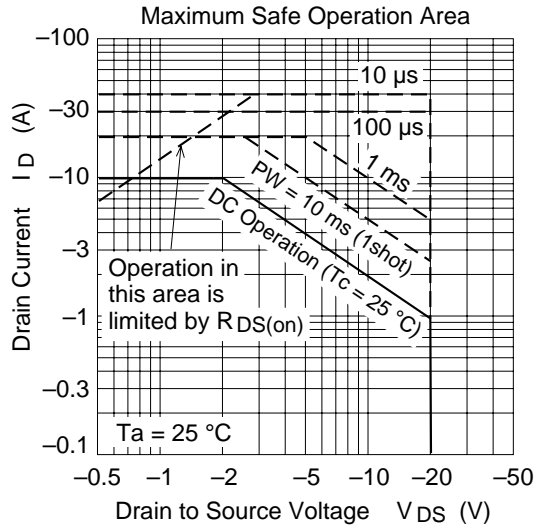
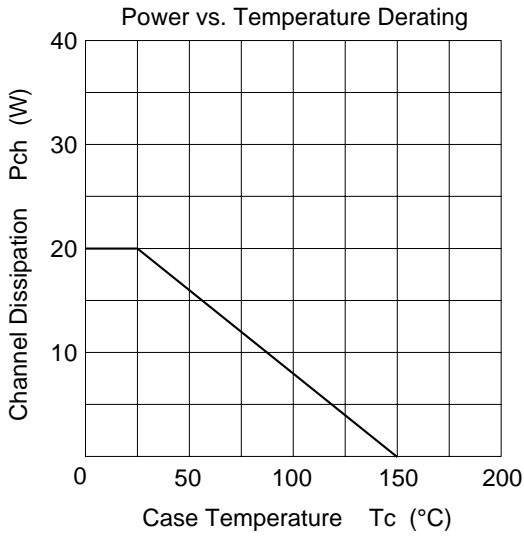
Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1 %

2. Value at Tc = 25°C

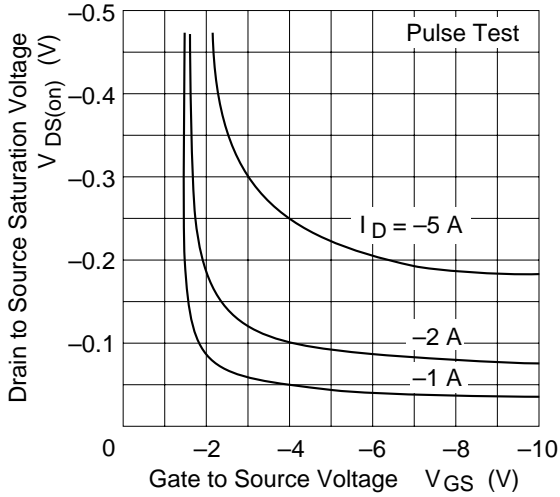
Electrical Characteristics (Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|---------------|----------|------|----------|---------------|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | -20 | — | — | V | $I_D = -10 \text{ mA}, V_{GS} = 0$ |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | ± 10 | — | — | V | $I_G = \pm 200 \text{ }\mu\text{A}, V_{DS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ± 10 | μA | $V_{GS} = \pm 6.5 \text{ V}, V_{DS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | -100 | μA | $V_{DS} = -16 \text{ V}, V_{GS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | -0.5 | — | -1.5 | V | $I_D = -1 \text{ mA}, V_{DS} = -10 \text{ V}$ |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 0.05 | 0.07 | Ω | $I_D = -5 \text{ A}$ $V_{GS} = -4 \text{ V}^{*1}$ |
| | | — | 0.07 | 0.1 | Ω | $I_D = -5 \text{ A}$ $V_{GS} = -2.5 \text{ V}^{*1}$ |
| Forward transfer admittance | $ y_{fs} $ | 7 | 12 | — | S | $I_D = -5 \text{ A}$ $V_{DS} = -10 \text{ V}^{*1}$ |
| Input capacitance | C_{iss} | — | 1170 | — | pF | $V_{DS} = -10 \text{ V}$ |
| Output capacitance | C_{oss} | — | 860 | — | pF | $V_{GS} = 0$ |
| Reverse transfer capacitance | C_{rss} | — | 310 | — | pF | $f = 1 \text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | — | 20 | — | ns | $I_D = -5 \text{ A}$ |
| Rise time | t_r | — | 325 | — | ns | $V_{GS} = -4 \text{ V}$ |
| Turn-off delay time | $t_{d(off)}$ | — | 350 | — | ns | $R_L = 2 \text{ }\Omega$ |
| Fall time | t_f | — | 425 | — | ns | |
| Body to drain diode forward voltage | V_{DF} | — | -1.0 | — | V | $I_F = -10 \text{ A}, V_{GS} = 0$ |
| Body to drain diode reverse recovery time | t_{rr} | — | 240 | — | ns | $I_F = -10 \text{ A}, V_{GS} = 0,$ $diF/dt = 20 \text{ A}/\mu\text{s}$ |

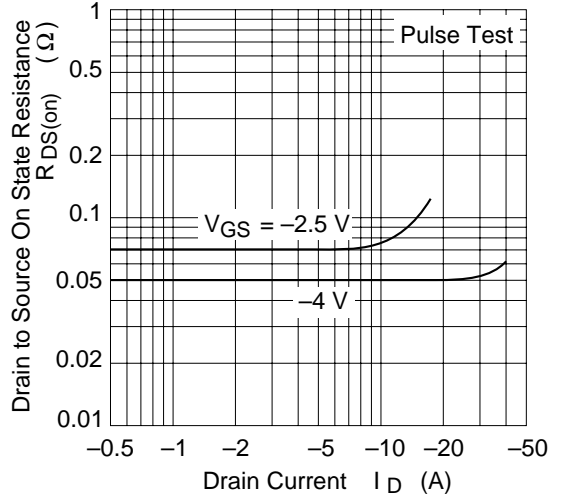
Note: 1. Pulse Test



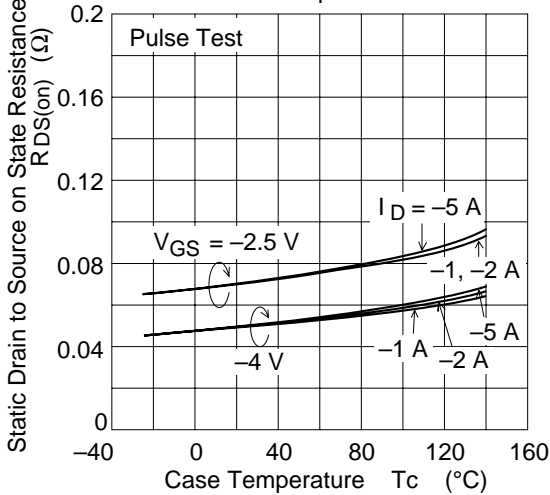
Drain to Source Saturation Voltage vs. Gate to Source Voltage



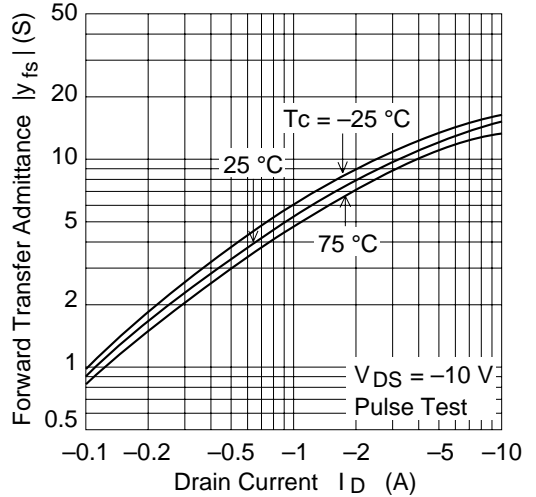
Static Drain to Source on State Resistance vs. Drain Current



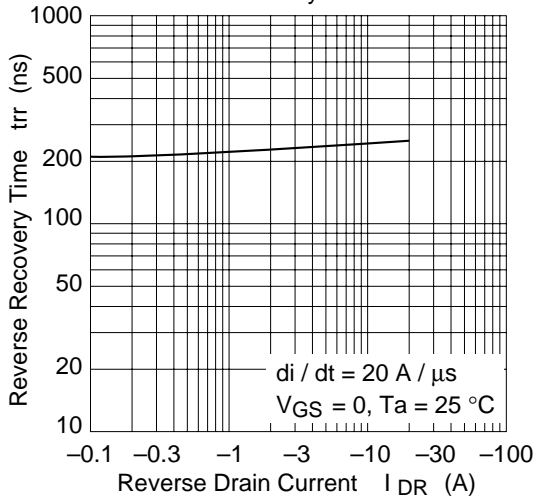
Static Drain to Source on State Resistance vs. Temperature



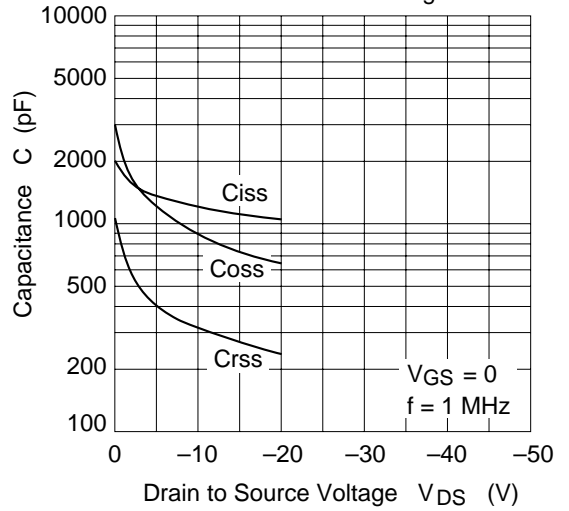
Forward Transfer Admittance vs. Drain Current



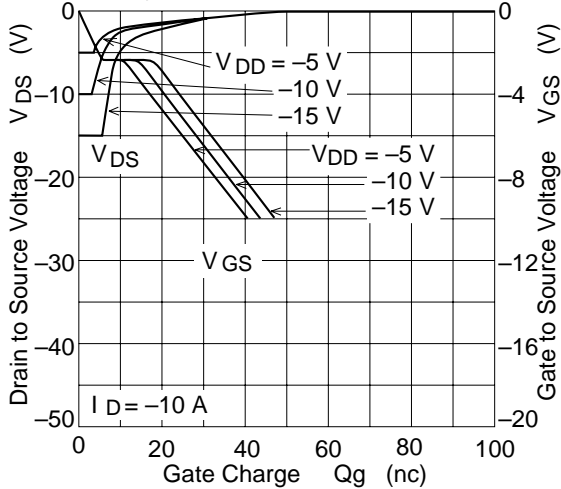
Body to Drain Diode Reverse Recovery Time



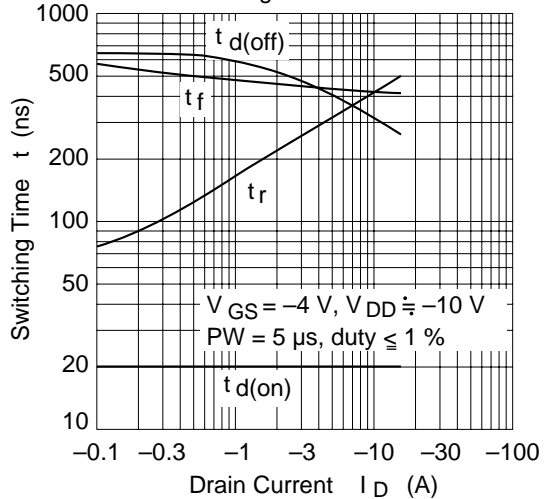
Typical Capacitance vs. Drain to Source Voltage

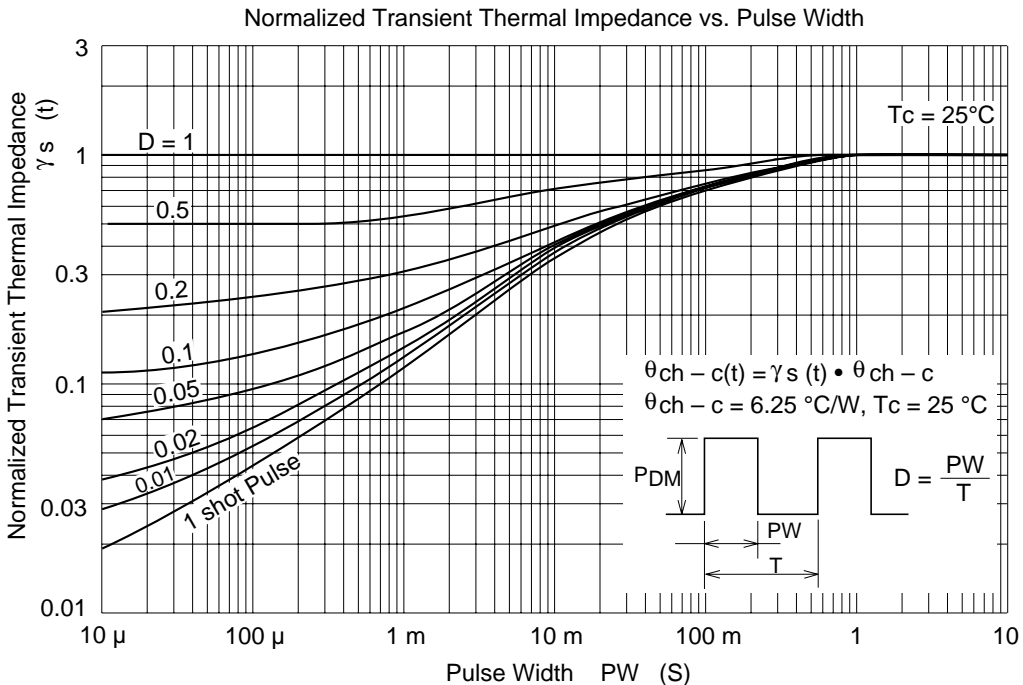
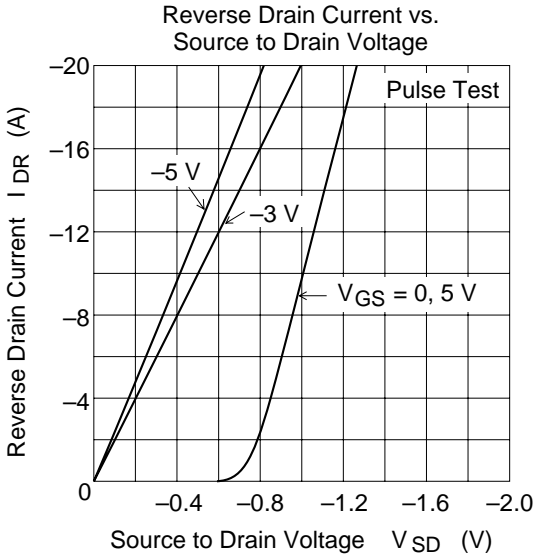


Dynamic Input Characteristics

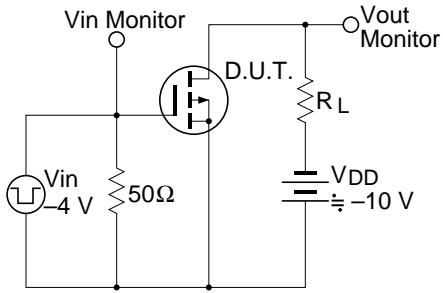


Switching Characteristics

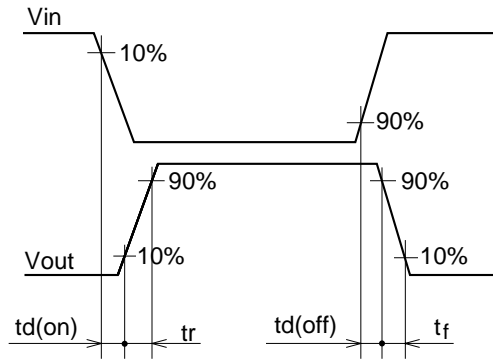


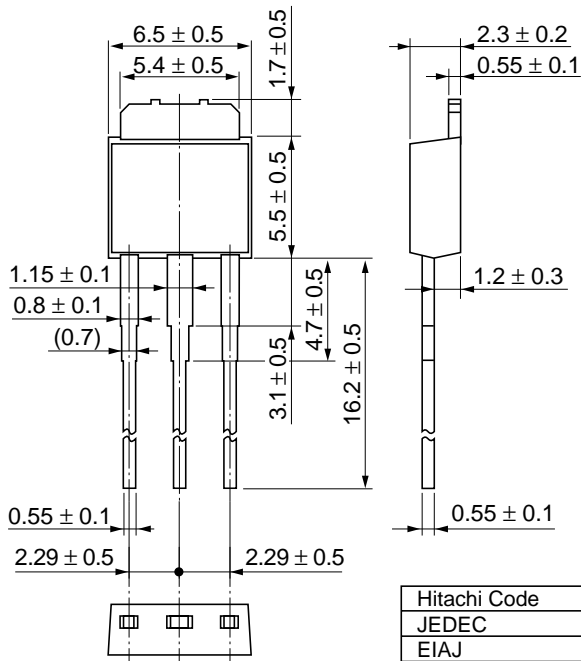


Switching Time Test Circuit



Waveforms





| | |
|--------------------------|--------------|
| Hitachi Code | DPAK (L)-(2) |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.42 g |

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