TOSHIBA FIELD EFFECT TRANSISTOR SILICON P CHANNEL MOS TYPE (L^2-π-MOS V)

2SJ511

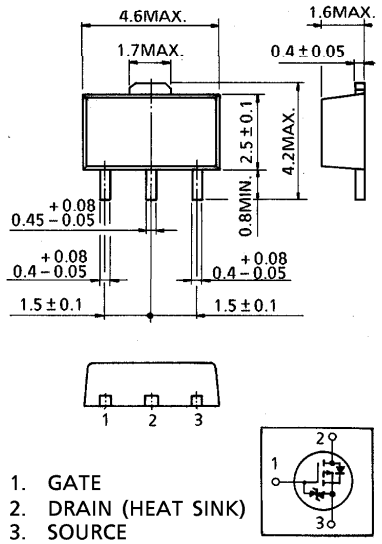
HIGH SPEED, HIGH CURRENT SWITCHING APPLICATIONS

CHOPPER REGULATOR, DC-DC CONVERTER AND MOTOR DRIVE APPLICATIONS

INDUSTRIAL APPLICATIONS

- 4V Gate Drive
- Low Drain-Source ON Resistance : $R_{DS\,(ON)} = 0.32\Omega$ (Typ.)
- High Forward Transfer Admittance : $|Y_{fs}| = 1.4S$ (Typ.)
- Low Leakage Current : $I_{DSS} = -100\mu A$ (Max.) ($V_{DS} = -30V$)
- Enhancement-Mode : $V_{th} = -0.8 \sim -2.0V$ ($V_{DS} = -10V$, $I_D = -1mA$)

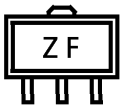
Unit in mm



JEDEC	—
EIAJ	—
TOSHIBA	2-5K1B

Weight : 0.05g (Typ.)

MARKING



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	−30	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$)		V_{DGR}	−30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	DC	I_D	−2	A
	Pulse	I_{DP}	−6	A
Drain Power Dissipation***		P_D	1.5	W
Single Pulse Avalanche Energy**		E_{AS}	55	mJ
Avalanche Current		I_{AR}	−2	A
Repetitive Avalanche Energy*		E_{AR}	0.15	mJ
Channel Temperature		T_{ch}	150	°C
Storage Temperature Range		T_{stg}	−55~150	°C

THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MAX.	UNIT
Thermal Resistance, Channel to Ambient	$R_{th\,(ch\text{-}a)}$	250	°C / W

Note ;

* Repetitive rating ; Pulse Width Limited by Max. junction temperature.

** $V_{DD} = -25V$, Starting $T_{ch} = 25°C$, $L = 10mH$, $R_G = 25\Omega$, $I_{AR} = -2A$

*** Mounted on ceramic substrate ($1inch^2 \times 0.8t$)

This transistor is an electrostatic sensitive device.
Please handle with caution.

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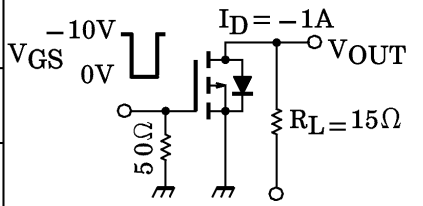
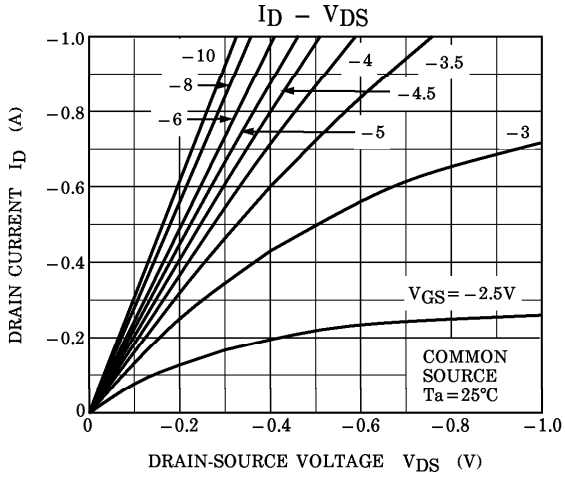
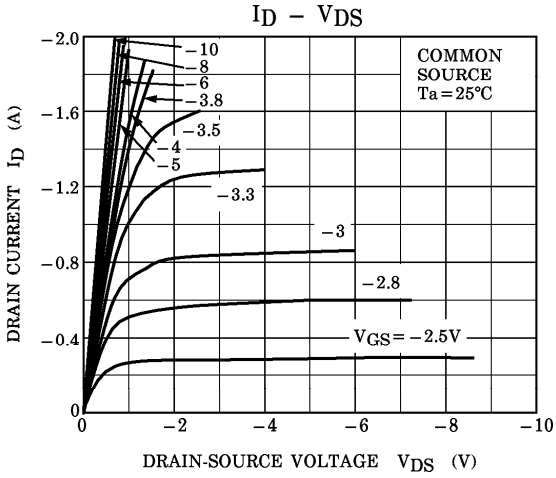
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

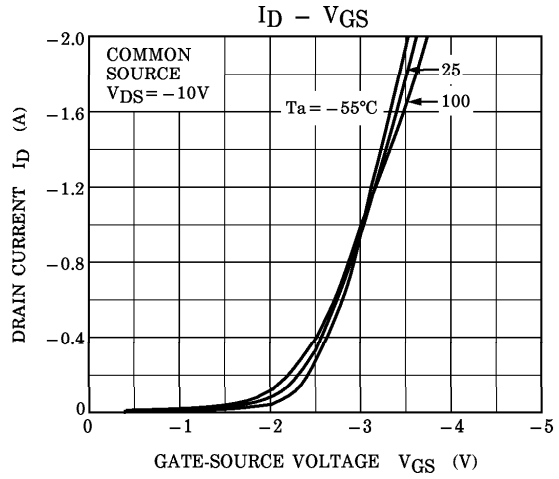
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	$V_{GS} = \pm 16V$, $V_{DS} = 0V$	—	—	±10	μA
Drain Cut-off Current		I_{DSS}	$V_{DS} = -30V$, $V_{GS} = 0V$	—	—	−100	μA
Drain-Source Breakdown Voltage		$V_{(BR)\,DSS}$	$I_D = -10mA$, $V_{GS} = 0V$	−30	—	—	V
Gate Threshold Voltage		V_{th}	$V_{DS} = -10V$, $I_D = -1mA$	−0.8	—	−2.0	V
Drain-Source ON Resistance		$R_{DS\,(ON)}$	$V_{GS} = -4V$, $I_D = -1A$	—	0.55	0.76	Ω
			$V_{GS} = -10V$, $I_D = -1A$	—	0.32	0.45	
Forward Transfer Admittance		$\|Y_{fs}\|$	$V_{DS} = -10V$, $I_D = -1A$	0.7	1.4	—	S
Input Capacitance		C_{iss}	$V_{DS} = -10V$, $V_{GS} = 0V$, f = 1MHz	—	160	—	pF
Reverse Transfer Capacitance		C_{rss}		—	30	—	
Output Capacitance		C_{oss}		—	85	—	
Switching Time	Rise Time	t_r	 V_{IN} : t_r, $t_f < 5ns$, Duty ≦ 1%, $t_w = 10\mu s$	—	30	—	ns
	Turn-on Time	t_{on}		—	45	—	
	Fall Time	t_f		—	30	—	
	Turn-off Time	t_{off}		—	120	—	
Total Gate Charge (Gate-Source Plus Gate-Drain)		Q_g	$V_{DD} \fallingdotseq -24V$, $V_{GS} = -10V$, $I_D = -2A$	—	5.5	—	nC
Gate-Source Charge		Q_{gs}		—	4.3	—	
Gate-Drain ("Miller") Charge		Q_{gd}		—	1.2	—	

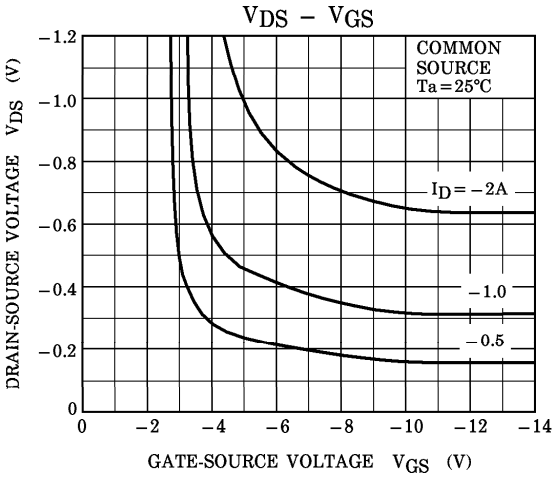
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (Ta = 25°C)

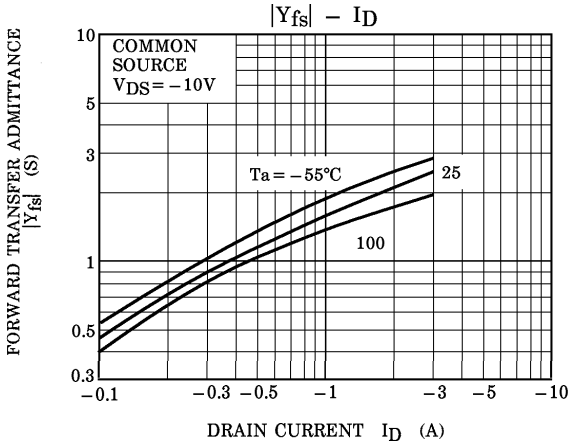
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Continuous Drain Reverse Current	I_{DR}	—	—	—	−2	A
Pulse Drain Reverse Current	I_{DRP}	—	—	—	−6	A
Diode Forward Voltage	V_{DSF}	$I_{DR} = -2A$, $V_{GS} = 0V$	—	—	1.5	V
Reverse Recovery Time	t_{rr}	$I_{DR} = -2A$, $V_{GS} = 0V$	—	40	—	ns
Reverse Recovery Charge	Q_{rr}	$dI_{DR} / dt = 50A / \mu s$	—	18	—	nC

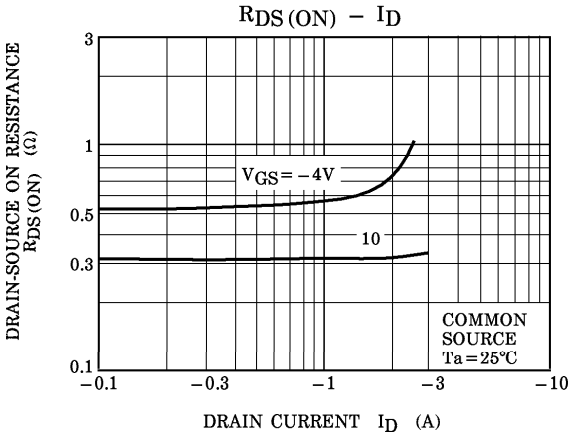

$I_D - V_{DS}$
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)
−10
−8
−6
−4
−3.5
−4.5
−5
−3
V_{GS} = −2.5V
COMMON SOURCE
Ta = 25°C


$I_D - V_{DS}$
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)
COMMON SOURCE
Ta = 25°C
−10
−8
−6
−3.8
−3.5
−4
−5
−3.3
−3
−2.8
V_{GS} = −2.5V

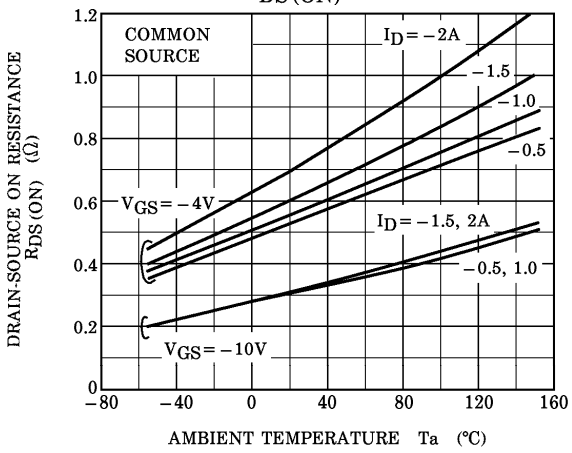

$I_D - V_{GS}$
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)
COMMON SOURCE
V_{DS} = −10V
Ta = −55°C
25
100


$V_{DS} - V_{GS}$
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)
COMMON SOURCE
Ta = 25°C
I_D = −2A
−1.0
−0.5

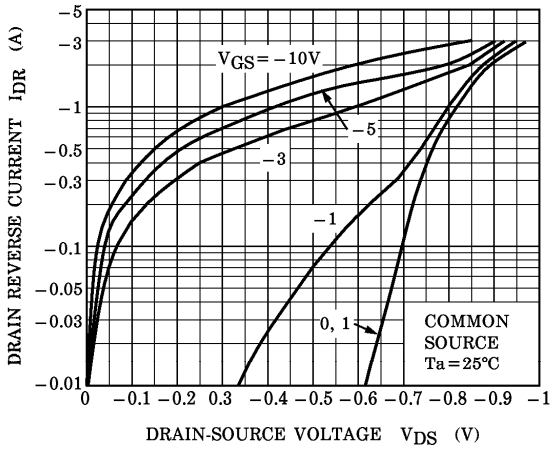

$|Y_{fs}| - I_D$
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)
COMMON SOURCE
V_{DS} = −10V
Ta = −55°C
25
100


$R_{DS\,(ON)} - I_D$
DRAIN-SOURCE ON RESISTANCE $R_{DS\,(ON)}$ (Ω)
DRAIN CURRENT I_D (A)
V_{GS} = −4V
10
COMMON SOURCE
Ta = 25°C

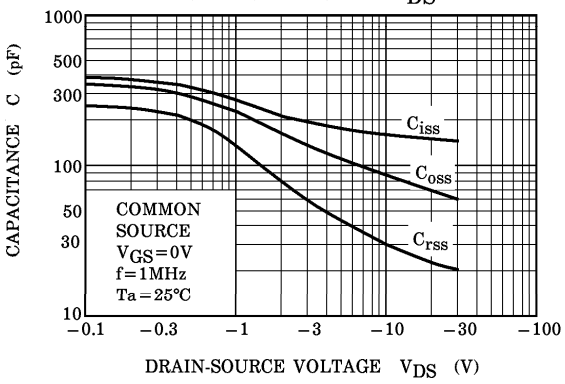
$R_{DS\,(ON)}$ – Ta



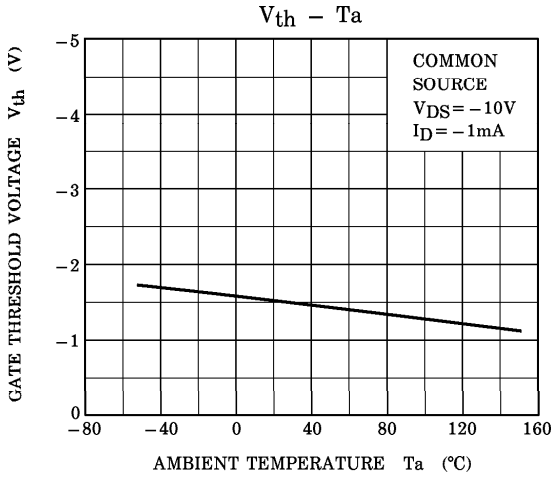
I_{DR} – V_{DS}



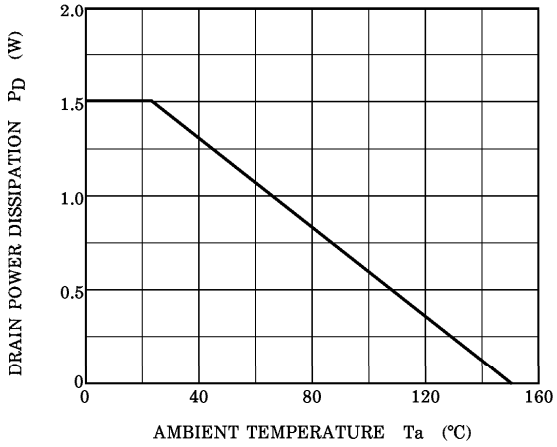
CAPACITANCE – V_{DS}



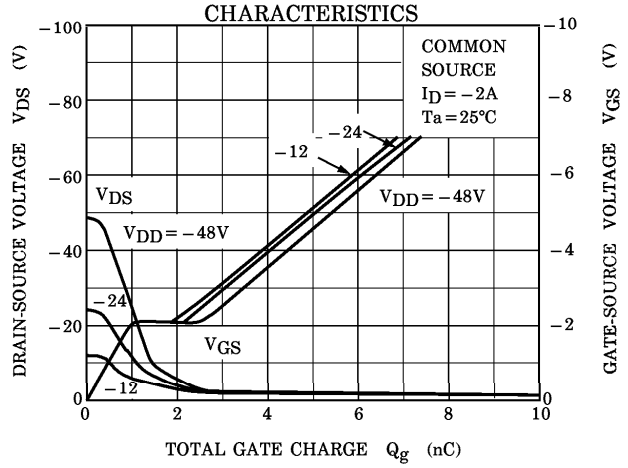
V_{th} – Ta



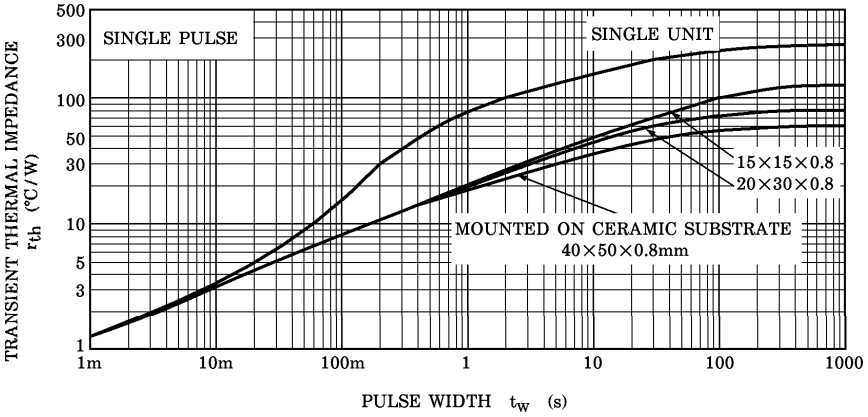
P_D – Ta



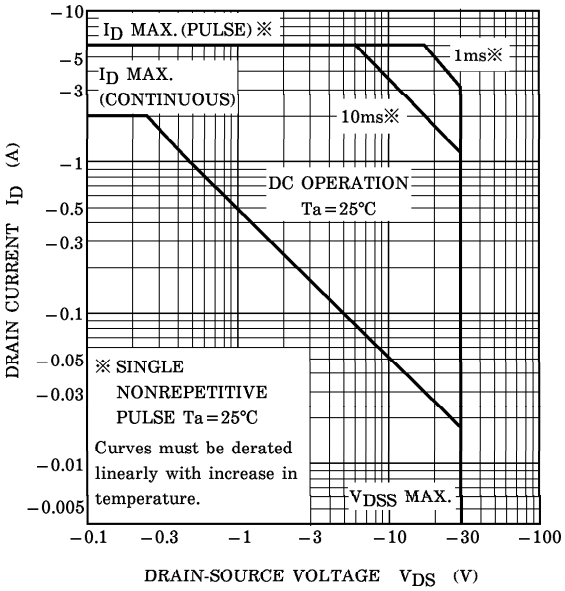
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



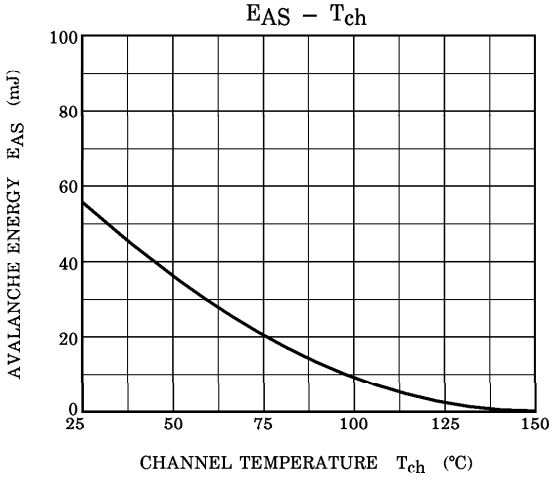
$r_{th} - t_w$

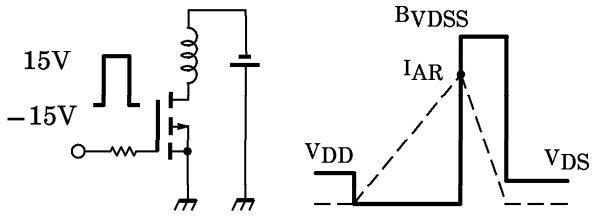


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





TEST CIRCUIT WAVE FORM

Peak $I_{AR} = -2A$, $R_G = 25\Omega$
$V_{DD} = -25V$, $L = 10mH$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$