

# 2SJ517

Silicon P Channel MOS FET  
High Speed Power Switching

# HITACHI

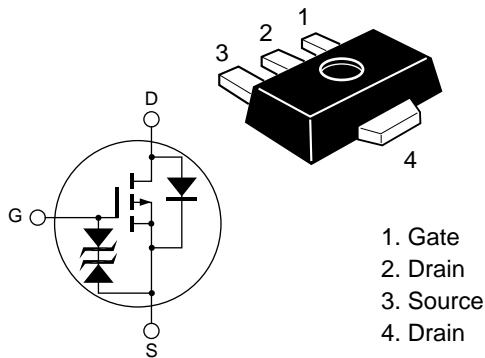
ADE-208-575B (Z)  
3rd. Edition  
Jun 1998

## Features

- Low on-resistance  
 $R_{DS(on)} = 0.18 \Omega$  typ. (at  $V_{GS} = -4V$ ,  $I_D = -1A$ )
- Low drive current
- High speed switching
- 2.5V gate drive devices.

## Outline

UPAK



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-20	V
Gate to source voltage	$V_{GSS}$	±10	V
Drain current	$I_D$	-2	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	-4	A
Body-drain diode reverse drain current	$I_{DR}$	-2	A
Channel dissipation	Pch <sup>Note2</sup>	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

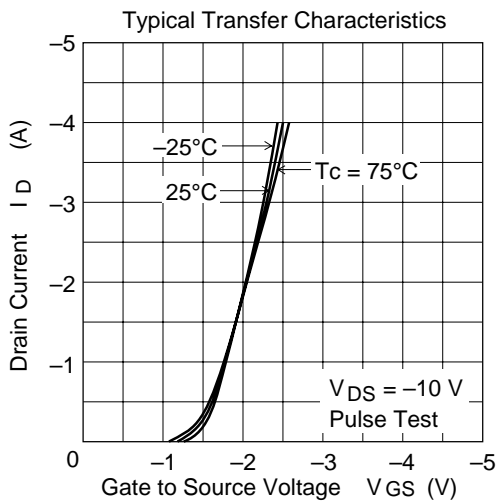
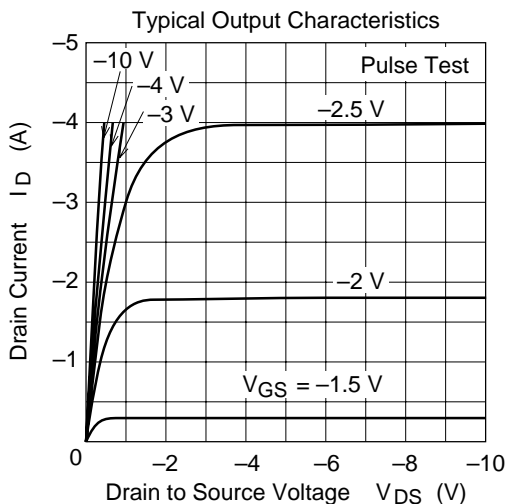
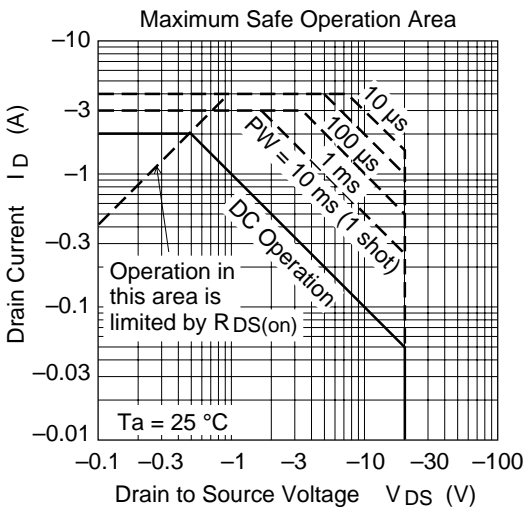
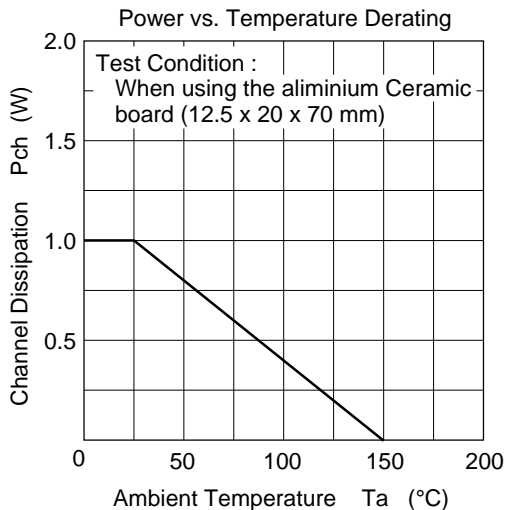
Note: 1.  $PW \leq 100\mu s$ , duty cycle  $\leq 10\%$   
 2. When using aluminium ceramic board (12.5 x 20 x 0.7 mm)

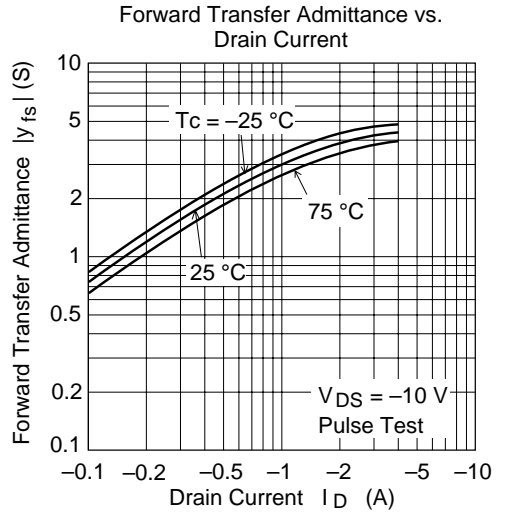
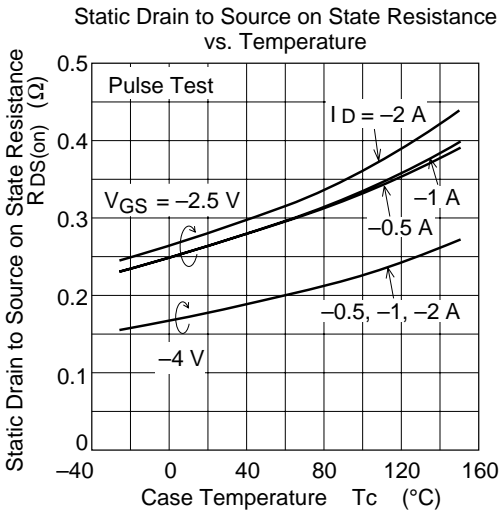
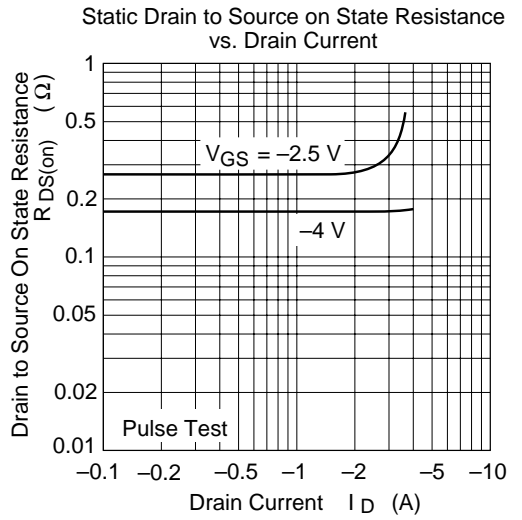
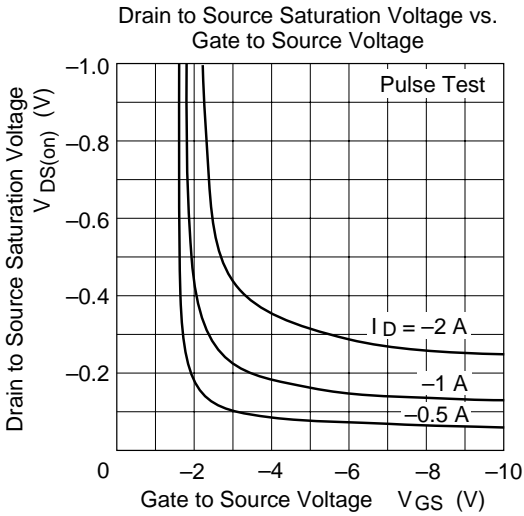
## Electrical Characteristics (Ta = 25°C)

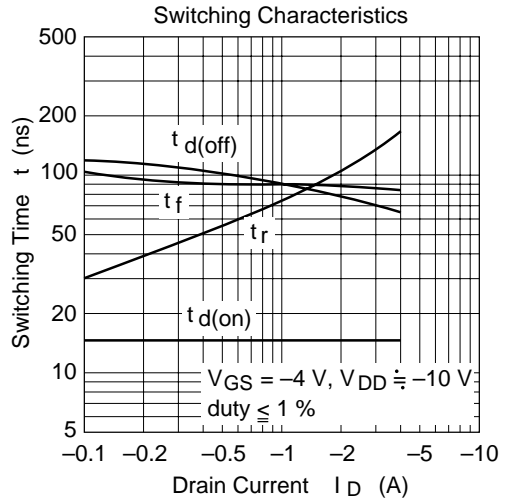
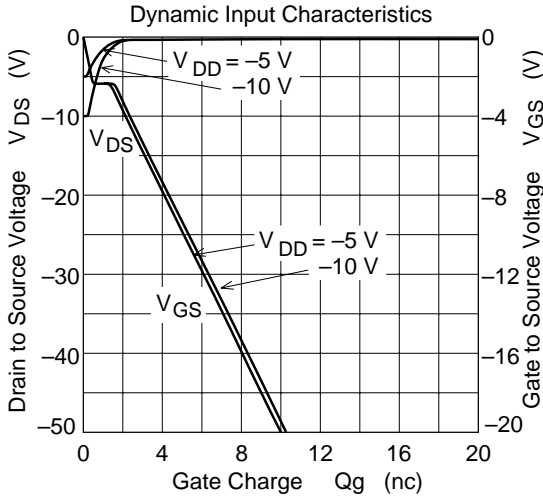
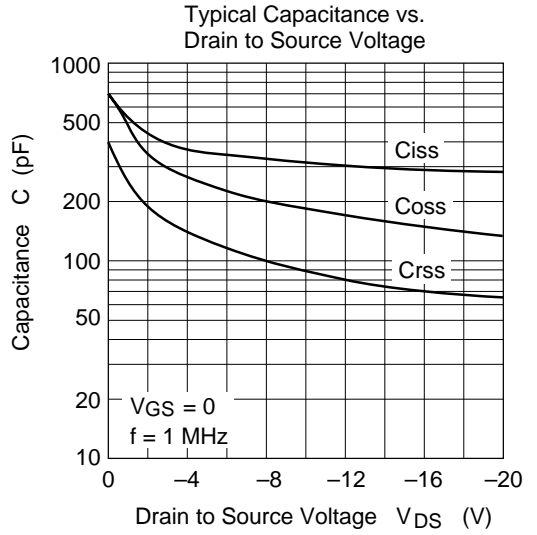
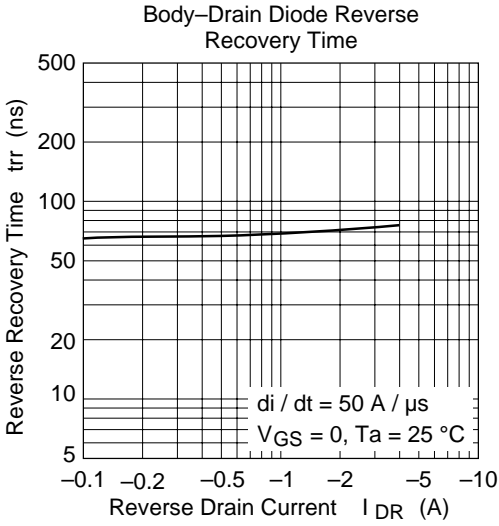
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-20	—	—	V	$I_D = -10mA, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	$I_G = \pm 100\mu A, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-10	μA	$V_{DS} = -20V, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = \pm 8V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.5	—	-1.5	V	$I_D = -1mA, V_{DS} = -10V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.18	0.24	Ω	$I_D = -1A, V_{GS} = -4V$ <sup>Note3</sup>
Static drain to source on state resistance	$R_{DS(on)}$	—	0.27	0.43	Ω	$I_D = -1A, V_{GS} = -2.5V$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	1.8	3.0	—	S	$I_D = -1A, V_{DS} = -10V$ <sup>Note3</sup>
Input capacitance	Ciss	—	320	—	pF	$V_{DS} = -10V$
Output capacitance	Coss	—	190	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	90	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	14	—	ns	$I_D = -1A, R_L = 10\Omega$
Rise time	$t_r$	—	75	—	ns	$V_{GS} = -4V$
Turn-off delay time	$t_{d(off)}$	—	90	—	ns	
Fall time	$t_f$	—	90	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	-0.95	—	V	$I_F = -2A, V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	70	—	ns	$I_F = -2A, V_{GS} = 0$ diF/dt = 50A/μs

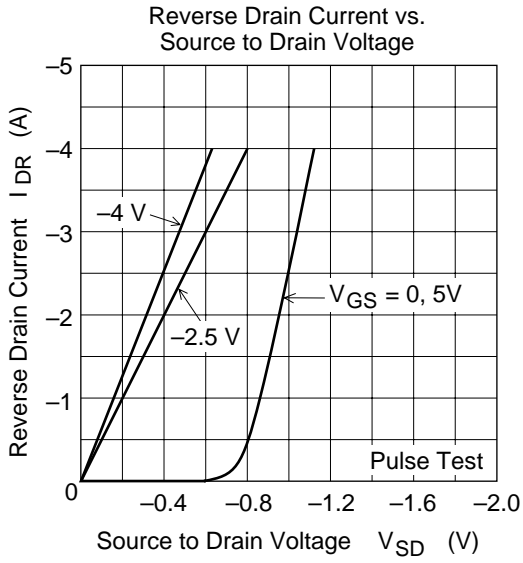
Note: 3. Pulse test  
 4. Marking is "YY".

## Main Characteristics

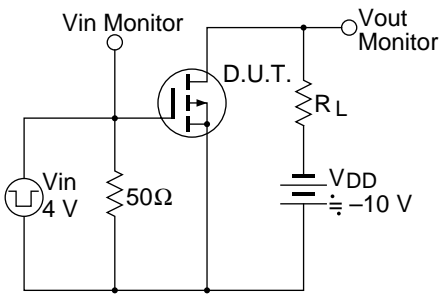




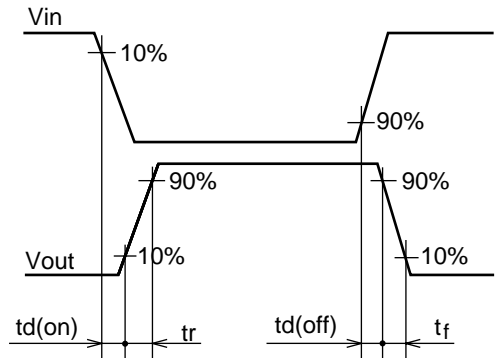




Switching Time Test Circuit

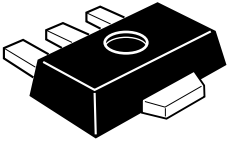
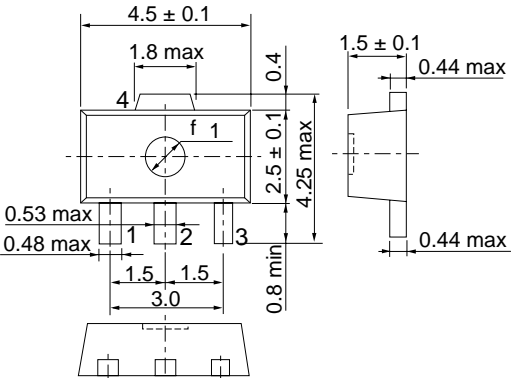


Waveform



Package Dimensions

Unit: mm



Hitachi Code	UPAK
EIAJ	SC-62
JEDEC	UPAK

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