

## 2SK3674-01L,S,SJ (900V/2.0Ω/7A)

1) Package T-PACK L ··· See Page 2/4  
S ··· See Page 3/4  
SJ ··· See Page 4/4

## 2) Absolute Maximum Ratings (Tc=25 unless otherwise specified)

| Items   | Symbols               | Ratings           | Units    |
|---|-----------------------|-------------------|----------|
| Drain-Source Voltage                                    | $V_{DS}$              | 900               | V        |
| Continuous Drain Current                                | $I_D$                 | ±7                | A        |
| Pulsed Drain Current                                    | $I_{D(pulse)}$        | ±28               | A        |
| Gate-Source Voltage                                     | $V_{GS}$              | ±30               | V        |
| Repetitive and Non-Repetitive Maximum Avalanche Current | $I_{AR}$              | 7                 | A        |
| Non-Repetitive Maximum Avalanche Energy                 | $E_{AS}$              | 269.5             | mJ *1    |
| Maximum Drain-Source dV/dt                              | dV/dt                 | 20                | kV/us    |
| Peak Diode recovery dV/dt                               | dV/dt                 | 5                 | kV/us *2 |
| Maximum Power Dissipation                               | $P_D @ T_c=25$        | 225               | W        |
|   | $P_D @ T_a=25$        | 1.67              | W        |
| Operating and Storage Temperature range                 | $T_{ch}$<br>$T_{stg}$ | 150<br>-55 ~ +150 |          |

## 3) Electrical Characteristics (Tch=25 unless otherwise specified)

| Items                            | Symbols      | Test Conditions                | min. | typ. | max. | Units    |
|----------------------------------|--------------|--------------------------------|------|------|------|----------|
| Drain-Source Breakdown Voltage   | $BV_{DSS}$   | $I_D=250\mu A$ $V_{GS}=0V$     | 900  | ---  | ---  | V        |
| Gate Threshold Voltage           | $V_{GS(th)}$ | $I_D=250\mu A$ $V_{DS}=V_{GS}$ | 3.0  | ---  | 5.0  | V        |
| Zero Gate Voltage Drain Current  | $I_{DSS}$    | $V_{DS}=900V$ $T_{ch}=25$      | ---  | ---  | 50   | $\mu A$  |
|                                  |              | $V_{GS}=0V$ $T_{ch}=125$       | ---  | ---  | 500  | $\mu A$  |
| Gate-Source Leakage Current      | $I_{GSS}$    | $V_{GS}=\pm 30V$ $V_{DS}=0V$   | ---  | ---  | 100  | nA       |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $I_D=3.5A$ $V_{GS}=10V$        | ---  | ---  | 2.0  | $\Omega$ |
| Input Capacitance                | $C_{iss}$    | $V_{DS}=25V$                   | ---  | 980  | ---  | pF       |
| Output Capacitance               | $C_{oss}$    | $V_{GS}=0V$                    | ---  | 120  | ---  |          |
| Reverse Transfer Capacitance     | $C_{rss}$    | f=1MHz                         | ---  | 6    | ---  | nC       |
| Total Gate Charge                | Qg           | $V_{CC}=450V$                  | ---  | 28   | ---  |          |
| Gate to Source Charge            | Qgs          | $I_D=7A$                       | ---  | 9    | ---  |          |
| Gate to Drain (Miller) Charge    | Qgd          | $V_{GS}=10V$                   | ---  | 8    | ---  |          |
| Avalanche Capability             | $I_{AV}$     | L=10.1mH Tch=25                | 7    | ---  | ---  | A        |
| Diode Forward On-Voltage         | $V_{SD}$     | $I_F=7A, V_{GS}=0V, Tch=25$    | ---  | 1.0  | 1.5  | V        |

## 4) Thermal Characteristics

| Items              | Symbols        | Test Conditions | min. | typ. | max. | Units |
|--------------------|----------------|-----------------|------|------|------|-------|
| Channel to Case    | $R_{th(ch-c)}$ |                 |      |      | 0.56 | /W    |
| Channel to Ambient | $R_{th(ch-a)}$ |                 |      |      | 75.0 | /W    |

\*1 L=10.1mH, Vcc=90V

\*2  $I_F \leq -I_D, -di/dt=50A/\mu s, V_{CC} \leq BV_{DSS}, Tch \leq 150^\circ C$ 

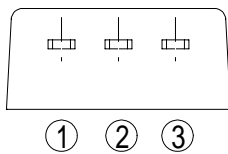
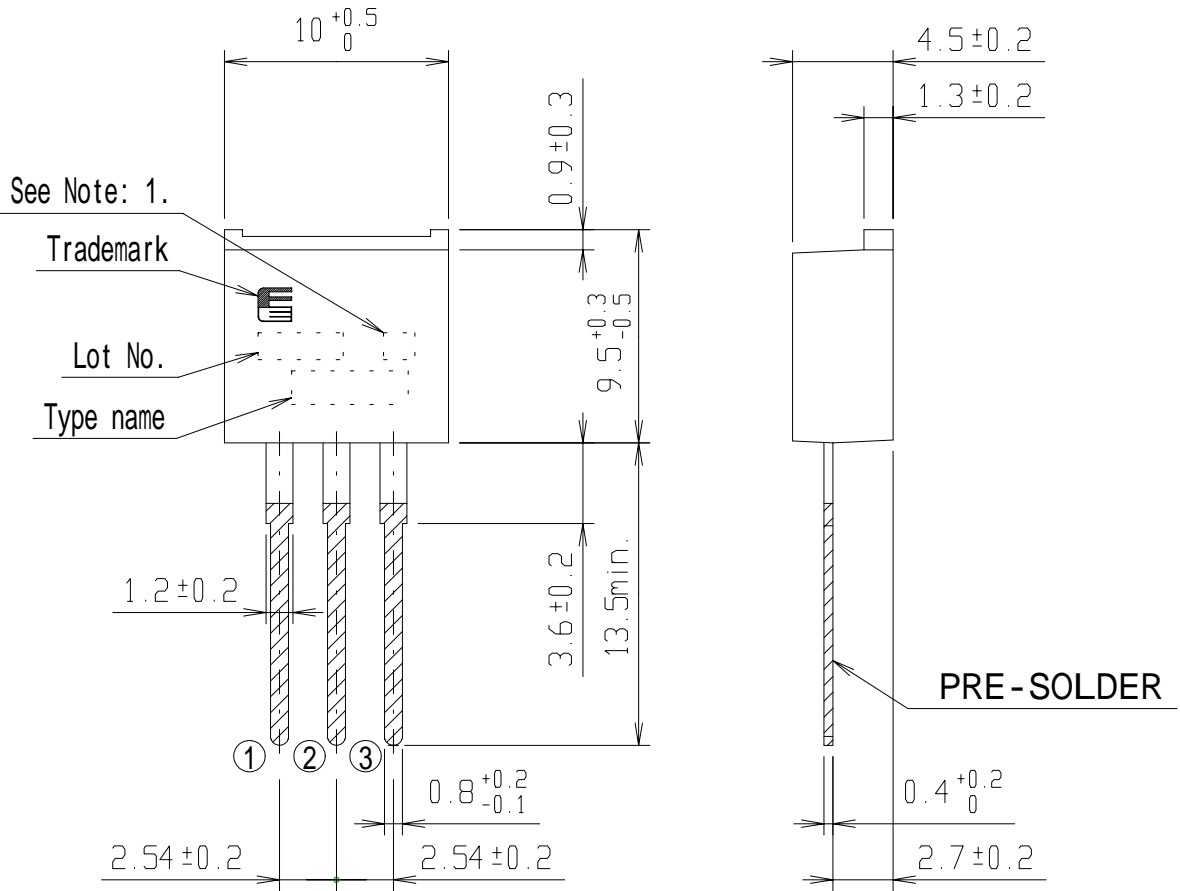
| DATE                 | NAME        | APPROVED | Fuji Electric Co.,Ltd. |               |
|----------------------|-------------|----------|------------------------|---------------|
| DRAWN Sep. -10-'02   | T. Kuboyama |          |                        |               |
| CHECKED Sep. -10-'02 | T. Yamada   | T. HOSEN | DWG. NO.               | MT5F12615 1/4 |

This material and the information herein is the property of Fuji Electric Co., Ltd. They shall be neither reproduced, copied, lent, or disclosed in any way whatsoever for the use of any third party nor used for the manufacturing purposes without the express written consent of Fuji Electric Co., Ltd.

REVISIONS

MA4LE

# FUJI POWER MOS FET



## CONNECTION

- ① GATE
- ② DRAIN
- ③ SOURCE

JEDEC : TO-220AB

Note: 1. Guaranteed mark of avalanche ruggedness.

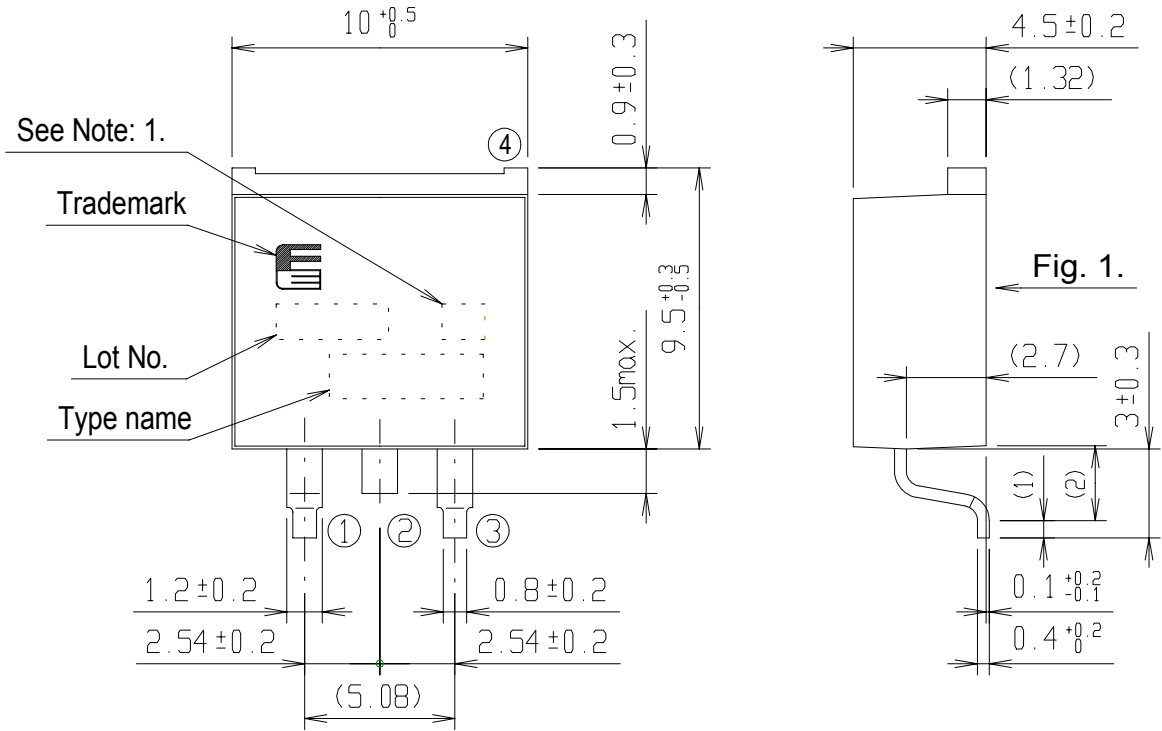
DIMENSIONS ARE IN MILLIMETERS.

This material and the information herein is the property of Fuji Electric Co.,Ltd. They shall be neither reproduced, copied, lent, or disclosed in any way whatsoever for the use of any third party nor used for the manufacturing purposes without the express written consent of Fuji Electric Co.,Ltd.

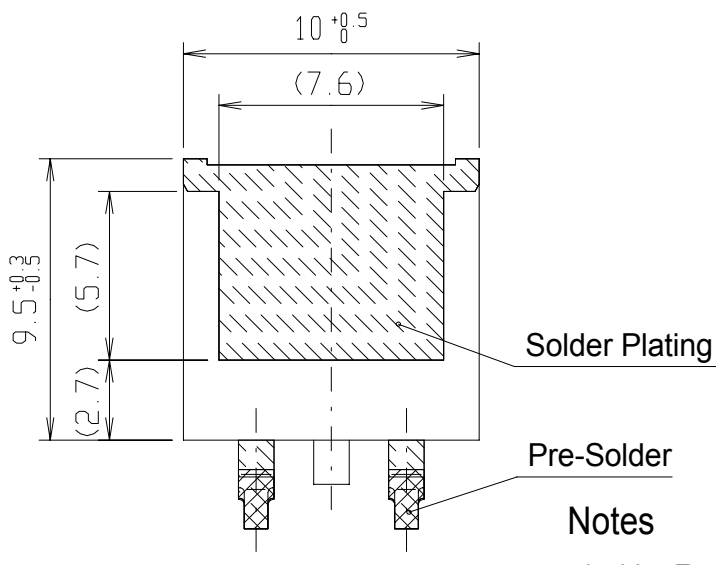
|           |      |      |          |                               |
|-----------|------|------|----------|-------------------------------|
|           | DATE | NAME | APPROVED | <b>Fuji Electric Co.,Ltd.</b> |
| DRAWN     |      |      |          | DWG. NO. MT5F12615 2/4        |
| CHECKED   |      |      |          |                               |
| REVISIONS |      |      |          |                               |

# FUJI POWER MOS FET

## OUT VIEW



**Fig. 1.**



## CONNECTION

- ① GATE
- ④ ② DRAIN
- ③ SOURCE

### Notes

Note: 1. Guaranteed mark of avalanche ruggedness.

1. ( ) : Reference dimensions.
2. The metal part is covered with the solder plating, part of cutting is without the solder plating.

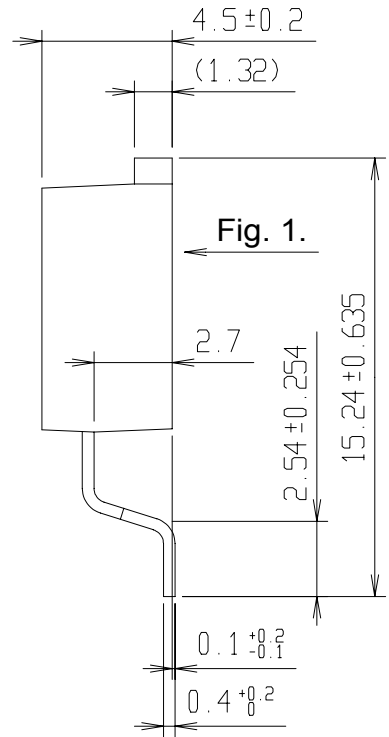
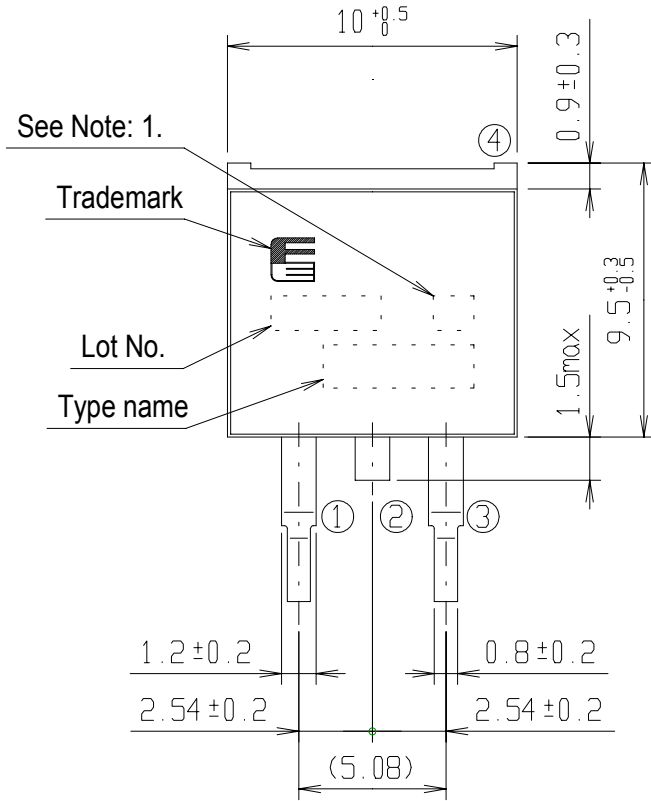
DIMENSIONS ARE IN MILLIMETERS.

This material and the information herein is the property of Fuji Electric Co.,Ltd. They shall be neither reproduced, copied, lent, or disclosed in any way whatsoever for the use of any third party nor used for the manufacturing purposes without the express written consent of Fuji Electric Co.,Ltd.

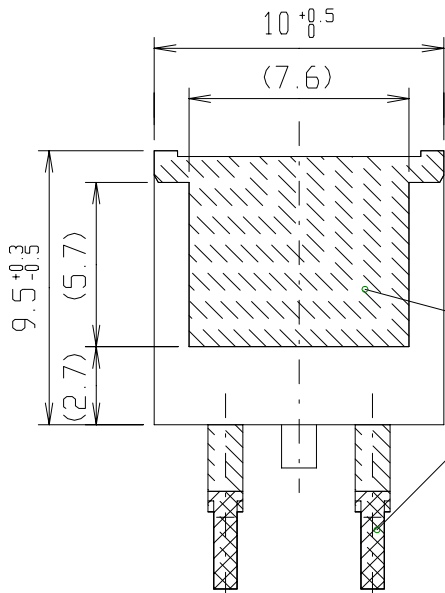
|           |      |      |          |                               |
|-----------|------|------|----------|-------------------------------|
|           | DATE | NAME | APPROVED | <b>Fuji Electric Co.,Ltd.</b> |
| DRAWN     |      |      |          | DWG. NO. MT5F12615 3/4        |
| CHECKED   |      |      |          |                               |
| REVISIONS |      |      |          |                               |

# FUJI POWER MOS FET

## OUT VIEW



**Fig. 1.**



### CONNECTION

- ① GATE
- ④ ② DRAIN
- ③ SOURCE

### Notes

1. ( ) : Reference dimensions.
2. The metal part is covered with the solder plating, part of cutting is without the solder plating.

Note: 1. Guaranteed mark of avalanche ruggedness.

DIMENSIONS ARE IN MILLIMETERS.

This material and the information herein is the property of Fuji Electric Co.,Ltd. They shall be neither reproduced, copied, lent, or disclosed in any way whatsoever for the use of any third party nor used for the manufacturing purposes without the express written consent of Fuji Electric Co.,Ltd.

| DATE | NAME | APPROVED |
|------|------|----------|
|      |      |          |
|      |      |          |

|                               |               |
|-------------------------------|---------------|
| <b>Fuji Electric Co.,Ltd.</b> |               |
| DWG. NO.                      | MT5F12615 4/4 |

REVISIONS

MA4LE