

Intel® 82575 Gigabit Ethernet Controller

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Revision History

Date	Revision	Description
August 2005	0.10	Initial Release
January 2006	0.25	Added general information, updated pins list
July 2006	0.50	Removed information regarding Fast Management Link; added general information
February 2007	0.75	Added measured power values; corrected Visual Pin Assignment Diagrams (RBIAS0_N and RBIAS1_N corrected to VSS).
June 2007	1.0	Updated classification, changed RMII to NC-SI, updated pin list, updated NC-SI timing specs. changed LAN_PWR_GOOD to Internal_Power_On_Reset.



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1.0 Introduction

The Intel® 82575 Gigabit Ethernet Controller is a single, compact component with two fully integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) ports. The device uses the PCI Express Base Specification, Rev.1.1RD.

The Intel 82575 provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3z, 802.3u, and 802.3ab). Ports also contain a Serializer-Deserializer (SERDES) to support 1000Base-SX/LX (optical fiber) and Gigabit backplane applications. In addition to managing MAC and PHY Ethernet layer functions, the controller manages PCI Express packet traffic across its transaction, link, and physical/logical layers. The SERDES can be used in SGMII mode to connect to external PHY, either on-board or via the SFP connector.

The Intel 82575's on-board System Management Bus (SMB) ports enable network manageability implementations required by information technology personnel for remote control and alerting via the LAN. With SMB, management packets can be routed to or from a management processor. Enhanced pass-through capabilities also allow system remote control over standardized interfaces. Also included is a new manageability interface, NC-SI that supports the DMTF preOS sideband protocol. An internal management interface called MDIO enables the MAC (and software) to monitor and control the PHY. Both ports support the Wake on LAN feature.

The 82575 Gigabit Ethernet Controller with PCI Express architecture is designed for high performance and low memory latency. The device is optimized to connect to a system Memory Control Hub (MCH) using four PCI Express lanes. Alternatively, the 82575 controller can connect to an I/O Control Hub that has a PCI Express interface.

Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. Combining a parallel and pipe-lined logic architecture optimized for Gigabit Ethernet and independent transmit and receive queues, the 82575 controller efficiently handles packets with minimum latency. The 82575 controller includes advanced interrupt handling features, including MSI-X support. The 82575 uses efficient ring buffer descriptor data structures, with up to 64 packet descriptors cached on chip. A large 48 KByte per port on-chip packet buffer maintains superior performance. In addition, using hardware acceleration, the controller offloads tasks from the host, such as TCP/UDP/IP checksum calculations and TCP segmentation.

The 82575 operation can be configured using EEPROM and FLASH; it can be also be used in EEPROM-less configurations.

The 82575 is packaged in a 25mm X 25mm, 576-pin flip chip ball grid array (FCBGA).

1.1 Document Scope

This document contains targeted datasheet specifications for the 82575 Gigabit Ethernet Controller, including signal descriptions, DC and AC parameters, packaging data, and pinout information.

1.2 Reference Documents

This application assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

82575 Gigabit Ethernet Controller Design Guide. Intel Corporation.

Intel Ethernet Controllers Timing Device Selection Guide. Intel Corporation.

PCI Express Base Specification, Revision 1.1.



PCI Express Card Electromechanical Specification, Revision 1.0a. PCI Special Interest Group.

PCI Bus Power Management Interface Specification, Revision 1.1. PCI Special Interest Group.

IEEE Standard 802.3, 2002 Edition. Institute of Electrical and Electronics Engineers (IEEE). This version incorporates various IEEE standards previously published separately.

System Management Bus (SMBus) Specification, SBS Implementers Forum, Ver. 2.0, August 2000.

INF-8074i Specification for SFP (Small Form factor Pluggable) Transceiver.



1.3 Block Diagram

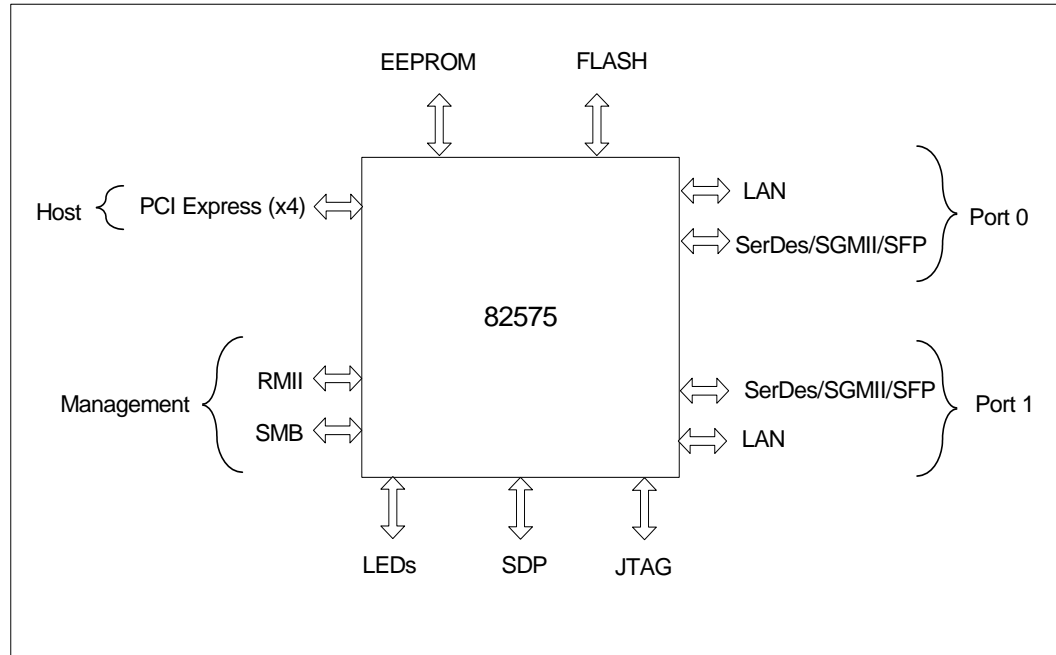


Figure 1. 82575 Gigabit Ethernet Controller Block Diagram



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2.0 Features of the 82575 Gigabit Ethernet Controller

2.1 PCI Express Features

Features	Benefits
Uses x4 PCI Express interface on MCH device	<ul style="list-style-type: none"> • Bus sharing not required • Low latency path to memory • Relieves congestion for IO devices connected to ICH
Peak bandwidth 2 GB/s in each direction per PCI Express lane	<ul style="list-style-type: none"> • Supports Gigabit Ethernet at full wire speed
PCI Express Power Management	<ul style="list-style-type: none"> • Compatible extensions to PCI power management and ACPI • PE_WAKE_N available for wakeup event
High bandwidth density per pin	<ul style="list-style-type: none"> • Less congested board routing
64-bit address support for systems using more than 4 GB of physical memory	<ul style="list-style-type: none"> •

2.2 MAC-Specific Features

Features	Benefits
I/O Acceleration Technology ² (IOAT ²)	<ul style="list-style-type: none"> • Accelerated TCP I/O.
Four optimized transmit and receive queues	<ul style="list-style-type: none"> • Network packets handled without waiting or buffer overflow.
IEEE 802.3x compliant flow control support with software controllable pause times and threshold values	<ul style="list-style-type: none"> • Control over the transmissions of pause frames through software or hardware triggering • Frame loss reduced from receive overruns
Caches up to 64 packet descriptors (per queue)	<ul style="list-style-type: none"> • Efficient use of PCI Express bandwidth
Separate transmit and receive queues per port	<ul style="list-style-type: none"> • Efficient packet prioritization
Programmable host memory receive buffers (256 Bytes to 16 KBytes) and cache line size (64 Bytes to 128 Bytes)	<ul style="list-style-type: none"> • Efficient use of PCI Express bandwidth
Wide, pipelined internal data path architecture	<ul style="list-style-type: none"> • Low latency data handling • Superior DMA transfer rate performance
Dual 8 KByte configurable Transmit and Receive FIFO buffers	<ul style="list-style-type: none"> • No external FIFO memory requirements • FIFO size adjustable to application
Descriptor ring management hardware for transmit and receive	<ul style="list-style-type: none"> • Simple software programming model
Optimized descriptor fetching and write-back mechanisms	<ul style="list-style-type: none"> • Efficient system memory and use of PCI Express bandwidth



Features	Benefits
Mechanism available for reducing interrupts generated by transmit and receive operations	<ul style="list-style-type: none"> Maximizes system performance and throughput
Support for transmission and reception of packets up to 9.5 kB	<ul style="list-style-type: none"> Enables jumbo frames
MSI-X Support	<ul style="list-style-type: none"> Part of the PCI standard, enables sending interrupt messages to specific CPUs in a multiple-cores platform

2.3 PHY-Specific Features

Features	Benefits
IEEE 802.3x compliant flow control support with software controllable pause times and threshold values	Control over the transmissions of pause frames through software or hardware triggering Frame loss reduced from receive overruns
Line Length > 140m	Reliable operation at greater distances
Operates with worst-case cable	Reliability
Supports carrier extension and packet bursting (half duplex)	Improves performance
Auto-negotiation with support for Next Page	Improves performance and reliability
PMA loopback capable (No echo cancel)	Facillitates testing/troubleshooting
Advanced Power Management - <ul style="list-style-type: none"> Low power link up "Smart Power Down - Link disconnect 	Improves power capabilities
Support for limited auto MDIO register init - limited number of registers	Improves performance
Fiber/Copper switch support	Ease of design
SERDES Signal Detect and support of non-AN partner	
Smart Speed	
Auto crossover for MDI	
Smart Power Down	
Advanced Cable Diagnostics	

2.4 Host Offloading Features

Features	Benefits
Transmit and receive IP, TCP and UDP checksum off-loading capabilities	<ul style="list-style-type: none"> Lower CPU utilization
Transmit TCP segmentation	<ul style="list-style-type: none"> Increased throughput and lower CPU utilization Large send offload feature (in Microsoft* Windows* XP) compatible
IPv6 Offloading	<ul style="list-style-type: none"> Checksum and segmentation capability extended to new standard packet type



Features	Benefits
Header split replication in receive	<ul style="list-style-type: none"> Helps the driver to focus on the relevant part of the packet without the need to parse it.
Advanced packet filtering	<ul style="list-style-type: none"> 16 exact matched packets (unicast or multicast) 4096-bit hash filter for multicast frames Promiscuous (unicast and multicast) transfer mode support Optional filtering of invalid frames
IEEE 802.1q VLAN support with VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags	<ul style="list-style-type: none"> Ability to create multiple virtual LAN segments
Double Vlan	<ul style="list-style-type: none"> Insert in Tx and extract in Rx
Descriptor ring management hardware for transmit and receive	<ul style="list-style-type: none"> Optimized fetching and write-back mechanisms for efficient system memory and PCI bandwidth usage
9.5 kByte jumbo frame support	<ul style="list-style-type: none"> High throughput for large data transfers on networks supporting jumbo frames
Receive Side Scaling (RSS)	<ul style="list-style-type: none"> Multiple Rx queues
VMDq	<ul style="list-style-type: none"> Virtualization environment. In this environment, packets dedicated to different virtual machines can be routed to different queues, thus easing the routing of these packets to the target machine.
Direct Cache Access (DCA)	<ul style="list-style-type: none"> The IO device activates a pre-fetch engine in the CPU that loads the data into the CPU cache ahead of time, before use, eliminating cache misses and reducing CPU load.
Fragmented UDP checksum offload for packet reassembly	<ul style="list-style-type: none">

2.5 Manageability Features

Features	Benefits
Advance Pass Through-compatible management packet Tx/Rx support	
ASF 1.0 and Alert on LAN 2.0	
Both ports support Wake on LAN (WoL)	
SMBus port	Network management flexibility
NC-SI high-bandwidth interface	Manageability DMTF preOS sideband protocol support
On-board microcontroller	Promotes customized designs Allows packets routing to and from either LAN port and a server management processor
Preboot eXecution Environment (PXE) Flash interface support (32-bit and 64-bit)	Local Flash interface for PXE image
iSCSI Boot	Network Management Feature



Features	Benefits
Compliance with PCI Power Management 1.1 and ACPI 2.0 register set compliant including: <ul style="list-style-type: none"> • D0 and D3 power states • Network Device Class Power Management Specification 1.1 	PCI power management capability requirements for PC and embedded applications
SNMP and RMON statistic counters	Easy system monitoring with industry standard consoles
SDG 3.0, WfM 3.0, and PC2001 compliance	Remote network management capabilities through DMI 2.0 and SNMP software
Watchdog Timer	Used to give an indication to the manageability firmware or external devices that the 82575 or the driver is not functioning.
SGMII interface for embedded applications with an I2C or MDC/MDIO control interface.	Ease of embedded designs

2.6 Additional Device Features

Features	Benefits
Two complete Gigabit Ethernet connections in a single device	<ul style="list-style-type: none"> • Inherent dual port teaming ability • High availability using one port for failover • Higher throughput than single Gigabit Ethernet port • Lower latency due to one electrical load on the bus • Saves critical board space • Reduced multi-port Gigabit Ethernet costs
Integrated SERDES	<ul style="list-style-type: none"> • Supports backplane and fiber applications as well as copper-based Gigabit via the SGMII interface
Four activity and link indication outputs (per port) that directly drive LEDs	<ul style="list-style-type: none"> • Link and activity indications (10, 100, and 1000 Mbps) on each port
Programmable LED functionality	<ul style="list-style-type: none"> • Software definable function (speed, link, and activity) and blinking allowing flexible LED implementations
Internal PLL for clock generation can use a 25 MHz crystal	<ul style="list-style-type: none"> • Lower component count and system cost
JTAG (IEEE 1149.1) Test Access Port built in silicon	<ul style="list-style-type: none"> • Simplified testing using boundary scan • Supports the IDCODE instruction
Four software definable pins per port	<ul style="list-style-type: none"> • Additional flexibility for LEDs or other low speed I/O devices
Provides loopback capabilities	<ul style="list-style-type: none"> • Validates silicon integrity
Four-wire SPI EEPROM interface	<ul style="list-style-type: none"> • Standard



2.7 Technology Features

Features	Benefits
576-pin Flip-Chip Ball Grid Array (FC-BGA) package	<ul style="list-style-type: none"> • 25 mm X 25 mm
Operating temperature: 1000BASE-T, 0 °C to 55 °C* 1000BASE-SX/LX (or SERDES backplane), 0 °C to 70 °C Storage temperature 65 °C to 140 °C	<ul style="list-style-type: none"> • Simple thermal design
Typical targeted power dissipation: 2.43 W @ D0 1000 Mbps 0.79 W @ D3cold 100 Mbps (wakeup enabled) 0.29 W @ D3cold (wakeup disabled)	<ul style="list-style-type: none"> • Conditions: FF materials, nominal voltage, 115 °C • Minimizes impact of incorporating Gigabit instead of Fast Ethernet.
Maximum Payload Size: 128 and 256	<ul style="list-style-type: none"> •
Max number of transactions (TLP) supported on PCIe: Four TX DMA requests + 1 TX descriptor + 1 RX descriptor	<ul style="list-style-type: none"> •

* For information about operating the 82575 outside of this range, please refer to the 82575 Thermal Management Application Note.



3.0 Signal Descriptions and Pinout List

The targeted signal names are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

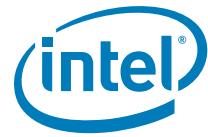
3.1 Signal Type Definitions

The signals of the 82575 controller are electrically defined as follows:

Name	Definition	DC specification
I	Input Standard input only digital signal.	See Table 9
O	Output Standard output only digital signal.	See Table 9
TS	Tri-state Bi-directional three-state digital input/output signal.	See Table 9
OD	Open Drain Wired-OR with other agents. The signaling agent asserts the OD signal, but the signal is returned to the inactive state by a weak pull-up resistor. The pull-up resistor may require two or three clock periods to fully restore the signal to the de-asserted state.	See Table 10
A	Analog PCI Express*, SERDES, or PHY analog signal.	See Table 10
P	Power Power connection, voltage reference, or other reference connection.	See Table 10

3.2 PCI Express Interface

Symbol	Type	Name and Function
PER_0_N PER_0_P PER_1_N PER_1_P PER_2_N PER_2_P PER_3_N PER_3_P	A(I)	High Speed Serial Receive Data These signals connect to corresponding PETn and PETp signals on a system motherboard or a PCI Express connector. Series AC coupling capacitors are required at the transmitter end. The PCI Express differential inputs are clocked at 2.5 Gb/s.



Symbol	Type	Name and Function
PET_0_N PET_0_P PET_1_N PET_1_P PET_2_N PET_2_P PET_3_N PET_3_P	A(0)	High Speed Serial Transmit Data These signals connect to corresponding PERn and PERp signals on a system motherboard or a PCI Express connector. Series AC coupling capacitors are required at the 82575 controller end. The PCI Express differential outputs are clocked at 2.5 Gb/s.
PE_RCOMP	A	High Speed Serial Impedance Compensation Connect the recommended resistor value 1.4K Ω from this ball to ground.
PE_CLK_P PE_CLK_N	A	100 MHz Differential Clock for the PCI Express Interface The reference clock is furnished by the system and has a 300 ppm frequency tolerance.
PE_RST_N	I	PCI Express Reset When the signal is low, all PCI Express functions are held in reset. When the signal is high, it denotes that main power is available to the 82575 controller and the reference clock is running. In systems with a PCI Express add-in card, this signal routes to the connector.
PE_WAKE_N	OD	Wake The device drives this signal low when it receives a wake-up event and either the PME Enable bit in the Power Management Control/Status Register or the Advanced Power Management Enable (APME) bit of the Wake-up Control Register (WUC) is 1b.

3.3 Power Management Signals

Symbol	Type	Name and Function
AUX_PWR	I	Auxiliary Power Present. If the Auxiliary Power signal is high, then auxiliary power is present and the 82575 device should support the D3 _{cold} power state.
LAN0_DIS_N LAN1_DIS_N	I	LAN Disables 0 and 1 Disables individual Ethernet ports. State is latched upon a rising edge of PERST_N or a PCI Express reset event. This pin has an internal pull-up resistor.
DEV_OFF_N	I	Device Off Asynchronously disables Ethernet controller.
MAIN_PWR_OK	I	Main Power OK Indicates that platform main power is up. Must be connected externally.



3.4 System Management Interface Signals

Symbol	Type	Name and Function
SMBCLK	OD	SMB Clock The SMB Clock signal is an open drain signals for the serial SMB interface.
SMBD	OD	SMB Data The SMB Data signal is an open drain signal for the serial SMB interface.
SMBALRT_N	OD	SMB Alert The SMB Alert signal is an open drain signal for serial SMB Port A. In ASF mode, this signal acts as a power good input. It acts as an alert input in 82559 compatible mode.
NCSI_CLK_IN	I	NCSI Reference Clock Input. Synchronous clock reference for receive, transmit and control interface. It is a 50MHz clock +/- 50 ppm.
NCSI_CLK_OUT	O	NCSI Reference Clock Output. Synchronous clock reference for receive, transmit and control interface. It is a 50MHz clock +/- 50 ppm. Serves as a clock source to the BMC and Zoar (when configured so).
NCSI_CRSDV	O	Carrier Sense / Receive Data Valid
NCSI_RXD[1] NCSI_RXD[0]	O	Receive Data. Data signals from the device to the BMC
NCSI_TX_EN	I	Transmit Enable
NCSI_TXD[1] NCSI_TXD[0]	I	Transmit Data. Data signals from BMC to the device

3.5 MDIO Signals

Symbol	Type	Name and Function
MDC	I	Management Data Clock. Used by the PHY as a clock timing reference for information transfer on the MDIO signal. The MDC is not required to be a continuous signal and can be frozen when no management data is transferred. The MDC signal has a maximum operating frequency of 2.5MHz.
MDIO	I/O	Management Data I/O. This internal signaling between the MAC and PHY logically represents a bi-directional data signal used to transfer control information and status to and from the PHY (to read and write the PHY management registers). Asserting and interpreting value(s) on this interface requires knowledge of the special MDIO protocol to avoid possible internal signal contention or miscommunication to/from the PHY



3.6 SPI EEPROM and FLASH Signals

Symbol	Type	Name and Function
EE_DI	TS	EEPROM Data Input The EEPROM Data Input pin is used for output to the SPI EEPROM memory device.
EE_DO	I	EEPROM Data Output The EEPROM Data Output pin is used for input from the SPI EEPROM memory device. The EE_DO includes an internal pull-up resistor.
EE_CS_N	TS	EEPROM Chip Select The EEPROM Chip Select signal is used to enable the device.
EE_SK	TS	EEPROM Serial Clock The EEPROM Shift Clock provides the clock rate for the SPI EEPROM interface, which is approximately 2 MHz.
FLSH_CE_N	TS	FLASH Chip Enable Output. Used to enable FLASH device.
FLSH_SCK	TS	FLASH Serial Clock Output.
FLSH_SI	TS	FLASH Serial Data Input. This pin is an output to the memory device.
FLSH_SO	I	FLASH Serial Data Output This pin is an input from the memory device.

3.7 LED Signals

Note: The LED signals are push-pull (active-high) outputs. They are fully programmable through the EEPROM interface

Symbol	Type	Name and Function
LED0_0	O	LED0_0. Programmable LED output for Port A. As the Link LED, it indicates link connectivity on Port A.
LED0_1	O	LED0_1. Programmable LED output for Port A. As the Activity LED, it flashes to indicate receive activity on Port A for packets destined for this node.
LED0_2	O	LED0_2 Programmable LED output for Port A. As the Link 100 LED, it indicates link at 100 Mbps for Port A.
LED0_3	O	LED0_3 Programmable LED output for Port A. As the Link 1000 LED, it indicates link at 1000 Mbps for Port A.
LED1_0	O	LED1_0. Programmable LED output for Port B. As the Link LED, it indicates link connectivity on Port B.



Symbol	Type	Name and Function
LED1_1	O	LED1_1 Programmable LED output for Port B. As the Activity LED, it flashes to indicate receive activity on Port B for packets destined for this node.
LED1_2	O	LED1_2 Programmable LED output for Port B. As the Link 100 LED, it indicates link at 100 Mbps for Port B.
LED1_3	O	LED1_3 Programmable LED output for Port B. As the Link 1000 LED, it indicates link at 1000 Mbps for Port B.

3.8 Other Signals

Symbol	Type	Name and Function
SDP0_0 SDP0_1 SDP0_2 SDP0_3 SDP1_0 SDP1_1 SDP1_2 SDP1_3	TS	Software Defined Pin (SDP) The Software Defined Pins are programmable with respect to input and output capability. These pins also can optionally be configured as interrupt inputs. SDP signals default to inputs upon power-up, but can be configured differently by the EEPROM.

3.9 Crystal Signals

Symbol	Type	Name and Function
XTAL1	AI	Crystal One The Crystal One pin is a 25 MHz input signal. It should be connected to a parallel resonant crystal with a frequency tolerance of 30 ppm or better. The other end of the crystal should be connected to XTAL2.
XTAL2	AO	Crystal Two Crystal Two is the output of an internal oscillator circuit used to drive a crystal into oscillation.



3.10 PHY Analog Signals

Symbol	Type	Name and Function
RBIAS0_P/RBIAS1_P	A	<p>Compensation Reference Resistor.</p> <p>A 1.4 KΩ, 1% tolerance resistor should be used. RBIAS_N should also be connected to ground (VSS).</p>
MDIO_P_0 MDIO_N_0 MDI1_P_0 MDI1_N_0	A	<p>Media Dependent Interface [0]</p> <p>1000BASE-T: In MDI configuration, these correspond to BI_DA+/-, and in MDI-X configuration, MDIp0/MDIn0 corresponds to BI_DB+/-.</p> <p>100BASE-TX: In MDI configuration, MDIp0/MDIn0 is used for the transmit pair, and in MDI-X configuration, MDIp0/MDIn0 is used for the receive pair.</p> <p>10BASE-T: In MDI configuration, MDIAp0/MDI_MINUS0_0 is used for the transmit pair, and in MDI-X configuration, MDIp0/MDIn0 is used for the receive pair.</p>
MDIO_P_1 MDIO_N_1 MDI1_P_1 MDI1_N_1	A	<p>Media Dependent Interface [1]</p> <p>1000BASE-T: In MDI configuration, MDIp1/MDIn1 corresponds to BI_DB+/-, and in MDI-X configuration, MDIp1/MDIn1 corresponds to BI_DA+/-.</p> <p>100BASE-TX: In MDI configuration, MDIp1/MDIn1 is used for the receive pair, and in MDI-X configuration, MDIp1/MDIn1 is used for the transmit pair.</p> <p>10BASE-T: In MDI configuration, MDIp1/MDIn1 is used for the receive pair, and in MDI-X configuration, MDIp1/MDIn1 is used for the transmit pair.</p>
MDIO_P_2 MDIO_N_2 MDI1_P_2 MDI1_N_2	A	<p>Media Dependent Interface [2]</p> <p>1000BASE-T: In MDI configuration, MDIp2/MDIn2 corresponds to BI_DC+/-, and in MDI-X configuration, MDIp2/MDIn2 corresponds to BI_DD+/-.</p> <p>100BASE-TX: Unused.</p> <p>10BASE-T: Unused.</p>
MDIO_P_3 MDIO_N_3 MDI1_P_3 MDI1_N_3	A	<p>Media Dependent Interface [3]</p> <p>1000BASE-T: In MDI configuration, MDIp3/MDIn3 corresponds to BI_DD+/-, and in MDI-X configuration, MDIp3/MDIn3 corresponds to BI_DC+/-.</p> <p>100BASE-TX: Unused.</p> <p>10BASE-T: Unused.</p>



3.11 Serializer/Deserializer Signals

Symbol	Type	Name and Function
SRDSI_0_P SRDSI_0_N SRDSI_1_P SRDSI_1_N	AI	SERDES Receive Pairs A and B These signals make the differential receive pair for the 1.25 GHz serial interface. For serializer/deserializer operation, the inputs should be coupled to ECL voltage levels. If the SERDES interface is not used, these pins should not be connected.
SRDSO_0_P SRDSO_0_N SRDSO_1_P SRDSO_1_N	AO	SERDES Transmit Pairs A and B These signals make the differential transmit pair for the 1.25 GHz serial interface. For serializer/deserializer operation, the outputs drive the LVPECL voltage levels. If the SERDES interface is not used, these pins should not be connected.
SRDS0_SIG_DET/ SRDS1_SIG_DET	I	Signal Detects A and B These pins indicate whether the SERDES signals (connected to the 1.25 GHz serial interface) have been detected by the optical transceivers. If the SERDES interface is not used with copper media, these can be left with no connection (NC). If the SERDES interface is not used with fiber media, the SIG_DET inputs should be tied high to VCC.
SER_RCOMP	A	SERDES Impedance Compensation. Connect the recommended resistor (1.4K Ω) from this ball to ground.
SFP0_I2C_CLK	O	Port 0 SFP I2C clock. Connects to Mod-Def1 input of SFP. Can also be used as MDC pin.
SFP0_I2C_DATA	TS/ OD	Port 0 SFP I2C data. Connects to Mod-Def2 pin of SFP. Can also be used as MDIO pin
SFP1_I2C_CLK	O	Port 1 SFP I2C clock. Connects to Mod-Def1 input of SFP. Can also be used as MDC pin.
SFP1_I2C_DATA	TS/ OD	Port 1 SFP I2C data. Connects to Mod-Def2 pin of SFP. Can also be used as MDIO pin

3.12 Test Interface Signals

Note: Pull-up resistors are needed on these signals as shown in the reference schematic.

Symbol	Type	Name and Function
JTCK	I	JTAG Test Access Port Clock
JTDI	I	JTAG Test Access Port Test Data In
JTDO	OD	JTAG Test Access Port Test Data Out
JTMS	I	JTAG Test Access Port Mode Select



3.13 Power Supply Connections

3.13.1 Digital and Analog Supplies

Symbol	Type	Name and Function
VCC3P3	P	3.3 V Digital Power Supply. For I/O circuits.
VCC1P8	P	1.8 V Analog Power Supply For PHY analog, PHY I/O, PCI Express analog, and Phase Lock Loop circuits, Connect all 1.8 V pins to a single power supply.
VCC1P0	P	1.0 V Digital Power Supply For core digital, PHY digital, PCI Express digital and clock circuits, connect all 1.0 V pins to a single power supply.

3.13.2 Grounds, Reserved Pins and No Connects

Symbol	Type	Name and Function
VSS	P	Ground.
RSVD_VCC		Reserved, VCC These pins are reserved by Intel and may have factory test functions. For normal operation, connect them directly to VCC. Do not connect them to pull-up resistors.
RSVD_GND	P	Reserved, Ground These pins are reserved by Intel and may have factory test functions. For normal operation, connect them directly to ground. Do not connect them to pull-down resistors.
RSVD_NC	P	Reserved, No Connect These pins are reserved by Intel and may have factory test functions. For normal operation, do not connect any circuitry to these pins. Do not connect pull-up or pull-down resistors.
NC	P	No Connect This pin is not connected internally.

4.0 Pinout/Signal Name

Table 1. Pinout

Name	Pin
PE_CLK_P	N2
PE_CLK_N	N1



PET_0_P	D2
PET_0_N	D1
PET_1_P	H2
PET_1_N	H1
PET_2_P	R2
PET_2_N	R1
PET_3_P	W2
PET_3_N	W1
PER_0_P	F2
PER_0_N	F1
PER_1_P	K2
PER_1_N	K1
PER_2_P	U2
PER_2_N	U1
PER_3_P	AA2
PER_3_N	AA1
PE_WAKE_N	AC20
PE_RST_N	AC9
PE_RCOMP	L1
RSVDM3_NC	M3
RSVDM2_NC	M2
FLSH_SI	AC14
FLSH_SO	AD14
FLSH_SCK	AD15
FLSH_CE_N	AC15



EE_DI	A21
EE_DO	A20
EE_SK	B20
EE_CS_N	B21
SMBD	AD21
SMBCLK	AC21
SMBALRT_N	AD20
RSVDAD17_NC	AD17
RSVDAC17_NC	AC17
RSVDAC16_NC	AC16
RSVDAD16_NC	AD16
NCSI_CLK_IN	B5
NCSI_CLK_OUT	B4
NCSI_CRD_DV	A4
NCSI_RXD_1	A6
NCSI_RXD_0	B7
NCSI_TX_EN	B6
NCSI_TXD_1	A7
NCSI_TXD_0	B8
SDP0_0	A16
SDP0_1	B16
SDP0_2	B17



SDP0_3	B15
SDP1_0	AD10
SDP1_1	A12
SDP1_2	A13
SDP1_3	AC10
RSVDAB19_NC	AB19
RSVDAB18_NC	AB18
RSVDAD9_3P3	AD9
MAIN_PWR_OK	AD4
DEV_OFF_N	B9
RSVDL14_1P0	L14
RSVDP14_1P0	P14
XTAL1	N23
XTAL2	N24
SRDSI_0_P	J23
SRDSI_0_N	J24
SRDSO_0_P	K23
SRDSO_0_N	K24
SRDSO_SIG_DET	A9
SRDSI_1_P	T23
SRDSI_1_N	T24
SRDSO_1_P	R23
SRDSO_1_N	R24



SRDS1_SIG_DET	A10
SER_RCOMP	L22
RSVDM23_NC	M23
RSVDM24_NC	M24
SFP0_I2C_CLK/ MDC0	AD19
SFP0_I2C_DATA/ MDIO0	AD18
SFP1_I2C_CLK/ MDC1	AC19
SFP1_I2C_DATA/ MDIO1	AC18
LED0_0	A19
LED0_1	B19
LED0_2	B18
LED0_3	A18
LED1_0	AD13
LED1_1	AC11
LED1_2	AC13
LED1_3	AC12
MDIO_P_0	C24
MDIO_N_0	C23
MDIO_P_1	D24
MDIO_N_1	D23
MDIO_P_2	F24
MDIO_N_2	F23
MDIO_P_3	G24



MDIO_N_3	G23
RBIAS0_P	E22
VSS	F22
IEEE_TEST0_P	A22
IEEE_TEST0_N	B22
MDI1_P_0	AB24
MDI1_N_0	AB23
MDI1_P_1	AA24
MDI1_N_1	AA23
MDI1_P_2	W24
MDI1_N_2	W23
MDI1_P_3	V24
MDI1_N_3	V23
RBIAS1_P	Y22
VSS	W22
IEEE_TEST1_P	AD22
IEEE_TEST1_N	AC22
RSVDAD8_VSS	AD8
JTCK	AC6
JTDI	AD7
JTDO	AC8
JTMS	AC7
RSVDAC5_NC	AC5
AUX_PWR	B14
LAN1_DIS_N	A15



RSVDB12_NC	B12
LAN0_DIS_N	B13
RSVDA8_3P3	A8
RSVDA11_3P3	A11
RSVDB10_3P3	B10
RSVDB11_3P3	B11
RSVDA14_VSS	A14
NCB3	B3
NCAC3	AC3
NCAD3	AD3
VCC3P3	AD6
VCC3P3	AD12
VCC3P3	A5
VCC3P3	A17
VCC1P8	P5
VCC1P8	P4
VCC1P8	N9
VCC1P8	N8
VCC1P8	N5
VCC1P8	N4
VCC1P8	M9
VCC1P8	M8
VCC1P8	M5
VCC1P8	M4
VCC1P8	L9
VCC1P8	L8
VCC1P8	L5
VCC1P8	L4
VCC1P8	L15
VCC1P8	K15



VCC1P8	J15
VCC1P8	H15
VCC1P8	G15
VCC1P8	E20
VCC1P8	E19
VCC1P8	D20
VCC1P8	D19
VCC1P8	Y20
VCC1P8	Y19
VCC1P8	V15
VCC1P8	U15
VCC1P8	T15
VCC1P8	R15
VCC1P8	P15
VCC1P8	AA20
VCC1P8	AA19
VCC1P8	N21
VCC1P8	N15
VCC1P8	M21
VCC1P8	M15
VCC1P8	P9
VCC1P8	P8
VCC1P0	R14
VCC1P0	R13
VCC1P0	R12
VCC1P0	R11
VCC1P0	P13
VCC1P0	P12
VCC1P0	L13
VCC1P0	L12
VCC1P0	K14
VCC1P0	K13



VCC1P0	K12
VCC1P0	K11
VCC1P0	V5
VCC1P0	V4
VCC1P0	U5
VCC1P0	U4
VCC1P0	P11
VCC1P0	N11
VCC1P0	M11
VCC1P0	L11
VCC1P0	H5
VCC1P0	H4
VCC1P0	G5
VCC1P0	G4
VCC1P0	J21
VCC1P0	J20
VCC1P0	J18
VCC1P0	J17
VCC1P0	L21
VCC1P0	L20
VCC1P0	L18
VCC1P0	L17
VCC1P0	K21
VCC1P0	K20
VCC1P0	K18
VCC1P0	K17
VCC1P0	T21
VCC1P0	T20
VCC1P0	T18
VCC1P0	T17
VCC1P0	P21
VCC1P0	P20
VCC1P0	P18



VCC1P0	P17
VCC1P0	R21
VCC1P0	R20
VCC1P0	R18
VCC1P0	R17
VSS	Y9
VSS	Y8
VSS	Y7
VSS	Y6
VSS	Y15
VSS	Y14
VSS	Y13
VSS	Y12
VSS	Y11
VSS	Y10
VSS	W9
VSS	W8
VSS	W7
VSS	W22
VSS	W14
VSS	W13
VSS	W12
VSS	W11
VSS	W10
VSS	V9
VSS	V8
VSS	V14
VSS	V13
VSS	V12
VSS	V11
VSS	V10
VSS	U9



VSS	U14
VSS	U13
VSS	U12
VSS	U11
VSS	U10
VSS	T14
VSS	T13
VSS	T12
VSS	T11
VSS	N14
VSS	N13
VSS	N12
VSS	M14
VSS	M13
VSS	M12
VSS	J14
VSS	J13
VSS	J12
VSS	J11
VSS	H9
VSS	H14
VSS	H13
VSS	H12
VSS	H11
VSS	H10
VSS	G9
VSS	G8
VSS	G14
VSS	G13
VSS	G12
VSS	G11
VSS	G10
VSS	F22



VSS	F9
VSS	F8
VSS	F7
VSS	F14
VSS	F13
VSS	F12
VSS	F11
VSS	F10
VSS	E9
VSS	E8
VSS	E7
VSS	E6
VSS	E15
VSS	E14
VSS	E13
VSS	E12
VSS	E11
VSS	E10
VSS	D9
VSS	D8
VSS	D7
VSS	D6
VSS	D5
VSS	D16
VSS	D15
VSS	D14
VSS	D13
VSS	D12
VSS	D11
VSS	D10
VSS	C9
VSS	C8
VSS	C7



VSS	C6
VSS	C5
VSS	C4
VSS	C17
VSS	C16
VSS	C15
VSS	C14
VSS	C13
VSS	C12
VSS	C11
VSS	C10
VSS	B2
VSS	B1
VSS	AD5
VSS	AD2
VSS	AD11
VSS	AD1
VSS	AC4
VSS	AC2
VSS	AC1
VSS	AB9
VSS	AB8
VSS	AB7
VSS	AB6
VSS	AB5
VSS	AB4
VSS	AB17
VSS	AB16
VSS	AB15
VSS	AB14
VSS	AB13
VSS	AB12
VSS	AB11



VSS	AB10
VSS	AA9
VSS	AA8
VSS	AA7
VSS	AA6
VSS	AA5
VSS	AA16
VSS	AA15
VSS	AA14
VSS	AA13
VSS	AA12
VSS	AA11
VSS	AA10
VSS	A3
VSS	A2
VSS	A1
VSS	Y24
VSS	Y23
VSS	Y21
VSS	Y18
VSS	Y17
VSS	Y16
VSS	W21
VSS	W20
VSS	W19
VSS	W18
VSS	W17
VSS	W16
VSS	W15
VSS	V22
VSS	V21
VSS	V20
VSS	V19



VSS	V18
VSS	V17
VSS	V16
VSS	U24
VSS	U23
VSS	U22
VSS	U21
VSS	U20
VSS	U19
VSS	U18
VSS	U17
VSS	U16
VSS	T22
VSS	T19
VSS	T16
VSS	R22
VSS	R19
VSS	R16
VSS	P24
VSS	P23
VSS	P22
VSS	P19
VSS	P16
VSS	N22
VSS	N20
VSS	N19
VSS	N18
VSS	N17
VSS	N16
VSS	M22
VSS	M20
VSS	M19
VSS	M18



VSS	M17
VSS	M16
VSS	L24
VSS	L23
VSS	L19
VSS	L16
VSS	K22
VSS	K19
VSS	K16
VSS	J22
VSS	J19
VSS	J16
VSS	H24
VSS	H23
VSS	H22
VSS	H21
VSS	H20
VSS	H19
VSS	H18
VSS	H17
VSS	H16
VSS	G22
VSS	G21
VSS	G20
VSS	G19
VSS	G18
VSS	G17
VSS	G16
VSS	F21
VSS	F20
VSS	F19
VSS	F18
VSS	F17



VSS	F16
VSS	F15
VSS	E24
VSS	E23
VSS	E21
VSS	E18
VSS	E17
VSS	E16
VSS	D22
VSS	D21
VSS	D18
VSS	D17
VSS	C22
VSS	C21
VSS	C20
VSS	C19
VSS	C18
VSS	B24
VSS	B23
VSS	AD24
VSS	AD23
VSS	AC24
VSS	AC23
VSS	AB22
VSS	AB21
VSS	AB20
VSS	AA22
VSS	AA21
VSS	AA18
VSS	AA17
VSS	A24
VSS	A23
VSS	Y5



VSS	Y4
VSS	Y3
VSS	Y2
VSS	Y1
VSS	W6
VSS	W5
VSS	W4
VSS	W3
VSS	V7
VSS	V6
VSS	V3
VSS	V2
VSS	V1
VSS	U8
VSS	U7
VSS	U6
VSS	U3
VSS	T9
VSS	T8
VSS	T7
VSS	T6
VSS	T5
VSS	T4
VSS	T3
VSS	T2
VSS	T10
VSS	T1
VSS	R9
VSS	R8
VSS	R7
VSS	R6
VSS	R5
VSS	R4



VSS	R3
VSS	R10
VSS	P7
VSS	P6
VSS	P3
VSS	P2
VSS	P10
VSS	P1
VSS	N7
VSS	N6
VSS	N3
VSS	N10
VSS	M7
VSS	M6
VSS	M10
VSS	M1
VSS	L7
VSS	L6
VSS	L3
VSS	L2
VSS	L10
VSS	K9
VSS	K8
VSS	K7
VSS	K6
VSS	K5
VSS	K4
VSS	K3
VSS	K10
VSS	J9
VSS	J8
VSS	J7
VSS	J6



VSS	J5
VSS	J4
VSS	J3
VSS	J2
VSS	J10
VSS	J1
VSS	H8
VSS	H7
VSS	H6
VSS	H3
VSS	G7
VSS	G6
VSS	G3
VSS	G2
VSS	G1
VSS	F6
VSS	F5
VSS	F4
VSS	F3
VSS	E5
VSS	E4
VSS	E3
VSS	E2
VSS	E1
VSS	D4
VSS	D3
VSS	C3
VSS	C2
VSS	C1
VSS	AB3
VSS	AB2
VSS	AB1
VSS	AA4



VSS	AA3
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5.0 Power Requirements

5.1 Targeted Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings¹

Symbol	Parameter	Min	Max	Unit
VCC(3.3)	DC supply voltage on 3.3 V pins with respect to VSS	VSS - 0.5	4.6	V
VCC(1.8)	DC supply voltage on 1.8 V pins with respect to VSS ²	VSS - 0.3	2.5	V
VCC(1.0)	DC supply voltage on 1.0 V pins with respect to VSS ^b	VSS - 0.2	1.7	V
V _I / V _O	3.3 V I/O Voltage 1.8 V I/O Voltage 1.0 V I/O Voltage	VSS - 0.5 VSS - 0.3 VSS - 0.2	4.6 2.5 1.7	V
I _O	DC output current	N/A	TBD	mA
T _{storage}	Storage temperature range	-65	140	°C
T _{case}	Case temperature under bias	0	85	°C
	ESD per MIL_STD-883 Test Method 3015, Specification 2001V Latchup Over/Undershoot: 150 mA, 125° C	N/A	VDD overstress: VDD(3.3) * (7.2 V)	V

1. Maximum ratings are referenced to ground (VSS). Permanent device damage is likely to occur if the ratings in this table are exceeded for an indefinite duration. These values should not be used as the limits for normal device operations.
2. During normal device power up and power down, the 1.8 V and 1.0 V supplies must not ramp before the 3.3 V supply.

5.2 Targeted Recommended Operating Conditions

5.2.1 General Operating Conditions

Table 3. Recommended Operating Conditions¹

Symbol	Parameter	Min	Max	Unit
VCC(3.3)	DC supply voltage on 3.3 V pins	3.0	3.6	V
VCC(1.8)	DC supply voltage on 1.8 V pins	1.71	1.89	V
VCC(1.0)	DC supply voltage on 1.0 V pins	0.95	1.05	V
t _R / t _F	Input rise/fall time (normal input)	0	200	ns
T _a	Operating temperature range (ambient)	0	55	°C
T _J	Junction temperature	N/A	≤110	°C

1. Sustained operation of the device at conditions exceeding these values, even if they are within the absolute maximum rating limits, might result in permanent damage. Device functionality to stated DC and AC limits is not guaranteed, if conditions exceed recommended operating conditions.



5.2.2 Voltage Ramp and Sequencing Recommendations

The following tables give the specifications for the power supply ramps:

Table 4. 3.3 V Supply Voltage Ramp

Parameter	Description	Min	Max	Unit
Rise Time	Time from 10% to 90% mark	0.1	100 ¹	ms
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Slope	Ramp rate at any time between 10% to 90%	24	28800	mV/ms
Operational Range	Voltage range for normal operating conditions	3	3.6	V
Ripple	Maximum voltage ripple at a bandwidth equal to 50 MHz	N/A	70	mV _{peak-peak}
Ripple	Overshoot time upon ramp ²	N/A	0.05	ms
Overshoot	Maximum voltage allowed ^b	N/A	100	mV

1. Good design practices achieve voltage ramps to within the regulation bands in approximately 20 ms or less.
2. Excessive overshoot can affect long term reliability.

Table 5. 1.8 V Supply Voltage Ramp

Parameter	Description	Min	Max	Unit
Rise Time	Time from 10% to 90% mark	0.1	100 ¹	ms
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Slope	Ramp rate at any time between 10% to 90%	14	60000	mV/ms
Operational Range	Voltage range for normal operating conditions	1.71	1.89	V
Ripple	Maximum voltage ripple at a bandwidth equal to 1 MHz	N/A	40	mV _{peak-peak}
Overshoot SettlingTime	Overshoot time upon ramp ²	N/A	0.1	ms
Overshoot	Maximum voltage allowed ^b	N/A	100	mV

1. Good design practices achieve voltage ramps to within the regulation bands in approximately 20 ms or less.
2. Excessive overshoot can affect long term reliability.

Table 6. 1.0 V Supply Voltage Ramp

Parameter	Description	Min	Max	Unit
Rise Time	Time from 10% to 90% mark	0.1	100 ¹	ms
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Slope	Ramp rate at any time between 10% to 90%	7.6	33600	mV/ms
Operational Range	Voltage range for normal operating conditions	0.95	1.05	V



Ripple	Maximum voltage ripple at a bandwidth equal to 1 MHz	N/A	40	mV _{peak-peak}
Overshoot SettlingTime	Overshoot time upon ramp ²	N/A	0.05	ms
Overshoot	Maximum voltage allowed ^b	N/A	100	mV

1. Good design practices achieve voltage ramps to within the regulation bands in approximately 20 ms or less.
2. Excessive overshoot can affect long term reliability.

Table 7. Power Supply Sequencing

Symbol	Parameter	Min	Max	Unit
T _{3 18}	VCC3p3 (3.3 V) stable to VCC1p8 stable	0	100	ms
T _{18 1}	VCC1p8 stable to VCC (1.0 V) stable	0		ms
T _{3 1}	VCC3p3 (3.3 V) stable to VCC (1.0 V) stable	0	100	mV
T _{m-per} , T _{m-ppo}	3.3 V core to GIO_PWR_GOOD and MAIN_PWR_OK on	TBD		ms
T _{per-m} , T _{ppo-m}	GIO_PWR_GOOD, MAIN_PWR_OK off before 3.3 V core down	0		ms

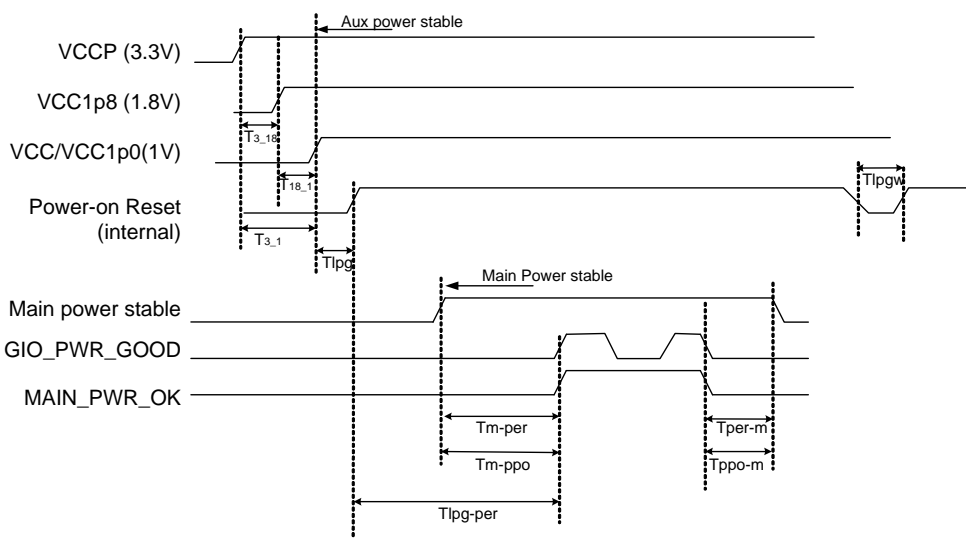


Figure 2. Voltage Power Sequencing Options

To meet the 375 mA inrush current requirements (not including external capacitors) the ramp time should be 5 ms - 100 ms on all power rails. For faster ramps (100 us - 5 ms), expect higher inrush current due to the high charging current of the decoupling capacitors of 3.3 V, 1.8 V and 1.0 V rails.



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6.0 Thermal

The 82575 device is specified for operation when the ambient temperature (TA) is within the range of 0 °C to 55 °C. For information about the thermal characteristics of the device, including operation outside this range, please refer to the 82575 Thermal Application Note.

7.0 Electrical Specification

7.1 DC Specifications

Table 8. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VCC(3.3)	DC supply voltage on 3.3 V pins		3.00	3.30	3.60	V
VCC(1.8)	DC supply voltage on 1.8 V pins		1.71	1.80	1.89	V
VCC(1.0)	DC supply voltage on 1.0 V pins		0.95	1.00	1.05	V

Table 9. I/O Characteristics

Symbol	Parameter	Condition ¹	Min	Typ	Max	Units
V _{IH}	Input high voltage		2.0	N/A	VCC(3.3) + 0.5	V
V _{IL}	Input low voltage		-0.5	N/A	0.8	V
I _{IN}	Input current	V _{IN} = VDD(3.3) or V _{SS}	-15	N/A	15	μA
V _{OH}	Output high voltage	I _{OH} = -16 mA V _{CC} = Min	2.4	N/A	N/A	V
		I _{OH} = -100 μA V _{CC} = Min	V _{CC} - 0.02	N/A	N/A	
V _{OL}	Output low voltage	I _{OL} = 14 mA V _{CC} = Min	N/A	N/A	0.4	V
		I _{OL} = 100 μA V _{CC} = Min	N/A	N/A	0.2	
I _{OZ}	Off-state output leakage current	V _O = V _{CC} or V _{SS}	-10	N/A	10	μA
C _{IN} ²	Input capacitance		N/A	2.5	N/A	pF
PU	Internal pull-up		2.6	N/A	5.5	kΩ
V _{OS}	Overshoot		N/A	N/A	4.0	V
V _{US}	Undershoot		N/A	N/A	-0.4	V

1. The input buffer also has hysteresis > 160 mV.



2. C_{in} = 2.5 pF(maximum input capacitance), C_{out} = 16 pF (characterized max output load capacitance per 160 MHz).

Table 10. Open Drain I/O

Symbol	Parameter	Condition	Min	Max	Units	Note
VCC3P3	Periphery supply		3.0	3.6	V	
VCC	Core supply		0.9	1.32	V	
Vih	Input High Voltage		2.1		V	
Vil	Input Low Voltage			0.8	V	
Ileakage	Output Leakage Current	$0 < V_{in} < VCC3P3$		+/-10	µA	2
Vol	Output Low Voltage	@ Ipullup		0.4	V	4
Ipullup	Current sinking	Vol=0.4V	4		mA	
Cin	Input Pin Capacitance			7	pF	3
Cout	Output Pin Capacitance			30	pF	3
Ioffsmb	Input leakage current	VCC3P3 off or floating		+/-10	µA	2

Notes:

1. Applies to SMBD0, SMBCLK0, SMBALRT_N, PE_WAKE_n, SFP1_I2C_Data, SFP0_I2C_Data pads.
2. Device meets this whether powered or not.
3. Characterized, not tested.
4. OD no high output drive. VOL max=0.4V at 14mA, VOL max=0.2V at 0.1mA

Table 11. Power Consumption

	D0a--Active Link					
	@10 Mbps	@100 Mbps	@ 1000 Mbps (copper)		@ 1000 Mbps (SERDES)	
	Typ I _{cc} (mA) ¹	Typ I _{cc} (mA) ¹	Typ I _{cc} (mA) ¹	Max I _{cc} (mA) ¹	Typ I _{cc} (mA) ¹	Max I _{cc} (mA) ²
3.3 V	18	18	18	23	19	19
1.8 V	344	312	841	856	142	203
1.0 V	304	388	856	1184	354	492
Total Device Power	0.98 W	1.01 W	2.43 W	2.80 W	0.67 W	0.92 W

1. Typical conditions: operating temperature (T_A) = 25 C, nominal voltages and moderate network traffic at full duplex.
2. Maximum conditions: maximum operating temperature (T_J) values, typical voltage values and continuous network traffic at full duplex.



	D0a--Idle Link Unplugged--no link LOs only Typ I _{cc} (mA) ¹
3.3 V	18
1.8 V	129
1.0 V	264
Total Device Power²	0.56

1. Typical conditions: room temperature (TA)=25C, nominal voltages and idle network (no traffic) at full duplex
2. Known errata on LOs & L1 states might impact device power consumption

	D0a--Idle Link @10Mbps LOs only Typ I _{cc} (mA) ¹
3.3 V	18
1.8 V	140
1.0 V	302
Total Device Power²	0.61 W

1. Typical conditions: room temperature (TA)=25C, nominal voltages and idle network (no traffic) at full duplex
2. Known errata on LOs & L1 states might impact device power consumption

	D0a--Idle Link @100Mbps (Copper) LOs only Typ I _{cc} (mA) ¹
3.3 V	18



	D0a--Idle Link @100Mbps (Copper) LOs only Typ I _{cc} (mA) ¹
1.8 V	837
1.0 V	755
Total Device Power²	2.32 W

1. Typical conditions: room temperature (TA)=25C, nominal voltages and idle network (no traffic) at full duplex
2. Known errata on LOs & L1 states might impact device power consumption

	D0a--Idle Link @1000Mbps (SERDES) Typ I _{cc} (mA) ¹
3.3 V	17
1.8 V	142
1.0 V	341
Total Device Power²	0.65 W

1. Typical conditions: room temperature (TA)=25C, nominal voltages and idle network (no traffic) at full duplex
2. Known errata on LOs & L1 states might impact device power consumption

	D3cold - wake-up enabled		D3cold-wake disabled
	@10 Mbps	@100 Mbps	
	Typ I _{cc} (mA)	Typ I _{cc} (mA)	Typ I _{cc} (mA)
3.3 V	18	18	18



	D3cold - wake-up enabled		D3cold-wake disabled
	@10 Mbps	@100 Mbps	
	Typ Icc (mA)	Typ Icc (mA)	Typ Icc (mA)
1.8 V	98	269	83
1.0 V	168	249	70
Total Device Power	0.40 W	0.79 W	0.29 W

	D(r) Uninitialized
	Disabled through DEV_OFF_N Typ Icc (mA)
3.3 V	11
1.8 V	179
1.0 V	283
Total Device Power	0.64

7.2 Resets

Power-on Reset (internal): The 82575 has an internal mechanism for sensing the power pins. Once the power is up and stable, it creates an internal reset, this reset acts as a master reset of the entire chip. It is level sensitive, and while it is 0, will hold all of the registers in reset. Power-on Reset is interpreted to be an indication that device power supplies are all stable. Power-on Reset changes state during system power-up.

In-band PCIe Reset: The 82575 will generate an internal reset in response to a physical layer message from the PCIe or when the PCIe link halts (entry to Polling or Detect state). This reset is equivalent to PCI reset in previous (PCI) gigabit LAN controllers.

Main_Power_Good: Used by the device to detect the D3Cold condition and activate part of the power saving scheme. Also used to change the state of the ASF manageability firmware.



7.3 Pull-up and Pull-down Specifications and Signals

Table 12. Internal and External Pull-up and Pull-down Values

	Min	Nominal	Max	Units
PU (Internal)	2.7K	5K	8.6K	Ω
PU (External, recommended)		≤3K		Ω
PD (External, recommended)		≤400		Ω

For external Pull-up requirements, see the 82575 reference schematics.

The table below lists internal & external pull-up resistors and whether they are activated in the different device states. Each internal PUP has a nominal value of 5kΩ, ranging from 2.7KΩ to 8.6KΩ.

The device states are defined as follow:

Power-up = while 3.3 V is stable, but not 1.0 V

Active = normal mode (not power up nor disable)

Disable = device disabled

Table 13. Internal Pull-up and External Pull Up Requirements

Signal Name	Power up	Active	Disable	External Recommended?	Notes
PE_WAKE_N	N	N	N	Y	
PE_RST_N	Y	N	N	N	
FLSH_SI	Y	N	Y	N	
FLSH_SO	Y	Y	Y	N	
FLSH_SCK	Y	N	Y	N	
FLSH_CE_N	Y	N	Y	Y	
EE_DI	Y	N	Y	N	
EE_DO	Y	Y	Y	N	
EE_SK	Y	N	Y	N	
EE_CS_N	Y	N	Y	Y	
SMBD	N	N	N	Y	
SMBCLK	N	N	N	Y	
SMBALRT_N	N	N	N	Y	



NCSI_CLK_IN	N	N	N	N	
NCSI_CLK_OUT	Y	N	N	N	
NCSI_CRSDV	N	N	N	Y	Pull down only if NCSI is NOT being used or configured for multi drop
NCSI_RXD[1:0]	N	N	N	Y	Pull Up only if NCSI is NOT being used or configured for multi drop
NCSI_TX_EN	N	N	N	N	Should be connected to external PD if NCSI is NOT used
NCSI_TXD[1:0]	N	N	N	N	Should be connected to external PD if NCSI is NOT used
SDP0[3:0]	Y	Y	N	N	
SDP1[3:0]	Y	Y	N	N	
DEV_OFF_N	Y	N	N		Must be connected on board
MAIN_PWR_OK	Y	N	N		Must be connected on board
SRDS_0_SIG_DET	Y	N	N		Must be connected externally
SRDS_1_SIG_DET	Y	N	N		Must be connected externally
SFP0_I2C_CLK	Y	N	Y	Y if active	If used.
SFP0_I2C_DATA	Y	N	N	Y	If used.
SFP1_I2C_CLK	Y	N	Y	Y if active	If used.
SFP1_I2C_DATA	Y	N	N	Y	If used.
LED0_0	Y	N	N		
LED0_1	Y	N	N		
LED0_2	Y	N	N		
LED0_3	Y	N	N		
LED1_0	Y	N	N		
LED1_1	Y	N	N		
LED1_2	Y	N	N		
LED1_3	Y	N	N		
JTCK	Y	N	N	N	



JTDI	Y	N	N	Y	
JTDO	Y	N	N	Y	
JTMS	Y	N	N	Y	
AUX_PWR	Y	N	N	Y (or PD)	
LAN1_DIS_N	Y	Y	Y		
LAN0_DIS_N	Y	Y	Y		

7.4 Targeted AC Characteristics

Table 14. 25 MHz Clock Input Requirements

Symbol	Parameter	Min	Typ	Max	Unit
f0	Frequency	N/A	25.000	N/A	MHz
df0	Frequency Variation	-50	N/A	+50	ppm
Dc	Duty Cycle	40	N/A	60	%
tr	Rise Time	N/A	N/A	5	ns
tf	Fall Time	N/A	N/A	5	ns
Jptp	Clock Jitter (peak-to-peak) ¹	N/A	N/A	250	ps
C _{in}	Input Capacitance	N/A	20	N/A	pF
T	Operating Temperature	N/A	N/A	70	°C
Aptp	Input clock amplitude (peak-to-peak)	1.0	1.2	1.3	V
Vcm	Clock common mode	N/A	0.6	N/A	V

1. Clock jitter is defined according to the recommendations of part 40.6.1.2.5 IEEE 1000Base-T Standard (at least 10⁵ clock edges, filtered by HPF with cut off frequency of 5000 Hz).

Table 15. Link Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
fGTX ¹	GTX_CLK frequency	N/A	125	N/A	MHz

1. GTX_CLK is used externally for test purposes only. See signals IEEE_TEST1_p and IEEE_TEST1_n.

7.4.1 EEPROM Interface

Applicable over recommended operating range from Ta = -40C to +85C, VCC3P3 = 3.3 V, Cload = 1 TTL Gate and 16pF (unless otherwise noted).

Symbol	Parameter	Min	Typ	Max	Units	Note
--------	-----------	-----	-----	-----	-------	------



t_{SCK}	SCK clock frequency	0	2	2.1	MHz	[1]
t_{RI}	Input rise time		2.5ns	2	us	
t_{FI}	Input fall time		2.5ns	2	us	
t_{WH}	SCK high time	200	250		ns	[2]
t_{WL}	SCK low time	200	250		ns	
t_{CS}	CS high time	250			ns	
t_{CSS}	CS setup time	250			ns	
t_{CSH}	CS hold time	250			ns	
t_{SU}	Data-in setup time	50			ns	
t_H	Data-in hold time	50			ns	
t_V	Output valid	0		200	ns	
t_{HO}	Output hold time	0			ns	
t_{DIS}	Output disable time			250	ns	

1. Clock is 2MHz
2. 50% duty cycle

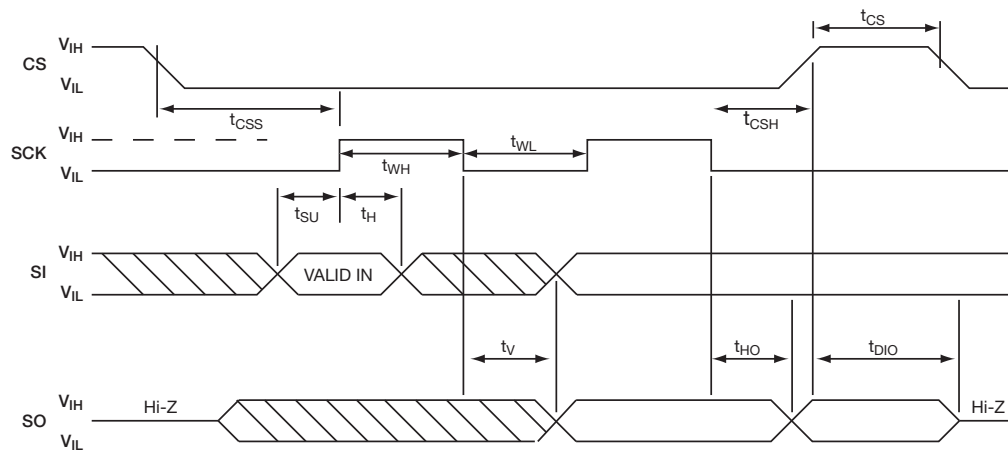


Figure 3. EEPROM Interface Time Diagram

7.4.2 FLASH Interface

Applicable over recommended operating range from $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC3P3} = 3.3\text{ V}$, $C_{load} = 1\text{ TTL Gate and }16\text{ pF}$ (unless otherwise noted)

Table 16. FLASH Parameters

Symbol	Parameter	Min	Typ	Max	Units	Note
t_{SCK}	SCK clock frequency	0	15.625	20	MHz	[1]
t_{RI}	Input rise time		2.5	20	ns	
t_{FI}	Input fall time		2.5	20	ns	
t_{WH}	SCK high time	20	32		ns	[2]
t_{WL}	SCK low time	20	32		ns	[2]
t_{CS}	CS high time	25			ns	
t_{CSS}	CS setup time	25			ns	
t_{CSH}	CS hold time	25			ns	
t_{SU}	Data-in setup time	5			ns	
t_H	Data-in hold time	5			ns	
t_V	Output valid			20	ns	
t_{HO}	Output hold time	0			ns	
t_{DIS}	Output disable time			100	ns	

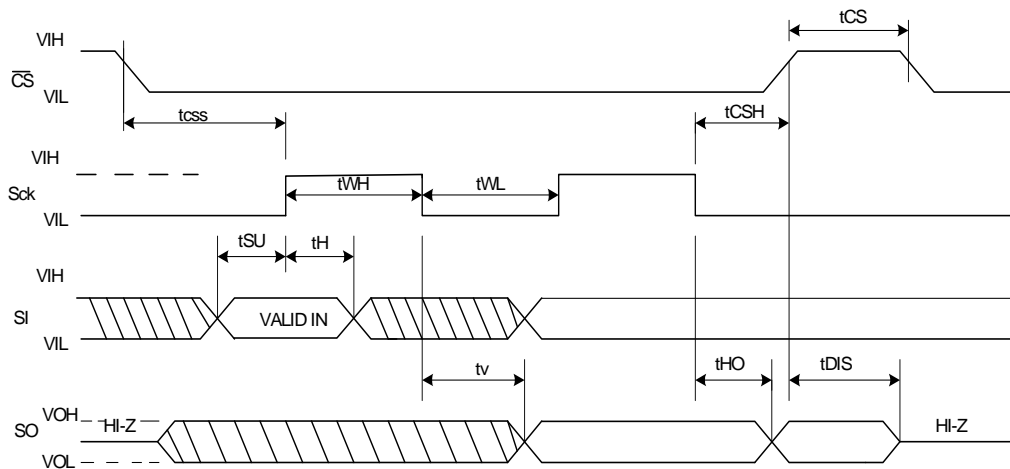


Figure 4. FLASH Timing Diagram

7.4.3 NC-SI Interface

Table 17. NC-SI AC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
--------	-----------	-----	-----	-----	-------	-------



	REF_CLK Frequency		50		MHz	2
	REF_CLK Duty Cycle	35		65	%	1
	REF_CLK accuracy			100	ppm	
Tsu	TXD[1:0], TX_EN, Data Setup to REF_CLK rising edge	3			ns	
Thold	TXD[1:0], TX_EN Data hold from REF_CLK rising edge	1.5			ns	6
Tval	RXD[1:0], CRS_DV Data valid from REF_CLK rising edge	1.8		9	ns	
Tor	RXD[1:0], CRS_DV Output Time rise	0.5		6	ns	3
Tof	RXD[1:0], CRS_DV Output Time fall	0.5		6	ns	3
Todr1	RXD[1:0], CRS_DV Output delay rise	2		5.8	ns	3
Todf1	RXD[1:0], CRS_DV Output delay fall	2		5.8	ns	3
Tidr2	TXD[1:0], TX_EN Input delay rise	0.5		6	ns	4, 5
Tidf2	TXD[1:0], TX_EN Input delay fall	0.5		6	ns	4, 5
Tir	TXD[1:0], TX_EN Input Time rise	0.02		0.15	ns	4, 5
Tif	TXD[1:0], TX_EN Input Time fall	0.02		0.15	ns	4, 5

Notes:

1. Clock Duty cycle measurement: High interval measured from Vih to Vil points, Low from Vil to next Vih
2. Clock interval measurement from Vih to Vih
3. Load = 25 pF
4. Load = 200 fF
5. The input delay test conditions: Maximum input level = VIN = 2.7V; Input rise/fall time (0.2VIN to 0.8VIN) = 1ns (Slew Rate ~ 1.5ns).
6. The NC-SI specification defines a hold time of 1.0 ns. In order to work with the 82575, the board designer should guarantee a hold time of 1.5 ns.

7.4.4 SMBus Interface

Table 18. SMBus AC Characteristics (master mode)

Symbol	Parameter	Min	Typ	Max	Units
F _{SMB}	SMBus Frequency		74.4	100	kHz
T _{BUF}	Time between STOP and START condition driven by the device		6.56		μs
T _{HD:STA}	Hold time after Start Condition. After this period, the first clock is generated.		6.72		μs
T _{SU:STA}	Start Condition setup time				μs
T _{SU:STO}	Stop Condition setup time		6.88		μs
T _{HD:DAT}	Data hold time		0.48		μs
T _{TIMEOUT}	Detect SMBClk low timeout	26.2		31.5	ms
T _{LOW}	SMBClk low time		5.76		μs

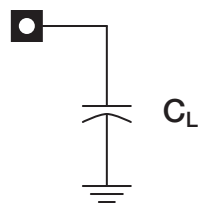
T_{HIGH}	SMBCIk high time		6.56		μs
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Table 19. SMBus AC Characteristics (slave mode)

Symbol	Parameter	Min	Typ	Max	Units
F_{SMB}	SMBus Frequency		74.4	100	kHz
T_{BUF}	Time between STOP and START condition driven by the device		6.56		μs
$T_{HD:STA}$	Hold time after Start Condition. After this period, the first clock is generated.		6.72		μs
$T_{SU:STA}$	Start Condition setup time		TBD		μs
$T_{SU:STO}$	Stop Condition setup time		6.88		μs
$T_{HD:DAT}$	Data hold time		0.48		μs
$T_{TIMEOUT}$	Detect SMBCIk low timeout	26.2		31.5	ms
T_{LOW}	SMBCIk low time		5.76		μs
T_{HIGH}	SMBCIk high time		6.56		μs

Table 20. AC Test Loads for General Output Pins

Symbol	Parameter	Min	Typ	Max	Unit
C_L	Capacitance of test load	N/A	16	N/A	pF


Figure 5. AC Test Loads for General Output Pins



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8.0 Crystal Requirements

Table 21. Reference Crystal Specification Requirements

Parameter Name	Symbol	Recommended Value	Conditions
Frequency	f_o	25.000 [MHz]	@25 [°C]
Vibration mode		Fundamental	
Cut		AT	
Operating /Calibration Mode		Parallel	
Frequency Tolerance @25°C	$\Delta f/f_o @25^\circ\text{C}$	±30 [ppm]	@25 [°C]
Temperature Tolerance	$\Delta f/f_o$	±30 [ppm]	
Operating Temperature	T_{opr}	-20 to +70 [°C]	
Non Operating Temperature Range	T_{opr}	-40 to +90 [°C]	
Equivalent Series Resistance (ESR)	R_s	50 [Ω] maximum	@25 [MHz]
Load Capacitance	C_{load}	20 [pF] (max 24pF)	
Shunt Capacitance	C_o	6 [pF] maximum	
Pullability from Nominal Load Capacitance	$\Delta f/C_{load}$	15 [ppm/pF] maximum	
Max Drive Level	D_L	0.5 [mW]	
Insulation Resistance	IR	500 [MΩ] minimum	@ 100V DC
Aging	$\Delta f/f_o$	±5 [ppm/year]	
Differential board capacitance*	C_D	2 [pF]	
Board Capacitance	C_s	4 [pF]	
External Capacitors	C_1, C_2	27 [pF]	
Board Resistance	R_s	0.1 [Ω]	

9.0 LED Configuration

The 82575 provides 4 LEDs per port that may be used to indicate the status of the traffic. The default setup of the LEDs is done via the EEPROM words 1Ch and 1Fh. The default setup for both ports is the same. This setup is reflected in the LEDCTL register of each port. Each driver may change its setup individually. For each of the LEDs the following parameters can be defined:

1. Mode: Defines which information is reflected by this LED. The encoding is described in the LEDCTL register.
2. Polarity: Defines the polarity of the LED.
3. Blink mode: should the LED blink or be stable.

In addition, the blink rate of all LEDs can be defined. The possible rates are 200 ms or 83 ms for each phase. There is one rate for all LEDs



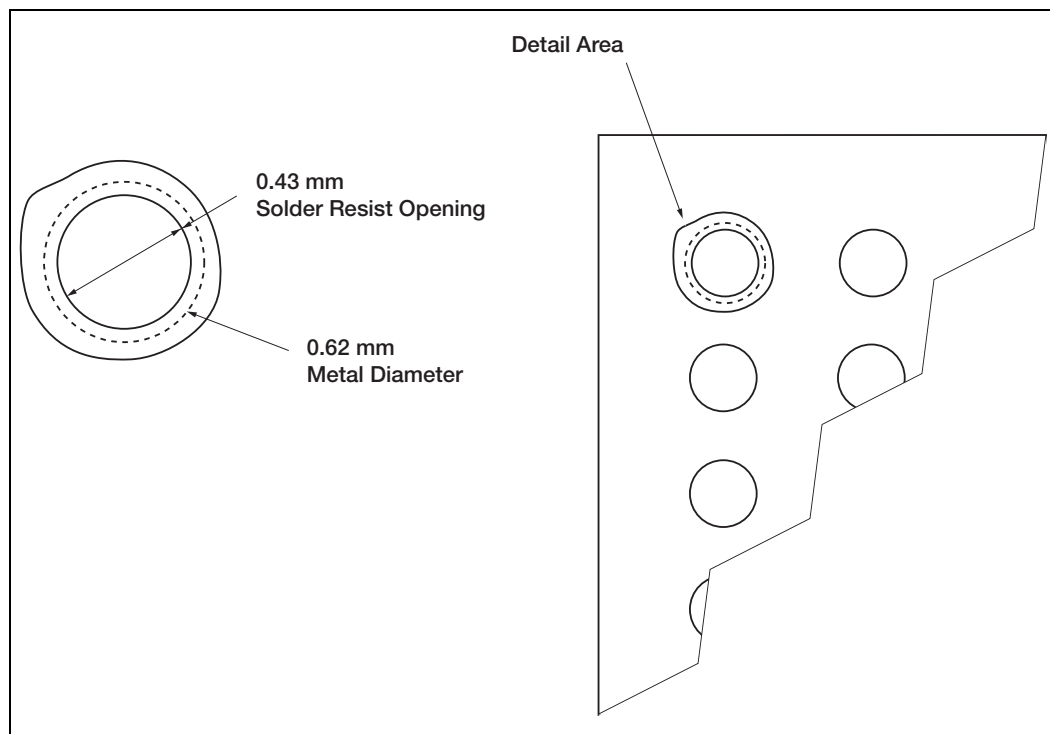
10.0 Mechanical Information

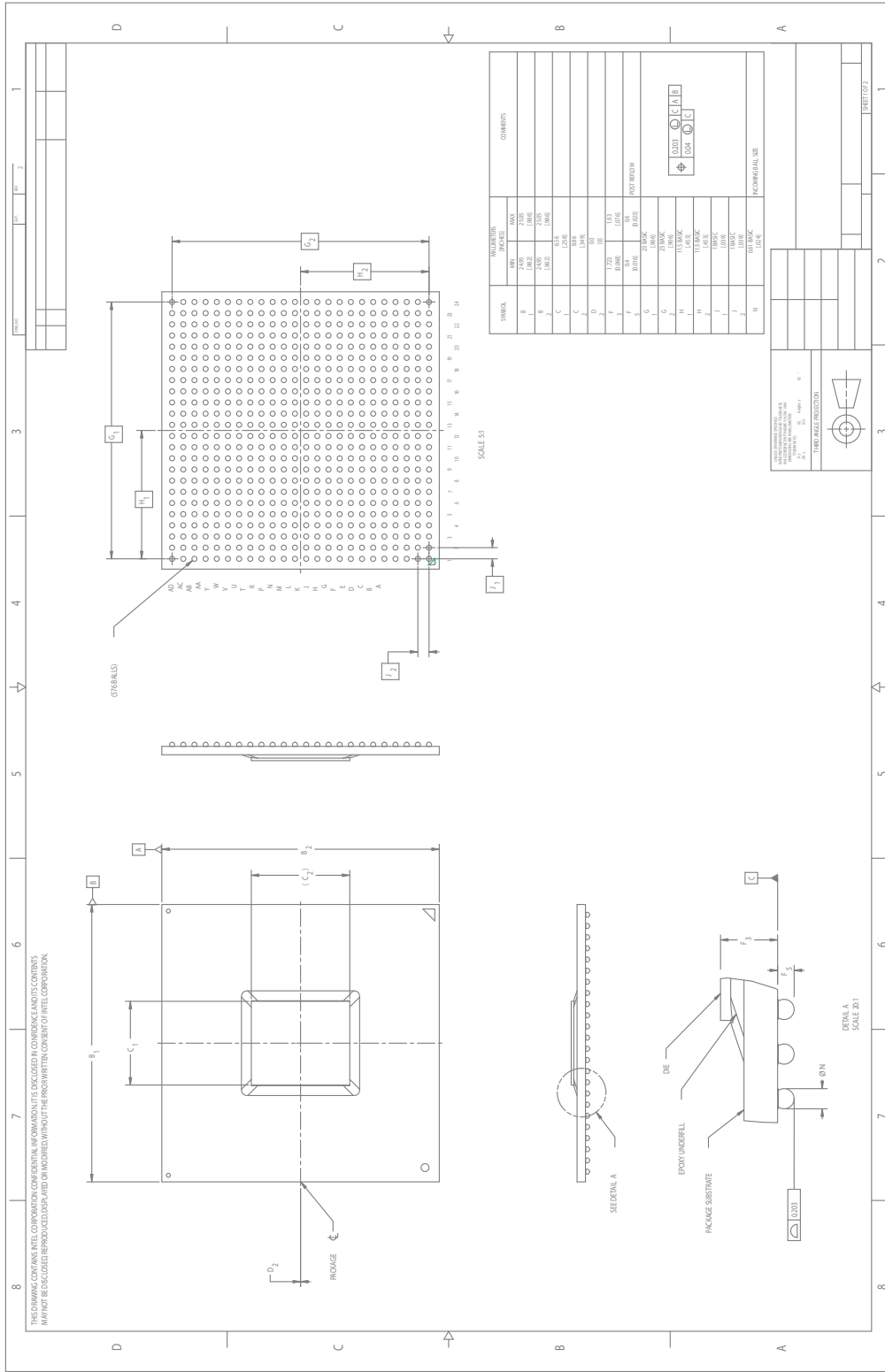
This section describes the 82575 device physical characteristics.

The targeted signal names are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

10.1 Targeted Package Information

The 82575 device is a 576-lead flip-chip ball grid array (FC-BGA) measuring 25 mm by 25 mm. The nominal ball pitch is 1 mm. See Figure 9.





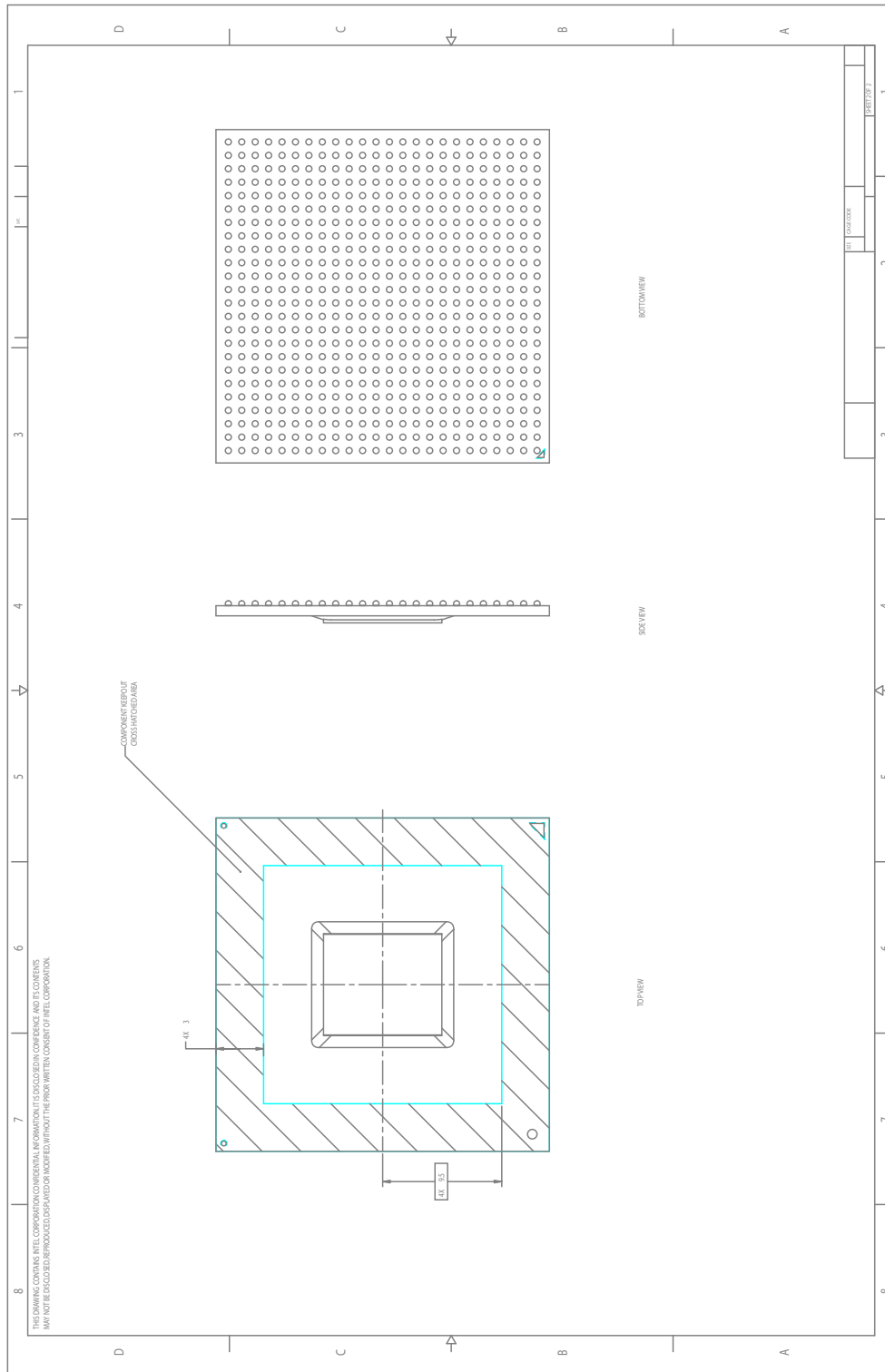


Figure 6. 82575 Mechanical Specifications



10.2 Visual Pin Assignments

This section contains the illustrations of the pin outs.

Figure 7. 82575 Visual Pin Assignment Part 1 (Top View)

	24	23	22	21	20	19	18	17	16	15	14	13
AD	VSS	VSS	IEEE_T EST1_P	SMBD	SMBALRT_N	SFP0_I2C_ CLK	SFP0_I2C_ Data	FLBMD	FLBSINTCKE X	FLSH_SCK	FLSH_SO	LED1_0
AC	VSS	VSS	IEEE_T EST1_N	SMBCLK	PE_WAKE_N	SFP1_I2C_ CLK	SFP1_I2C_ Data	FLBMCK	FLBSD	FLSH_CE_N	FLSH_SI	LED1_2
AB	MDI1_P_0	MDI1_N_0	VSS	VSS	VSS	RSVDAB19 _NC	RSVDAB18 _NC	VSS	VSS	VSS	VSS	VSS
AA	MDI1_P_1	MDI1_N_1	VSS	VSS	VCC1P8	VCC1P8	VSS	VSS	VSS	VSS	VSS	VSS
Y	VSS	VSS	RBIAS1 _P	VSS	VCC1P8	VCC1P8	VSS	VSS	VSS	VSS	VSS	VSS
W	MDI1_P_2	MDI1_N_2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
V	MDI1_P_3	MDI1_N_3	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC1P8	VSS	VSS
U	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC1P8	VSS	VSS
T	SRDSL_1_ N	SRDSL_1_ P	VSS	VCC1P0	VCC1P0	VSS	VCC1P0	VCC1P0	VSS	VCC1P8	VSS	VSS
R	SRDSO_1_ N	SRDSO_1_ P	VSS	VCC1P0	VCC1P0	VSS	VCC1P0	VCC1P0	VSS	VCC1P8	VCC1P0	VCC1P0
P	VSS	VSS	VSS	VCC1P0	VCC1P0	VSS	VCC1P0	VCC1P0	VSS	VCC1P8	RSVDP 1P014	VCC1P0
N	XTAL2	XTAL1	VSS	VCC1P8	VSS	VSS	VSS	VSS	VSS	VCC1P8	VSS	VSS



Figure 8. 82575 Visual Pin Assignment Part 2 (Top View)

M	RSVDM 24 NC	RSVDM 23 NC	VSS	VCC1P8	VSS	VSS	VSS	VSS	VSS	VCC1P8	VSS	VSS
L	VSS	VSS	SER_ RCOMP	VCC1P0	VCC1P0	VSS	VCC1P0	VCC1P0	VSS	VCC1P8	RSVDL 14 1P0	VCC1P0
K	SRDSO_0_ N	SRDSO_0_ P	VSS	VCC1P0	VCC1P0	VSS	VCC1P0	VCC1P0	VSS	VCC1P8	VCC3P3	VCC1P0
J	SRDSI_0_ N	SRDSI_0_ P	VSS	VCC1P0	VCC1P0	VSS	VCC1P0	VCC1P0	VSS	VCC1P8	VSS	VSS
H	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC1P8	VSS	VSS
G	MDIO_P_3	MDIO_N_3	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC1P8	VSS	VSS
F	MDIO_P_2	MDIO_N_2		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
E	VSS	VSS	RBIAS0 _P	VSS	VCC1P8	VCC1P8	VSS	VSS	VSS	VSS	VSS	VSS
D	MDIO_P_1	MDIO_N_1	VSS	VSS	VCC1P8	VCC1P8	VSS	VSS	VSS	VSS	VSS	VSS
C	MDIO_P_0	MDIO_N_0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
B	VSS	VSS	IEEE_T EST0_N	EE_CS_N	EE_SK	LED0_1	LED0_2	SDP0_2	SDP0_1	SDP0_3	AUX_PWR	LAN0_DIS_N
A	VSS	VSS	IEEE_T EST0_P	EE_DI	EE_DO	LED0_0	LED0_3	VCC3P3	SDP0_0	LAN1_DIS_N	RSVDA14 _NC	SDP1_2
	24	23	22	21	20	19	18	17	16	15	14	13



Figure 9. 82575 Visual Pin Assignment Part 3(Top View)

12	11	10	9	8	7	6	5	4	3	2	1	
VCC3P3	VSS	SDP1_0	RSVDAD9_NC	RSVDAD8_NC	JTDI	VCC3P3	VSS	MAIN_PWR_OK	NCAD3	VSS	VSS	AD
LED1_3	LED1_1	SDP1_3	PE_RST_N	JTDO	JTMS	JTCK	RSVDAC5_NC	VSS	NCAC3	VSS	VSS	AC
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AB
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PER_3_P	PER_3_N	AA
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	Y
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PET_3_P	PET_3_N	W
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC1P0	VCC1P0	VSS	VSS	VSS	V
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC1P0	VCC1P0	VSS	PER_2_P	PER_2_N	U
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	T
VCC1P0	VCC1P0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PET_2_P	PET_2_N	R
VCC1P0	VCC1P0	VSS	VCC1P8	VCC1P8	VSS	VSS	VCC1P8	VCC1P8	VSS	VSS	VSS	P
VSS	VCC1P0	VSS	VCC1P8	VCC1P8	VSS	VSS	VCC1P8	VCC1P8	VSS	PE_CLK_P	PE_CLK_N	N

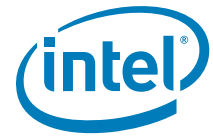


Figure 10. 82575 Visual Pin Assignment Part 4 (Top View)

VSS	VCC1P0	VSS	VCC1P8	VCC1P8	VSS	VSS	VCC1P8	VCC1P8	RSVDM3_NC	RSVDM2_NC	VSS	M
VCC1P0	VCC1P0	VSS	VCC1P8	VCC1P8	VSS	VSS	VCC1P8	VCC1P8	VSS	VSS	PE_RCOMP	L
VCC1P0	VCC1P0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PER_1_P	PER_1_N	K
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	J
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC1P0	VCC1P0	VSS	PET_1_P	PET_1_N	H
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC1P0	VCC1P0	VSS	VSS	VSS	G
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PER_0_P	PER_0_N	F
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	E
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PET_0_P	PET_0_N	D
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	C
RSVDB12_NC	RSVDB11_NC	RSVDB10_NC	DEV_OFF_N	RMII_TXD[0]	RMII_RXD_0	RMII_TX_EN	RMII_CLK_IN	RMII_CLK_OUT	NCB3	VSS	VSS	B
SDP1_1	RSVDA11_NC	SRDS1_SIG_DET	SRDS0_SIG_DET	RSVDA8_NC	RMII_TXD[1]	RMII_RXD_1	VCC3P3	RMII_CRSDV	VSS	VSS	VSS	A
12	11	10	9	8	7	6	5	4	3	2	1	

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