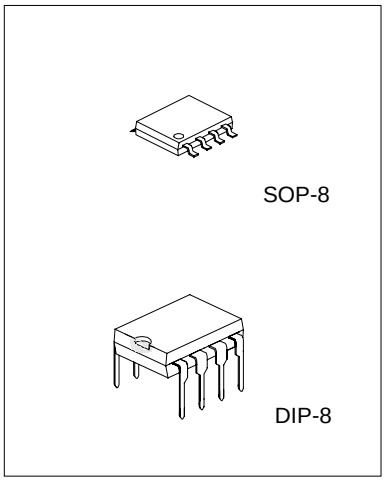
PC POWER SUPPLY SUPERVISORS



DESCRIPTION

The UTC 3511 provides protection circuits, power good output (PGO), fault protection latch (FPL_N), and protection detector function (PDON_N) control.

It can minimize external components of switching power supply systems in personal computer.

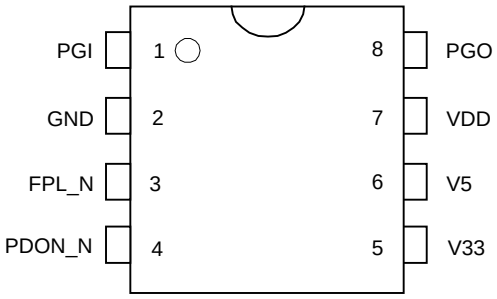
The Over Voltage Detector (OVD) monitors 3.3V, 5V, 12V input voltage level. The Under Voltage Detector (UVD) monitors 3.3V, 5V input voltage level. When OVD or UVD detect the fault voltage level, the FPL_N is latched HIGH and PGO goes LOW. The latch can be reset by PDON_N going HIGH. There is 2.4ms delay time for PDON_N turning off FPL_N.

When OVD and UVD detect the right voltage level, the power good output (PGO) will be issue.

FEATURES

* The Over Voltage Detector (OVD) monitors 3.3V, 5V, 12V input voltage level.
* The Under Voltage Detector (UVD) monitors 3.3V, 5V input voltage level.
* Both of the power good output (PGO) and the fault protection latch (FPL_N) are Open Drain Output.
* 75 ms time delay for UVD.
* 300 ms time delay for PGO.
* 38 ms for PDON_N input signal De-bounce.
* 73 us for internal signal De-glitches.
* 2.4 ms time delay for PDON_N turn-off FPL_N.

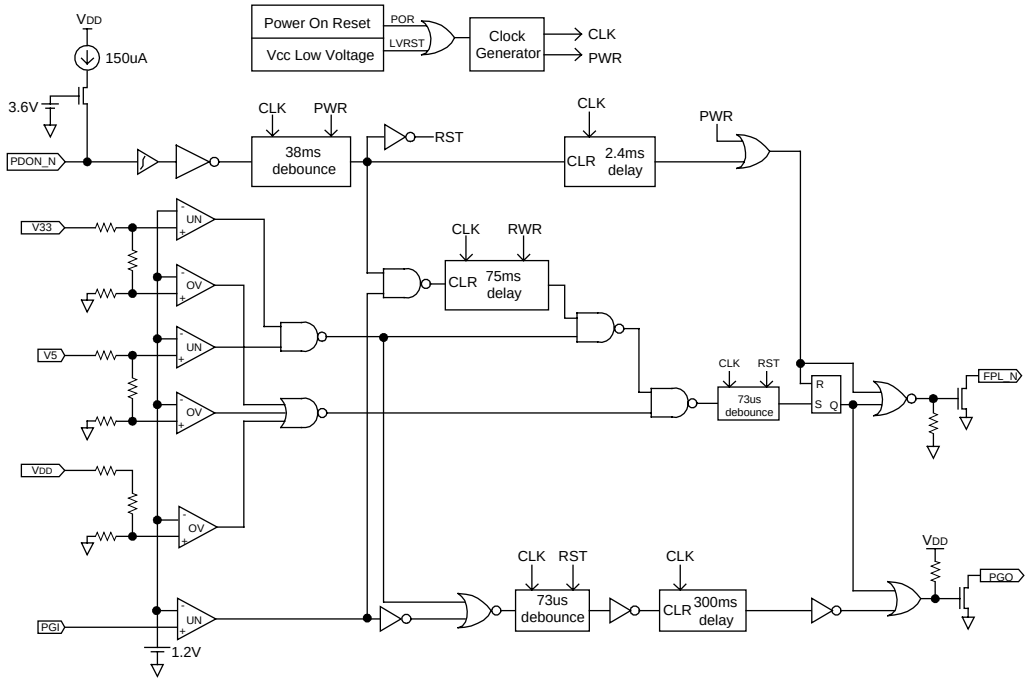
PIN CONFIGURATION



PIN DESCRIPTION

PIN No.	PIN NAME	TYPE	DESCRIPTION
1	PGI	I	Power good input pin
2	GND	P	Ground
3	FPL-N	O	Fault protection latch output pin (open drain output)
4	PDON-N	I	Protection detector function ON/OFF control input pin
5	V33	I	3.3V input pin
6	V5	I	5V input pin
7	VDD	I	Supply voltage/12V input pin
8	PGO	O	Power good output pin(open drain output)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Supply voltage		V_{DD}	-0.3 ~ 16	V
Input Voltage	PDON_N,V5,V33,PGI	Vin	-0.3 ~ 7	V
Output Voltage	FPL_N	V_{OUT}	-0.3 ~ 16	V
	PGO		-0.3 ~ 7	
Operating temperature		Topr	-40 ~ 125	°C
Storage temperature		Tstg	-55 ~ 150	°C

Note:Stresses above those listed may cause permanent damage to the devices

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{DD}	3.8	12	15	V
Input Voltage	PDON_N,V5,V33,PGI	Vin			7	V
Output Voltage	FPL_N	V_{OUT}			15	V
	PGO				7	V
Output Sink Current	FPL_N	Iosink			30	mA
	PGO				10	mA
Supply Voltage Rising Time		Trs	1			ms

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{DD}=5V)

Over Voltage Detection

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
Over voltage threshold	V33		3.7	3.9	4.1	V
	V5		5.7	6.1	6.5	
	V_{DD}/ V12		12.8	13.4	13.9	
Leakage current (FPL_N)	$I_{LEAKAGE}$	FPL_N=5V		5		uA
Low level output voltage (FPL_N)	V_{OL}	I_{sink}=10mA		0.3		V
		I_{sink}=30mA		0.7		

PGI and PGO

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
Under voltage threshold	V33		2.55	2.69	2.83	V
	V5		4.1	4.3	4.47	
Input threshold voltage (PGI)	V_{PGI}		1.16	1.20	1.24	
Leakage current (PGO)	$I_{LEAKAGE}$	PGO=5V		5		uA
Low level output voltage (PGO)	V_{OL}	I_{sink}=10mA		0.4		V

PDON_N

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
Input pull-up current	I_I	PDON_N=0V		150		uA
High-level input voltage	V_{IH}		2.4			V
Low-level input voltage	V_{IL}				1.2	V

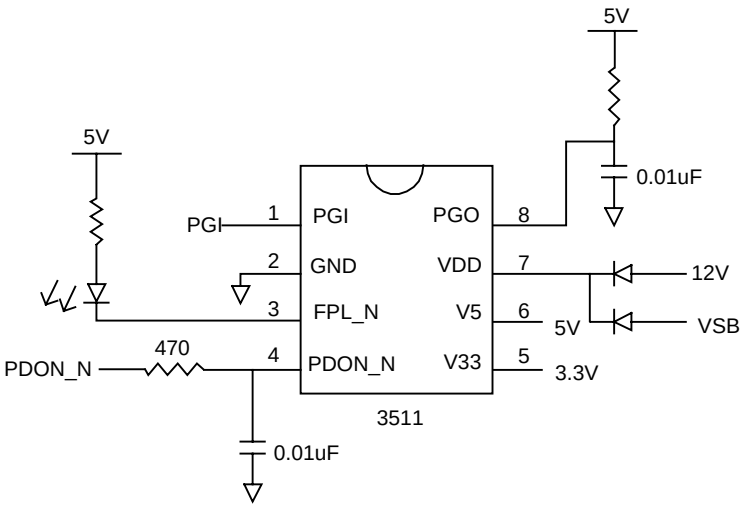
TOTAL DEVICE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
Supply current	Icc	PDON_N=5V			1	mA
low voltage	V_{DD}			3		V

SWITCHING CHARACTERISTICS, V_{DD}=5V

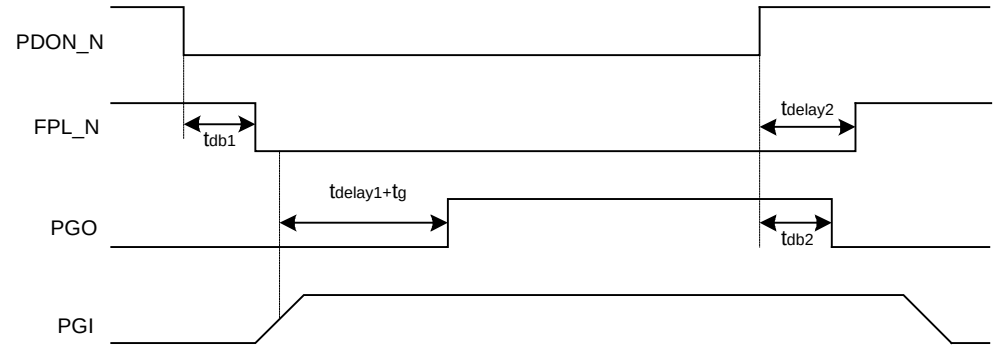
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
De-bounce time (PDON_N)	t_{db1}		32	38	61	ms
Delay time (PGI to PGO)	t_{delay}	Ta=-40°C ~ 125°C	200	300	490	ms
De-bounce time (PDON_N)	t_{db2}		32	38	61	ms
De-glitch time	t_g		63	73	120	us
PDON_N to FPL_N delay time	t_{delay2}		T_{db2}+2.0	T_{db2}+2.4	T_{db2}+3.8	ms
Internal UVD delay time	t_{delay3}	FPL_N go low & every Time PGI>1.2V	65	75	122	ms

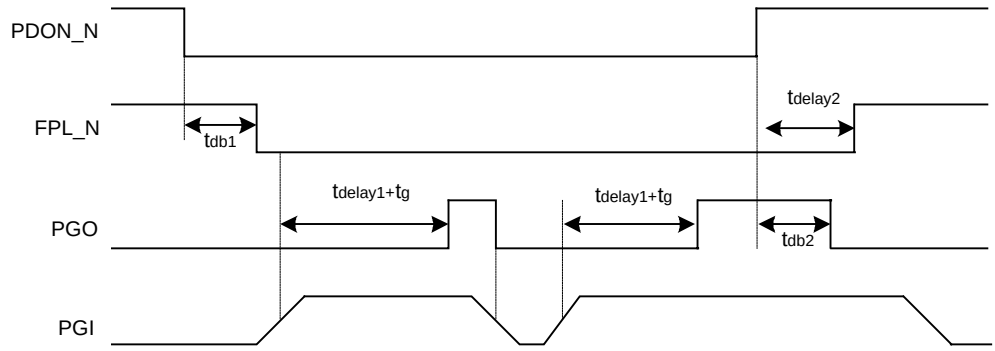
APPLICATION CIRCUIT



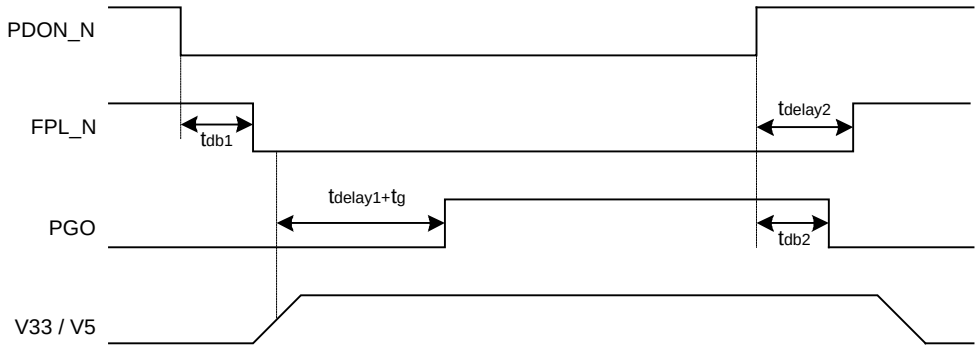
APPLICATION TIMMING

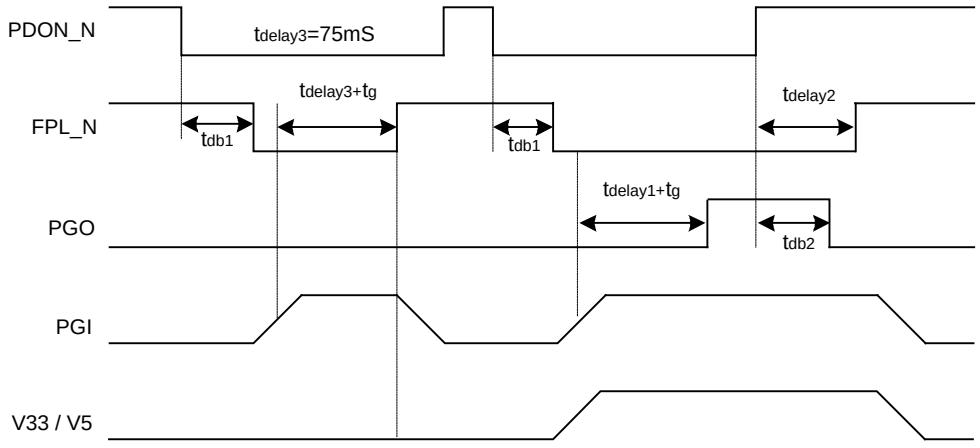
1. PGI (UNDER_VOLTAGE):





2. V33,V5 (UNDER_VOLTAGE):





3. V33,V5,V12 (OVER_VOLTAGE):