INTERSIL

3N172, 3N173 Diode Protected P-Channel Enhancement Mode MOS FET

FEATURES

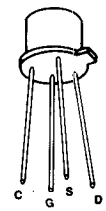
- High Input Impedance
- Diode Protected Gate

MAXIMUM RATINGS (@ 25°C ambient unless noted)

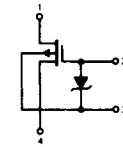
		3N172	3N173
V_{GSS}	Gate to Source Voltage	-40V	-30V
V_{DSS}	Drain to Source Voltage	-40V	-30V
V_{SDS}	Source to Drain Voltage	-40V	-30V
V_{DGO}	Drain to Gate Voltage	-40V	-30V
I_D	Drain Current	-50 mA	-50 mA
$I_{G(f)}$	Gate Forward Current	10 μA	10 μA
$I_{G(r)}$	Gate Reverse Current	1.0 mA	1.0 mA
P_D	Power Dissipation	375 mW	
	Derating Factor	3.0 mW/°C	
T_J	Operating Junction Temperature	-55 to +150°C	
T_{stg}	Storage Temperature	-65 to +200°C	
T_L	Lead Temperature 1/16" from Case for 10 sec max	+256°C	

PIN CONFIGURATION

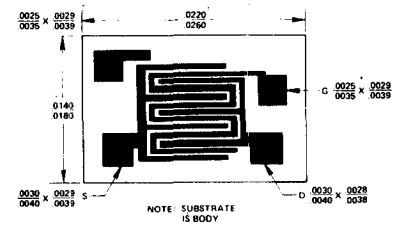
TO-72



DEVICE SCHEMATIC



CHIP TOPOGRAPHY 1503 Z



ORDERING INFORMATION

TO-72	WAFER	DICE
3N172	3N172/W	3N172/D
3N173	3N173/W	3N173/D

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

PARAMETER		3N172		3N173		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSS}	Gate Reverse Current		-200		-500	pA	V_{GS} = -20V
I_{GSS}	Gate Reverse Current (+125°C)		-0.5		-1.0	μA	V_{GS} = -20V
BV_{GSS}	Gate Breakdown Voltage	-40	-125	-30	-125	V	I_D = -10 μA
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30		V	I_D = -10 μA
BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30		V	I_S = -10 μA, V_{DB} = 0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = V_{GS}, I_D = -10 μA
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = -15V, I_D = -10 μA
V_{GS}	Gate Source Voltage	-3.0	-6.5	-2.5	-6.5	V	V_{DS} = -15V, I_D = -500 μA
I_{DSS}	Zero Gate Voltage Drain Current		-0.4		-10	nA	V_{DS} = -15V
I_{SDS}	Zero Gate Voltage Source Current		-0.4		-10	nA	V_{SD} = -15V, V_{DB} = 0
$r_{ds(on)}$	Drain Source On Resistance		250		350	ohms	V_{GS} = -20V, I_D = -100 μA
$I_{D(th)}$	On Drain Current	-5.0	-30	-5.0	-30	mA	V_{DS} = -15V, V_{GS} = -10V