



64K x 4 SRAM

SRAM MEMORY ARRAY

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-88681
- MIL-STD-883

FEATURES

- High Speed: 15, 20, 25, 35, 45, 55, and 70
- Battery Backup: 2V data retention
- Low power standby
- High-performance, low-power, CMOS double-metal process
- Single +5V ($\pm 10\%$) Power Supply
- Easy memory expansion with CE\
- All inputs and outputs are TTL compatible

OPTIONS

MARKING

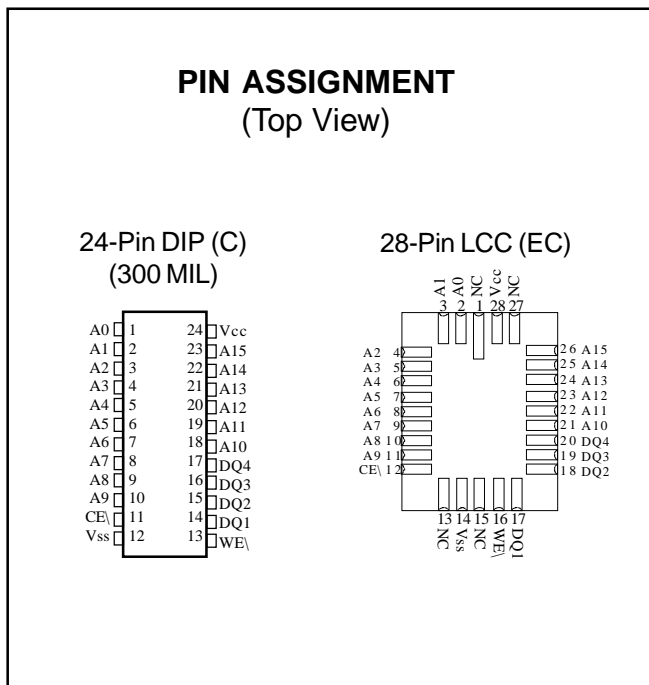
- **Timing**

15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
55ns access	-55*
70ns access	-70*
- **Package(s)**

Ceramic DIP (300 mil)	C	No. 106
Ceramic LCC	EC	No. 204
- **Operating Temperature Ranges**

Industrial (-40°C to +85°C)	IT
Military (-55°C to +125°C)	XT
- 2V data retention/low power L

*Electrical characteristics identical to those provided for the 45ns access devices.



GENERAL DESCRIPTION

The Austin Semiconductor SRAM family employs high-speed, low-power CMOS and are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Austin Semiconductor offers chip enable (CE\) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x4 configuration features common data input and output.

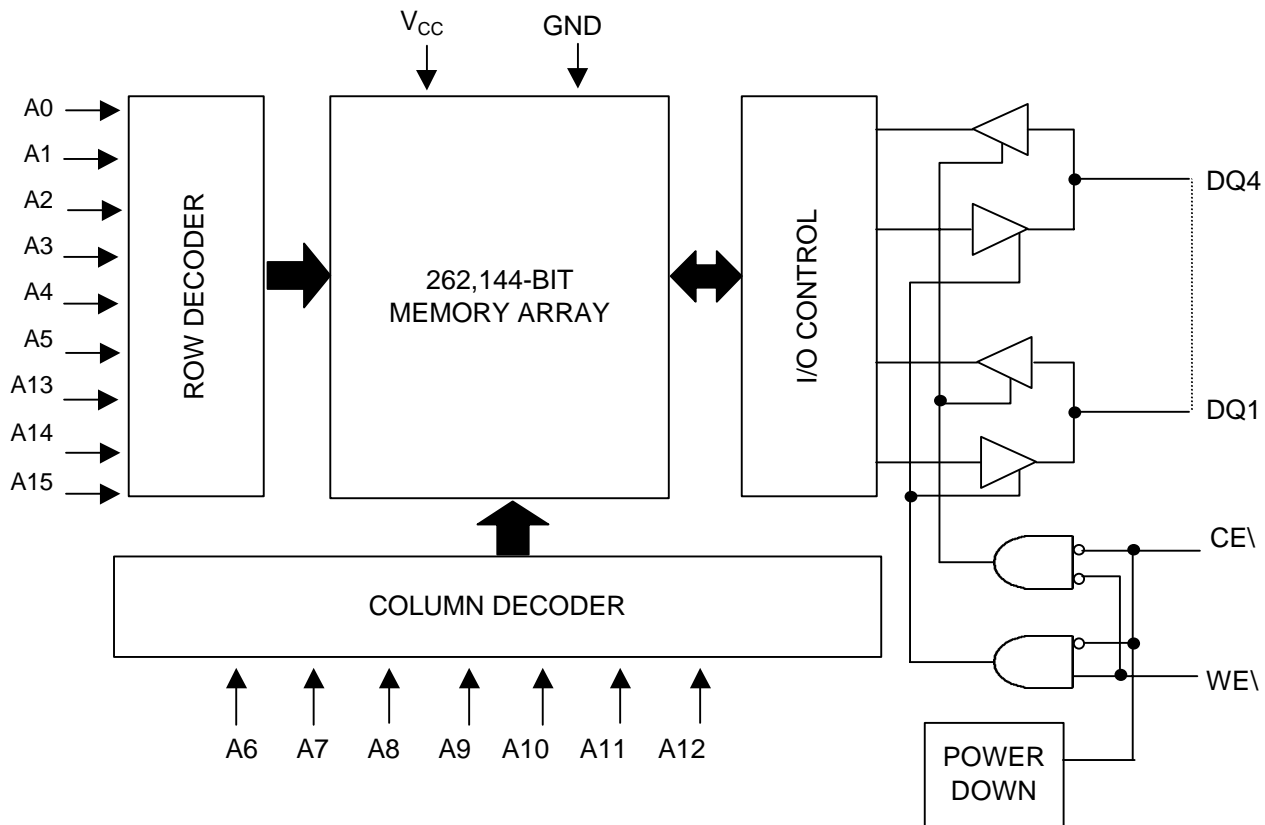
Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

These devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

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www.austinsemiconductor.com**



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	CE\	WE\	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V _{ss}	-0.5V to +7V
Voltage on V _{cc} Supply Relative to V _{ss}	-0.5V to +7V
Storage Temperature.....	-65°C to +150°C
Power Dissipation.....	1W
Short Circuit Output Current.....	50mA
Lead Temperature (soldering 10 seconds).....	+260°C
Junction Temperature.....	+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_c ≤ 125°C; V_{cc} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{CC} +0.5	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-10	10	μA	
Output Leakage Current	Output(s) disabled 0V ≤ V _{OUT} ≤ V _{CC}	I _{LO}	-10	10	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1

PARAMETER	CONDITIONS	SYM	MAX					UNITS	NOTES
			-15	-20	-25	-35	-45		
Power Supply Current: Operating	CE\ ≤ V _{IL} ; V _{CC} = MAX f = MAX = 1/t _{RC} (MIN) Output Open	I _{CC}	165	150	140	120	120	mA	3
Power Supply Current: Standby	CE\ ≥ V _{IH} ; All Other Inputs ≤ V _{IL} or ≥ V _{IH} ; V _{CC} = MAX f = 0 Hz	I _{SBT2}	45	45	40	25	25	mA	
	CE\ ≥ V _{CC} - 0.2V; V _{CC} = MAX V _{IL} ≤ V _{SS} + 0.2V V _{IH} ≥ V _{CC} - 0.2V; f = 0 Hz	I _{SBC2}	20	20	20	20	20	mA	
	"L" Version Only	I _{SBC2}	4	4	4	4	4	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYM	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C, f = 1MHz	C _I	10	pF	4
Output Capacitance	V _{CC} = 5V	C _O	12	pF	4



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

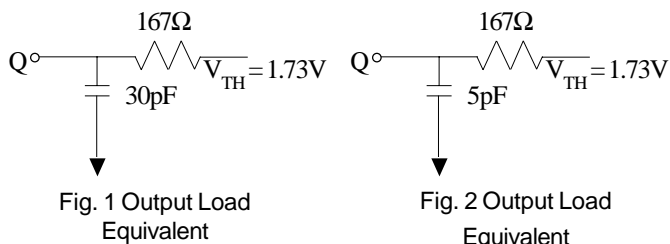
(Note 5) ($-55^{\circ}\text{C} \leq T_c \leq 125^{\circ}\text{C}$; $V_{cc} = 5V \pm 10\%$)

DESCRIPTION	SYMBOL	-15		-20		-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE													
READ cycle time	t_{RC}	15		20		25		35		45		ns	
Address access time	t_{AA}		15		20		25		35		45	ns	
Chip Enable access time	t_{ACE}		15		20		25		35		45	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		3		3		3		ns	7
Chip disable to output in High-Z	t_{HZCE}		8		10		10		20		20	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		ns	4
Chip disable to power-down time	t_{PD}		15		20		25		35		45	ns	4
WRITE CYCLE													
WRITE cycle time	t_{WC}	15		20		25		35		45		ns	
Chip Enable to end of write	t_{CW}	12		15		18		30		40		ns	
Address valid to end of write	t_{AW}	12		15		18		30		40		ns	
Address setup time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	2		2		2		5		5		ns	
WRITE pulse width	t_{WP}	12		15		17		30		40		ns	
Data setup time	t_{DS}	7		10		12		20		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	0		0		0		0		0		ns	7
Write Enable to output in High-Z	t_{HZWE}	0	7	0	10	0	11	0	20	0	20	ns	6, 7



ACTEST CONDITIONS

Input pulse levels	V _{ss} to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2



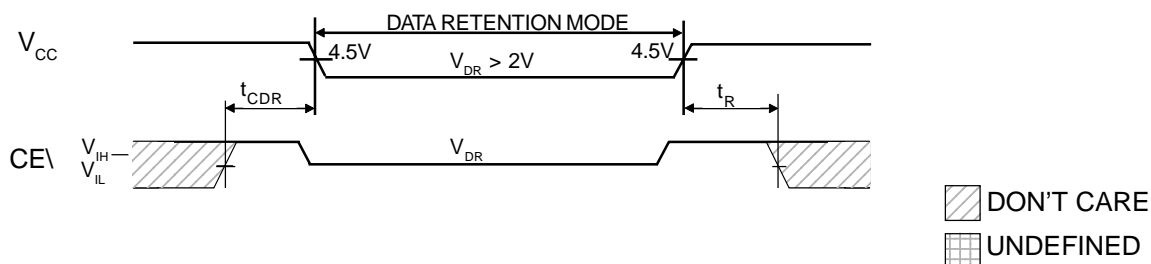
NOTES

- All voltages referenced to V_{SS} (GND).
- 3V for pulse width < 20ns
- I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{RC(MIN)}$ Hz.
- This parameter is guaranteed but not tested.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- t_{LZCE}, t_{LZWE}, t_{LZOE}, t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV typical from steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} and t_{HZOE} is less than t_{LZOE}.
- WE\ is HIGH for READ cycle.
- Device is continuously selected. Chip enable is held in its active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- t_{RC} = Read Cycle Time.
- Chip enable (CE\) and write enable (WE\) can initiate and terminate a WRITE cycle.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

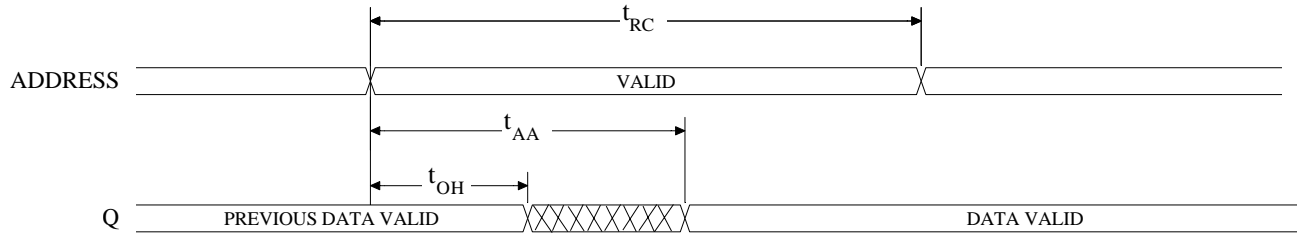
DESCRIPTION	CONDITIONS		SYM	MIN	MAX	UNITS	NOTES
VCC for Retention Data			V _{DR}	2	---	V	
Data Retention Current	CE\ ≥ (V _{CC} - 0.2V) V _{IN} ≥ (V _{CC} - 0.2V) or ≤ 0.2V	V _{CC} = 2V	I _{CCDR}		1	mA	
		V _{CC} = 3V			2	mA	
Chip Deselect to Data Retention Time			t _{CDR}	0	---	ns	4
Operation Recovery Time			t _R	t _{RC}		ns	4, 11

LOW V_{CC} DATA RETENTION WAVEFORM

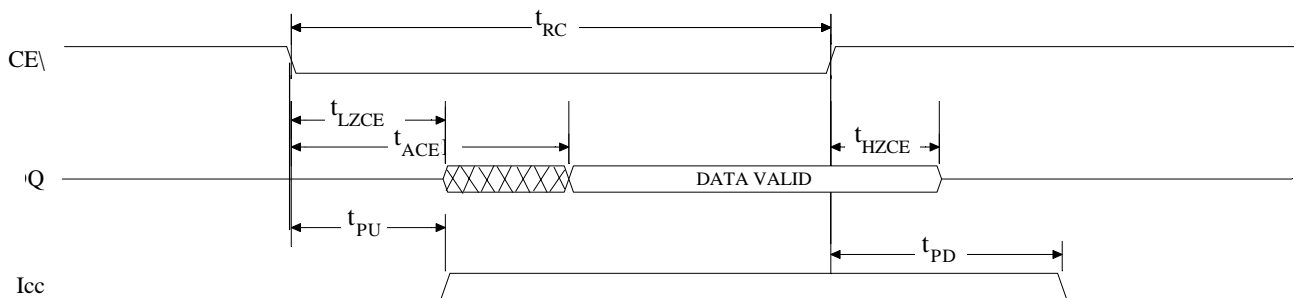




READ CYCLE NO. 1 ^{8,9}

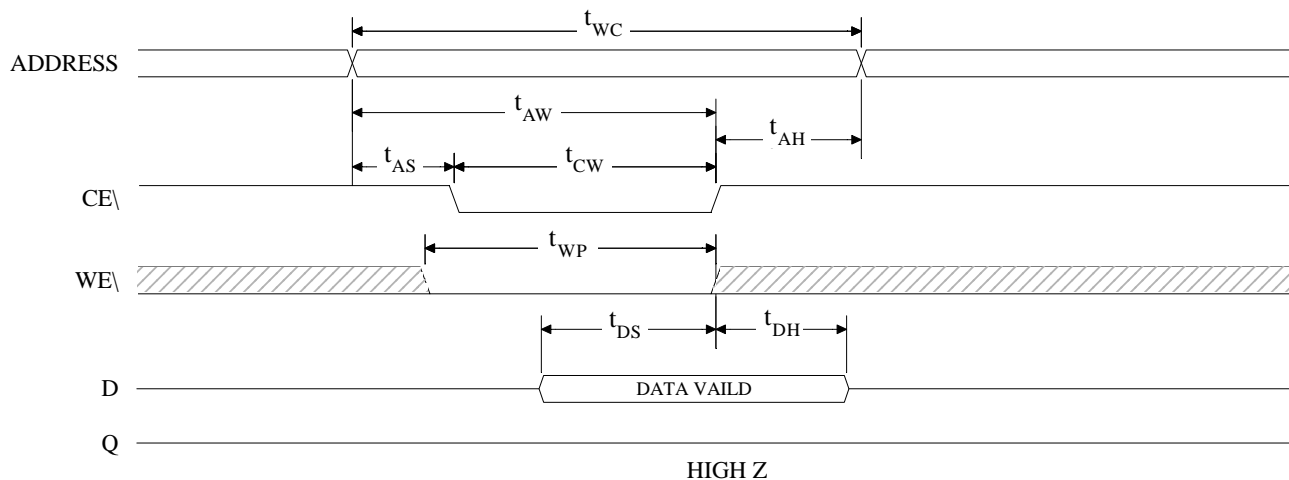


READ CYCLE NO. 2 ^{7, 8, 10}

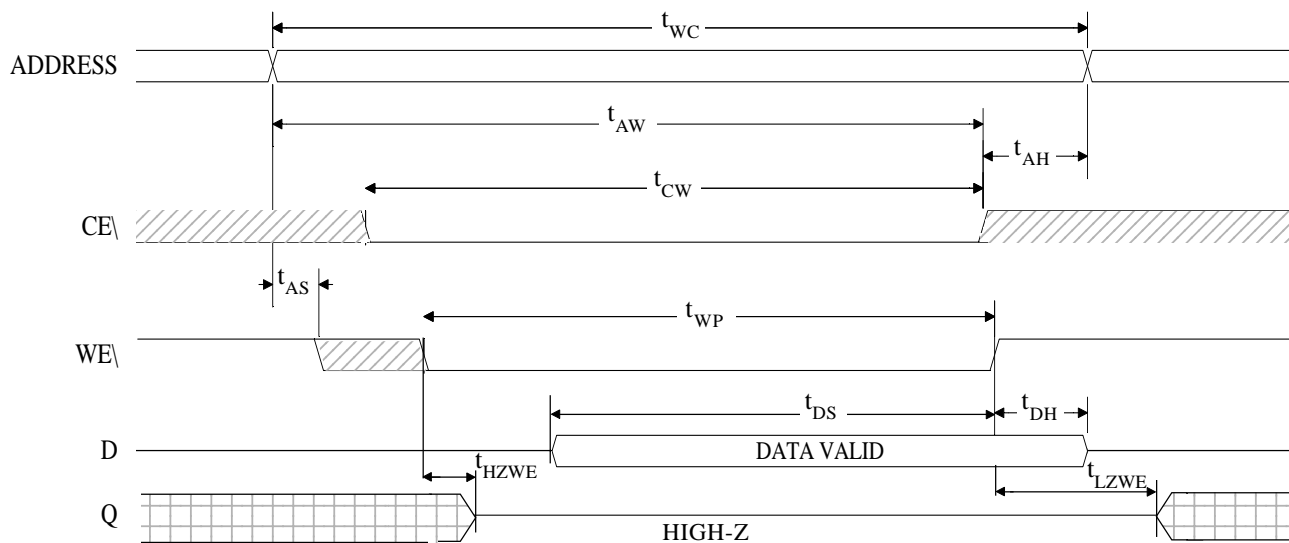




WRITE CYCLE NO. 1 ¹²
(Chip Enabled Controlled)



WRITE CYCLE NO. 2 ^{7,12}
(Write Enabled Controlled)



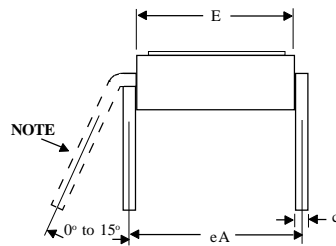
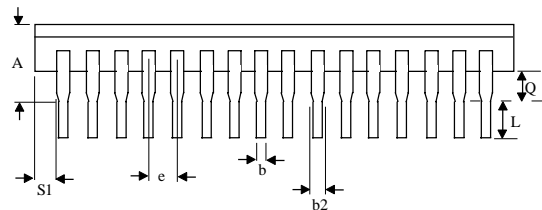
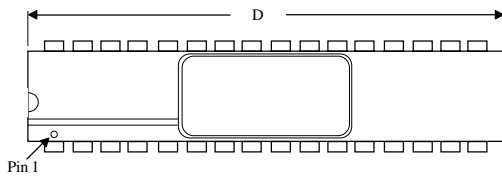
NOTE: Output enable (OE\) is inactive (HIGH).

▨ DON'T CARE
▣ UNDEFINED



MECHANICAL DEFINITIONS*

**ASI Case #106 (Package Designator C)
SMD #5962-88681, Case Outline L**



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	---	0.200
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	---	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	---

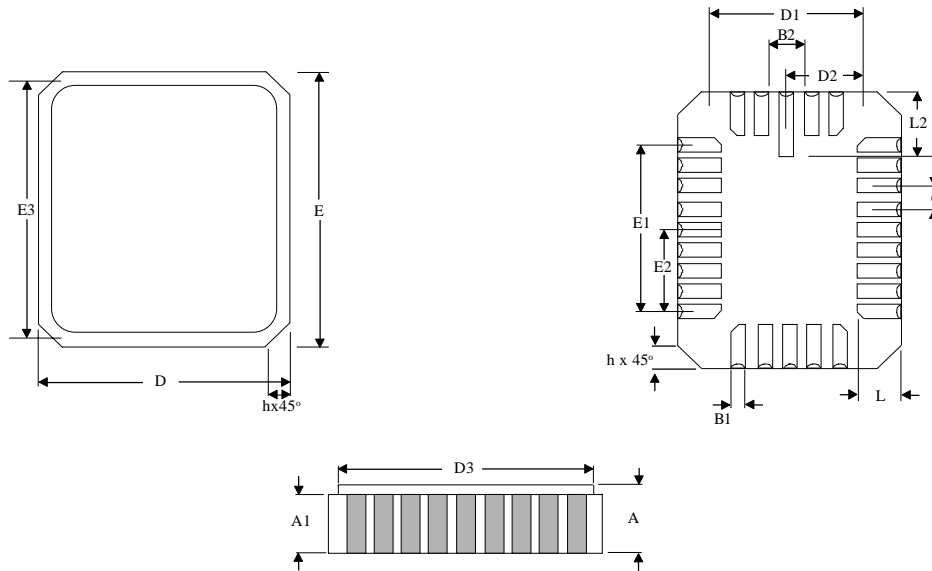
NOTE: These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.

*All measurements are in inches.



MECHANICAL DEFINITIONS*

ASI Case #204 (Package Designator EC)
SMD# 5962-88681, Case Outline X



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.060	0.120
A1	0.050	0.088
B1	0.022	0.028
B2	0.072 REF	
D	0.342	0.358
D1	0.200 BSC	
D2	0.100 BSC	
D3	---	0.358
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	---	0.558
e	0.050 BSC	
h	0.040 REF	
L	0.045	0.055
L2	0.075	0.095

NOTE: These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.

*All measurements are in inches.



ORDERING INFORMATION

EXAMPLE: MT5C2564C-20L/IT

Device Number	Package Type	Speed ns	Options**	Process
MT5C2564	C	-15	L	/*
MT5C2564	C	-20	L	/*
MT5C2564	C	-25	L	/*
MT5C2564	C	-35	L	/*
MT5C2564	C	-40	L	/*
MT5C2564	C	-55	L	/*
MT5C2564	C	-70	L	/*

EXAMPLE: MT5C2564EC-45/XT

Device Number	Package Type	Speed ns	Options**	Process
MT5C2564	EC	-15	L	/*
MT5C2564	EC	-20	L	/*
MT5C2564	EC	-25	L	/*
MT5C2564	EC	-35	L	/*
MT5C2564	EC	-40	L	/*
MT5C2564	EC	-55	L	/*
MT5C2564	EC	-70	L	/*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range
 XT = Extended Temperature Range
 883C = Full Military Processing

-40°C to +85°C
 -55°C to +125°C
 -55°C to +125°C

** OPTIONS

L = 2V Data Retention/Low Power



**ASI TO DSCC PART NUMBER
CROSS REFERENCE***

ASI Package Designator C

ASI Package Designator EC

ASI Part #	SMD Part #	ASI Part #	SMD Part #
MT5C2564C-20/883C	5962-8868106LA	MT5C2564EC-20/883C	5962-8868106XA
MT5C2564C-25/883C	5962-8868105LA	MT5C2564EC-25/883C	5962-8868105XA
MT5C2564C-35/883C	5962-8868101LA	MT5C2564EC-35/883C	5962-8868101XA
MT5C2564C-45/883C	5962-8868102LA	MT5C2564EC-45/883C	5962-8868102XA
MT5C2564C-55/883C	5962-8868103LA	MT5C2564EC-55/883C	5962-8868103XA
MT5C2564C-70/883C	5962-8868104LA	MT5C2564EC-70/883C	5962-8868104XA

* ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.