

ACS573MS

Radiation Hardened Octal Three-State Transparent Latch

January 1996

Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96724 and Intersil's QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Single Event Upset (SEU) Immunity: <1 x 10⁻¹⁰ Errors/Bit/Day
- Dose Rate Upset>10¹¹ RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability.....>10¹² RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range 4.5V to 5.5V
- · Input Logic Levels
 - VIL = 30% of VCC Max
 - VIH = 70% of VCC Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay 17ns (Max), 12ns (Typ)

Description

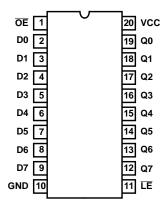
The Intersil ACS573MS is a Radiation Hardened Octal Transparent Latch with an active low output enable. The outputs are transparent to the inputs when the latch enable (LE) is High. When the latch goes low the data is latched. The output enable controls the three-state outputs. When the output enable pins (\overline{OE}) are high the output is in a high impedance state. The latch operation is independent of the state of output enable.

The ACS573MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic family.

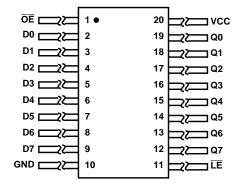
The ACS573MS is supplied in a 20 lead Ceramic Flatpack (K suffix) or a

Pinouts

20 LEAD CERAMIC DUAL-IN-LINE MIL-STD-1835 DESIGNATOR. CDIP2-T20, LEAD FINISH C **TOP VIEW**



20 LEAD CERAMIC FLATPACK MIL-STD-1835 DESIGNATOR, CDFP4-F20, LEAD FINISH C **TOP VIEW**



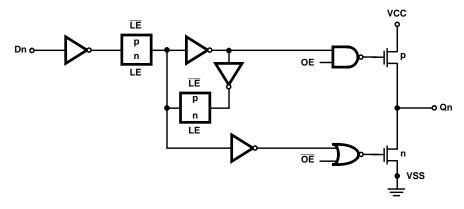
Ordering Information

| PART NUMBER | TEMPERATURE RANGE | SCREENING LEVEL | PACKAGE |
|-----------------|-------------------|-----------------------|--------------------------|
| 5962F9672401VRC | -55°C to +125°C | MIL-PRF-38535 Class V | 20 Lead SBDIP |
| 5962F9672401VXC | -55°C to +125°C | MIL-PRF-38535 Class V | 20 Lead Ceramic Flatpack |
| ACS573D/Sample | 25°C | Sample | 20 Lead SBDIP |
| ACS573K/Sample | 25°C | Sample | 20 Lead Ceramic Flatpack |
| ACS573HMSR | 25°C | Die | Die |

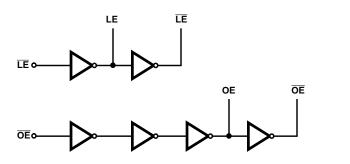
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Functional Diagram

1 OF 8 IDENTICAL CIRCUITS



COMMON CONTROLS



TRUTH TABLE

| ŌĒ | ΙΕ | DATA | OUTPUT |
|----|----|------|--------|
| L | н | Н | Н |
| L | Н | L | L |
| L | L | I | L |
| L | L | h | Н |
| Н | Х | Х | Z |

NOTE: L = Low Logic Level, H = High Logic Level, X = Don't Care, Z = High Impedance, I = Low Voltage Level Prior to High-to-Low Latch Enable Transition, h = High Voltage Level Prior to High-to-Low Latch Enable Transition.

ACS573MS

Die Characteristics

DIE DIMENSIONS:

102 mils x 102 mils 2,600mm x 2,600mm

METALLIZATION:

Type: AISi

Metal 1 Thickness: 7.125kÅ ±1.125kÅ Metal 2 Thickness: 9kÅ ±1kÅ

GLASSIVATION:

Type: SiO₂

Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

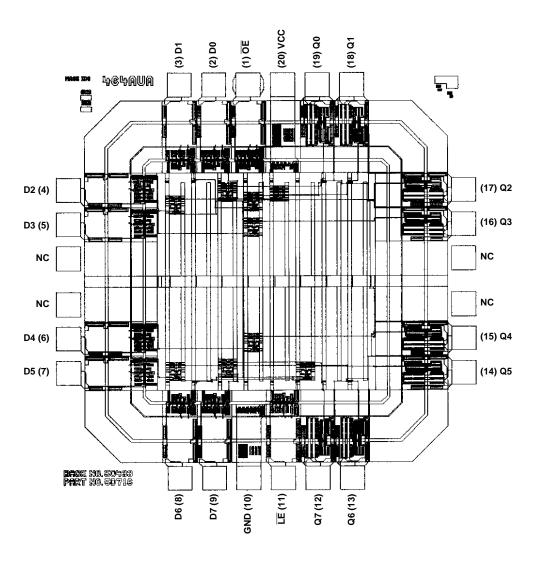
 $<2.0 \times 10^5 \text{ A/cm}^2$

BOND PAD SIZE:

> 4.3 mils x 4.3 mils $> 110\mu m$ x $110\mu m$

Metallization Mask Layout

ACS573MS



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