Data Sheet | August 2000 | File Number 3041.3

Radiation Hardened 8-Bit Input/Output Port

The Intersil HS-82C12RH is a radiation hardened 8-bit input/output port designed for use with the HS-80C85RH radiation hardened microprocessor. It is manufactured using a self-aligned, junction-isolated EPI-CMOS process and features three-state output buffers and device selection and control logic. A service request flip-flop is included for the generation and control of interrupts to the microprocessor. The device can be used in implement many of the peripheral and input/output functions of a microcomputer system. The HS-82C12RH is pinout- and function- compatible with industry-standard 8212 devices.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95818. A "hot-link" is provided on our homepage for downloading. www.intersil.com/spacedefense/space.asp

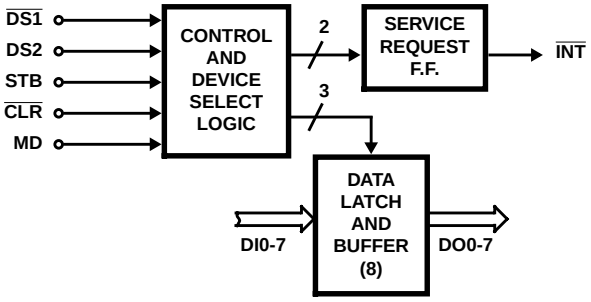
Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^{o}C)
5962R9581801QJC	HS1-82C12RH-8	-55 to 125
5962R9581801QXC	HS9-82C12RH-8	-55 to 125
5962R9581801V9A	HS0-82C12RH-Q	25
5962R9581801VJC	HS1-82C12RH-Q	-55 to 125
5962R9581801VXC	HS9-82C12RH-Q	-55 to 125

Features

- Electrically Screened to SMD # 5962-95818
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Performance
  - Hardened EPI-CMOS Process
  - Total Dose . . . . . 100 krad(Si) (Max)
  - Transient Upset . . . . . > 1 x 10^{8} rad(Si)/s
  - Latch-Up Immune
- Low Power Dissipation
- High Noise Immunity
- Single Power Supply . . . . . +5V
- Low Input Load Current
- 8-Bit Data Register and Buffer
- Asynchronous Register Clear
- Service Request Flip-Flop for Interrupt Generation
- Three-State Outputs
- Bus-Compatible with HS-80C85RH CPU
- Electrically Equivalent to Sandia SA3026
- Military Temperature Range . . . . . -55^{o}C to 125^{o}C

Functional Diagram

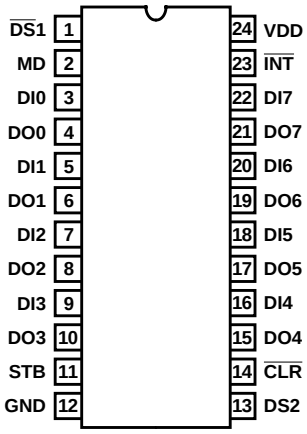


Pin Description

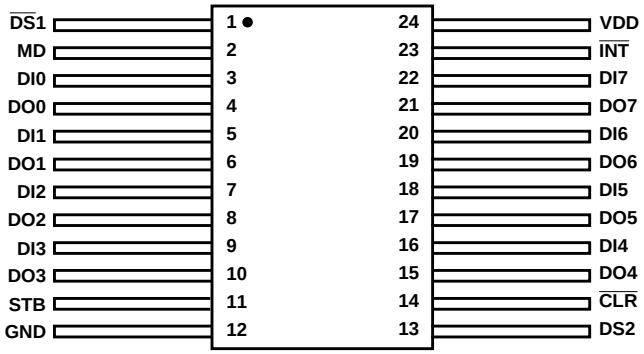
PIN	DESCRIPTION
DI0-DI7	Data In
DO0-DO7	Data Out
$\overline{DS1}$, DS2	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt
$\overline{CLR}$	Clear

Pinouts

24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T24
TOP VIEW



24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835 CDFP4-F24
TOP VIEW



Timing Waveforms

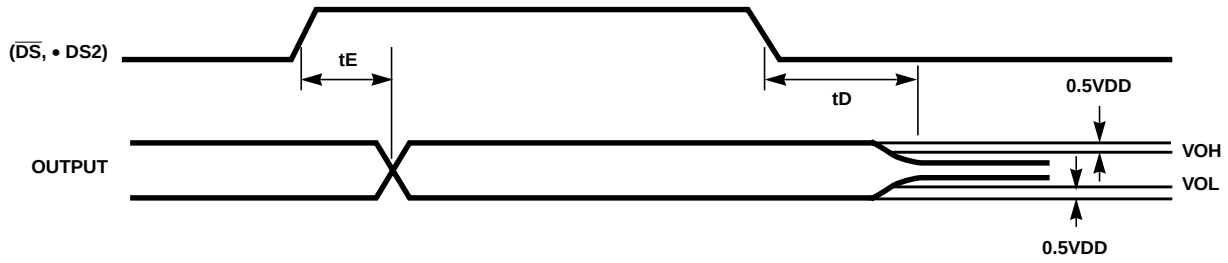


FIGURE 1. READ TIMING

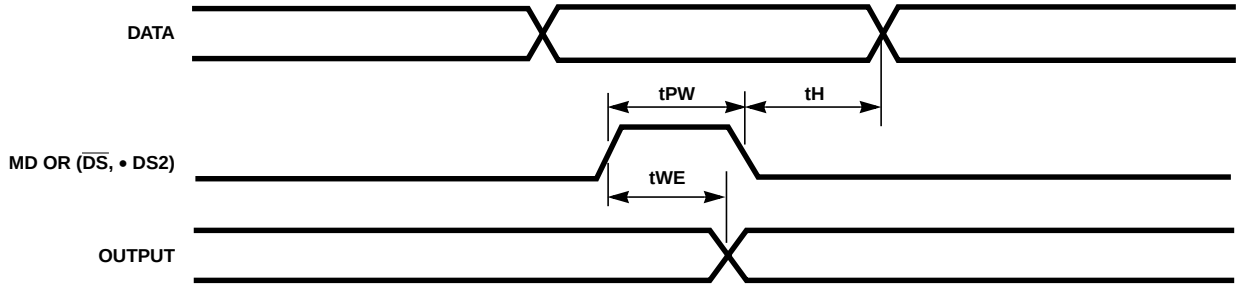


FIGURE 2. WRITE TIMING

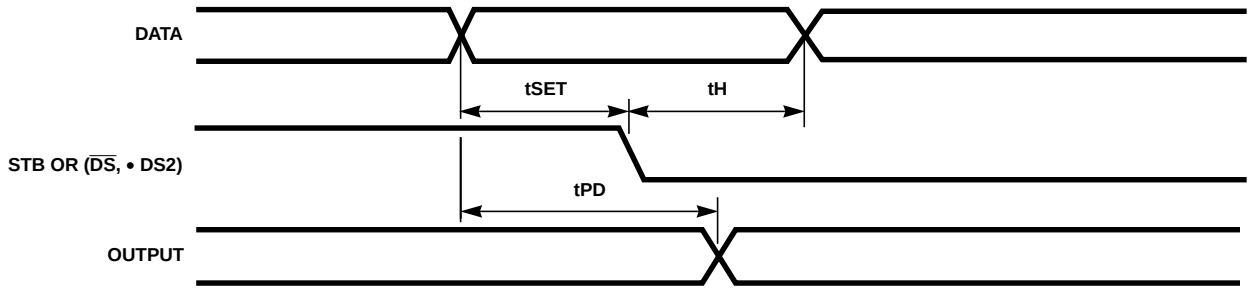


FIGURE 3. DATA SETUP, HOLD, PROPAGATION DELAY TIMING

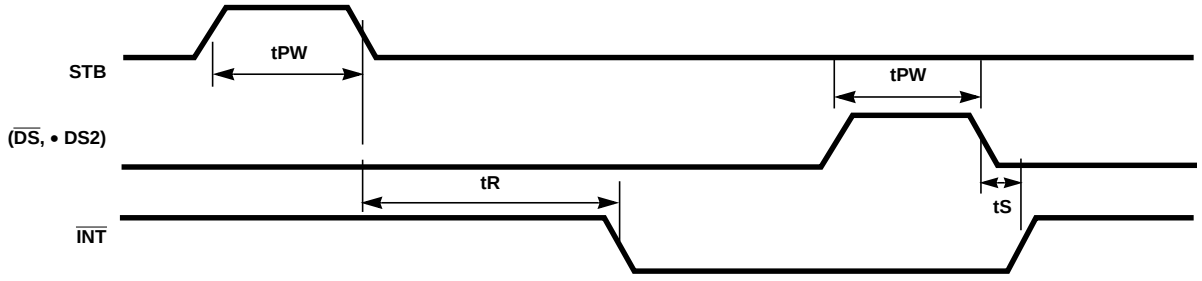


FIGURE 4. INTERRUPT TIMING

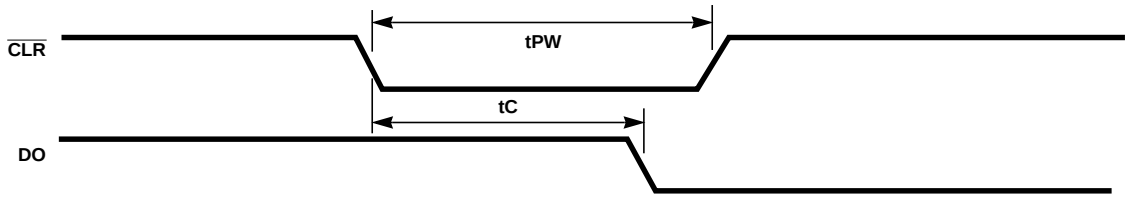


FIGURE 5. CLEAR TIMING

Functional Description

Data Latch

The data latch is comprised of eight “D” type flip-flops. The output of each flip-flop will follow the corresponding data input (DI0 - DI7) when the clock (C) is high. The clock input is level sensitive and the data becomes latched when the clock returns low.

An asynchronous reset ($\overline{CLR}$) is used to clear the latched data. Since the clock (C) overrides the reset ($\overline{CLR}$), the data must be in the latched state in order to clear the flip-flops. If the data is not latched (i.e. clock is high) when $\overline{CLR}$ goes low, then the Q outputs of the data latch will continue to follow the data input, overriding the reset signal.

Output Buffer

Three-state buffers are used to provide output drive for the data latch. A high level on the “output buffer enable” control line enables the buffer outputs. When “output buffer enable” is low the buffer outputs are forced to the high-impedance state.

Device Select Logic

The inputs $\overline{DS}1$ and DS2 are used for device selection. When $\overline{DS}1$ is low and DS2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously cleared when the device is selected.

Mode

the mode input (MD) is used to control the state of the output buffer and to determine the source of the data latch clock (C). When MD is high, the output buffers are enabled and the source of the data latch clock (C) is the device select logic ($\overline{DS}1 \bullet DS2$).

When MD is low, the state of the output buffer is controlled by the device select logic ($\overline{DS}1 \bullet DS2$) and the source of the data latch clock is the strobe (STB) input.

Strobe

The strobe input (STB) is used as the data latch clock (C) when the mode input (MD) is low. The service request flip-flop is synchronously set on the negative going edge of STB.

Service Request Flip-Flop

The service request flip-flop is to generate interrupts to microcomputer systems. It is negative edge triggered and asynchronously cleared (reset).

The output of the service request flip-flop is AND-gated with the device select logic ($\overline{DS}1 \bullet DS2$). The output of the AND gate is the active low interrupt ($\overline{INT}$) signal.

Logic Diagram

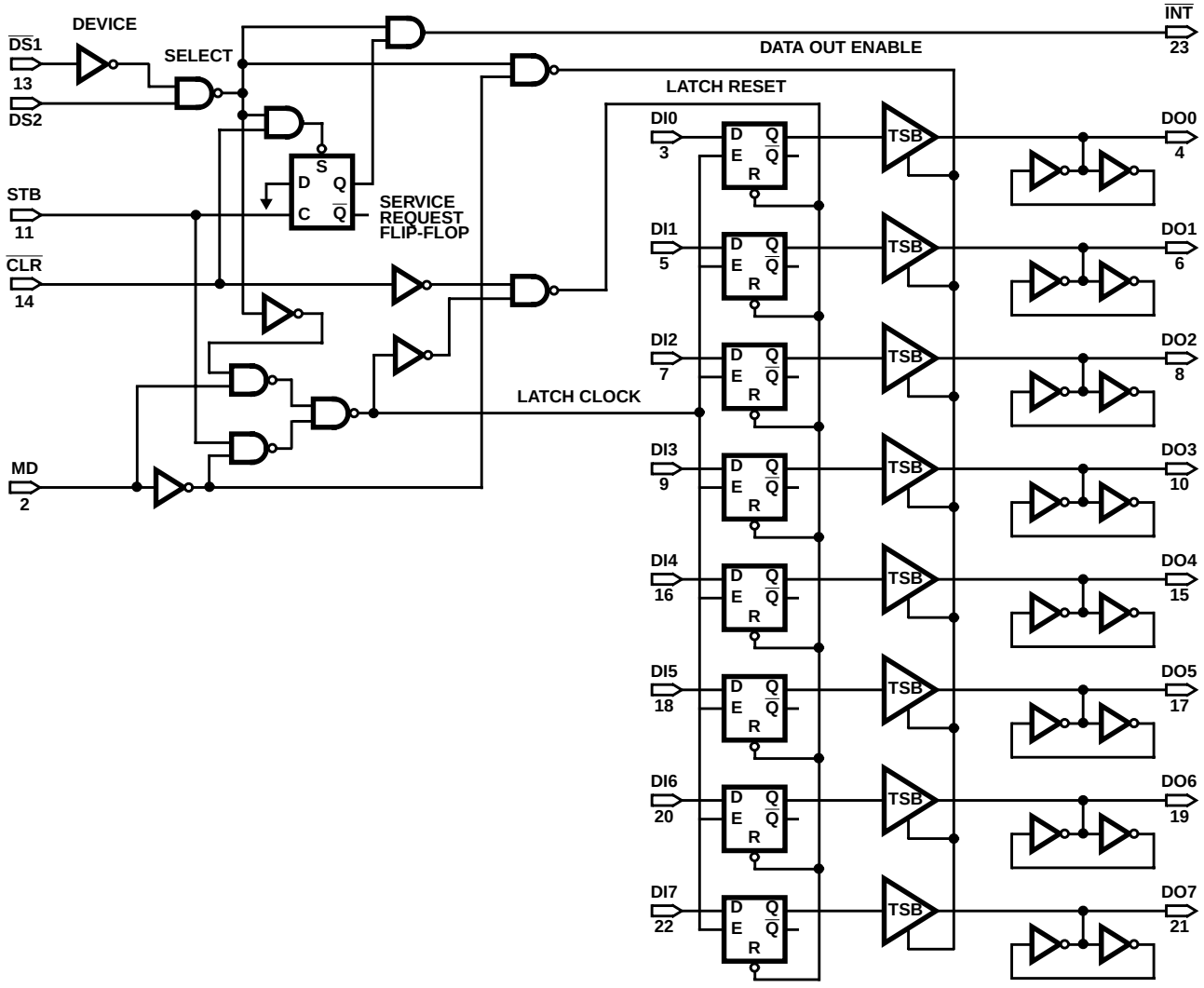


TABLE 1. DATA OUT

STB	MD	$\overline{DS1} \bullet DS2$	DATA OUT EQUALS
0	0	0	High Z State
1	0	0	High Z State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

$\overline{TABLE\ 2.\ INT}$

$\overline{CLR}$	$\overline{DS1} \bullet DS2$	STB	(NOTE) Q	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌐	1	0
1	1 RESET	0	0	0
1	0	0	0	1

NOTE: Internal Service Request Flip-Flop

Die Characteristics

DIE DIMENSIONS:

90 mils x 76 mils x 14 mils ±1 mil

INTERFACE MATERIALS:

Glassivation:

Type: SiO2
Thickness: 8kÅ ±1kÅ

Top Metallization:

Type: AlSi
Thickness: 11kÅ ±2kÅ

Substrate:

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish:

Silicon

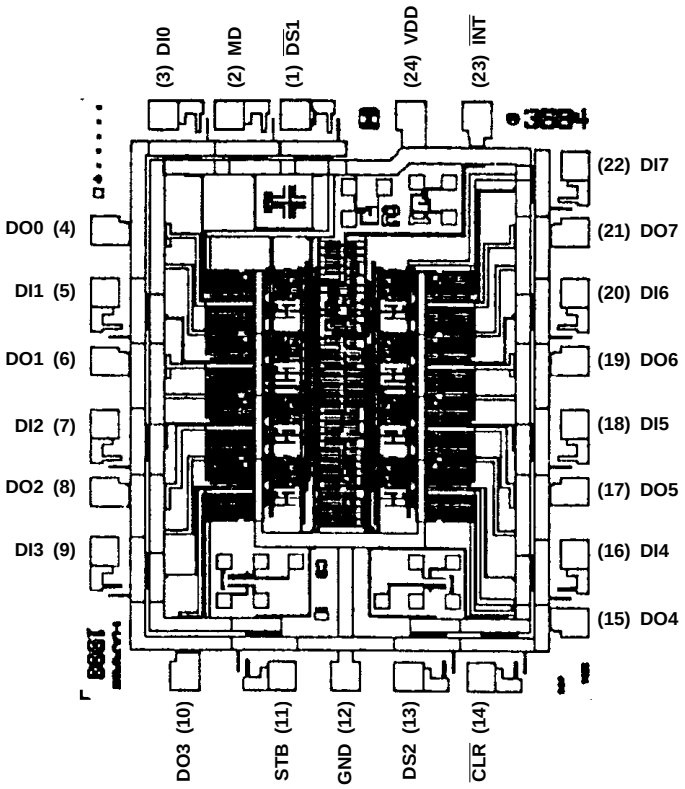
ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

Metallization Mask Layout

HS-82C12RH



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