

$V_{DSM}$	=	4200 V
$I_{TAVM}$	=	3960 A
$I_{TRMS}$	=	6230 A
$I_{TSM}$	=	60000 A
$V_{T0}$	=	0.95 V
$r_T$	=	0.13 m $\Omega$

## Phase Control Thyristor

# 5STP 38N4200

Doc. No. 5SYA1012-03 Jan. 02

- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate

### Blocking

Maximum rated values <sup>1)</sup>

Symbol	Conditions	5STP 38N4200	5STP 38N4000	5STP 38N3600
$V_{DRM}, V_{RRM}$	f = 50 Hz, $t_p = 10ms$	4200 V	4000 V	3600 V
$V_{RSM1}$	$t_p = 5ms$ , single pulse	4600 V	4400 V	4000 V
$dV/dt_{crit}$	Exp. to $0.67 \times V_{DRM}$ , $T_j = 125^\circ C$	2000 V/ $\mu s$		

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	$I_{DRM}$	$V_{DRM}$ , $T_j = 125^\circ C$			400	mA
Reverse leakage current	$I_{RRM}$	$V_{RRM}$ , $T_j = 125^\circ C$			400	mA

### Mechanical data

Maximum rated values <sup>1)</sup>

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	$F_M$		81	90	108	kN
Acceleration	a	Device unclamped			50	m/s <sup>2</sup>
Acceleration	a	Device clamped			100	m/s <sup>2</sup>

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m			2.9		kg
Surface creepage distance	$D_s$		56			mm
Air strike distance	$D_a$		22			mm

<sup>1)</sup> Maximum Ratings are those values beyond which damage to the device may occur

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**On-state***Maximum rated values <sup>1)</sup>*

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. average on-state current	$I_{TAVM}$	Half sine wave, $T_c = 70^\circ\text{C}$			3960	A
RMS on-state current	$I_{TRMS}$				6230	A
Max. peak non-repetitive surge current	$I_{TSM}$	$t_p = 10\text{ ms}$ , $T_j = 125^\circ\text{C}$ , $V_D = V_R = 0\text{ V}$			60000	A
Limiting load integral	$I^2t$				18000	$\text{kA}^2\text{s}$
Max. peak non-repetitive surge current	$I_{TSM}$	$t_p = 8.3\text{ ms}$ , $T_j = 125^\circ\text{C}$ , $V_D = V_R = 0\text{ V}$			65000	A
Limiting load integral	$I^2t$				17500	$\text{kA}^2\text{s}$

**Characteristic values**

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	$V_T$	$I_T = 3000\text{ A}$ , $T_j = 125^\circ\text{C}$			1.35	V
Threshold voltage	$V_{T0}$	$I_T = 2500\text{ A} - 7500\text{ A}$ , $T_j = 125^\circ\text{C}$			0.95	V
Slope resistance	$r_T$	$T_j = 125^\circ\text{C}$			0.13	$\text{m}\Omega$
Holding current	$I_H$	$T_j = 25^\circ\text{C}$			100	mA
		$T_j = 125^\circ\text{C}$			75	mA
Latching current	$I_L$	$T_j = 25^\circ\text{C}$			500	mA
		$T_j = 125^\circ\text{C}$			350	mA

**Switching***Maximum rated values <sup>1)</sup>*

Parameter	Symbol	Conditions	min	typ	max	Unit
Critical rate of rise of on-state current	$di/dt_{crit}$	$T_j = 125^\circ\text{C}$ , $I_{TRM} = 5000\text{ A}$ , $V_D \leq 0.67 \cdot V_{DRM}$ , $I_{FG} = 2\text{ A}$ , $t_r = 0.5\ \mu\text{s}$			250	$\text{A}/\mu\text{s}$
Critical rate of rise of on-state current	$di/dt_{crit}$		Cont. $f = 50\text{ Hz}$			1000
Circuit-commutated turn-off time	$t_q$	$T_j = 125^\circ\text{C}$ , $I_{TRM} = 5000\text{ A}$ , $V_R = 200\text{ V}$ , $di_T/dt = -5\text{ A}/\mu\text{s}$ , $V_D \leq 0.67 \cdot V_{DRM}$ , $dv_D/dt = 20\text{ V}/\mu\text{s}$ ,	600			$\mu\text{s}$

**Characteristic values**

Parameter	Symbol	Conditions	min	typ	max	Unit
Recovery charge	$Q_{rr}$	$T_j = 125^\circ\text{C}$ , $I_{TRM} = 5000\text{ A}$ , $V_R = 200\text{ V}$ , $di_T/dt = -5\text{ A}/\mu\text{s}$	5000		10000	$\mu\text{As}$
Delay time	$t_d$	$V_D = 0.4 \cdot V_{DRM}$ , $I_{FG} = 2\text{ A}$ , $t_r = 0.5\ \mu\text{s}$			3	$\mu\text{s}$

## Triggering

Maximum rated values <sup>1)</sup>

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V <sub>FGM</sub>				12	V
Peak forward gate current	I <sub>FGM</sub>				10	A
Peak reverse gate voltage	V <sub>RGM</sub>				10	V
Gate power loss	P <sub>G</sub>	For DC gate current			3	W
Average gate power loss	P <sub>GAV</sub>		see Fig. 9			

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate trigger voltage	V <sub>GT</sub>	T <sub>j</sub> = 25°C			2.6	V
Gate trigger current	I <sub>GT</sub>	T <sub>j</sub> = 25°C			400	mA
Gate non-trigger voltage	V <sub>GD</sub>	V <sub>D</sub> = 0.4 x V <sub>DRM</sub> , T <sub>vjmax</sub> = 125°C	0.3			V
Gate non-trigger current	I <sub>GD</sub>	V <sub>D</sub> = 0.4 x V <sub>DRM</sub> , T <sub>vjmax</sub> = 125°C	10			mA

## Thermal

Maximum rated values <sup>1)</sup>

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T <sub>j</sub>				125	°C
Storage temperature range	T <sub>stg</sub>		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	R <sub>th(j-c)</sub>	Double side cooled			5.7	K/kW
	R <sub>th(j-c)A</sub>	Anode side cooled			11.4	K/kW
	R <sub>th(j-c)C</sub>	Cathode side cooled			11.4	K/kW
Thermal resistance case to heatsink	R <sub>th(c-h)</sub>	Double side cooled			1	K/kW
	R <sub>th(c-h)</sub>	Single side cooled			2	K/kW

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^n R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
R <sub>i</sub> (K/kW)	3.4	1.26	0.68	0.35
τ <sub>i</sub> (s)	0.8685	0.1572	0.0219	0.0078

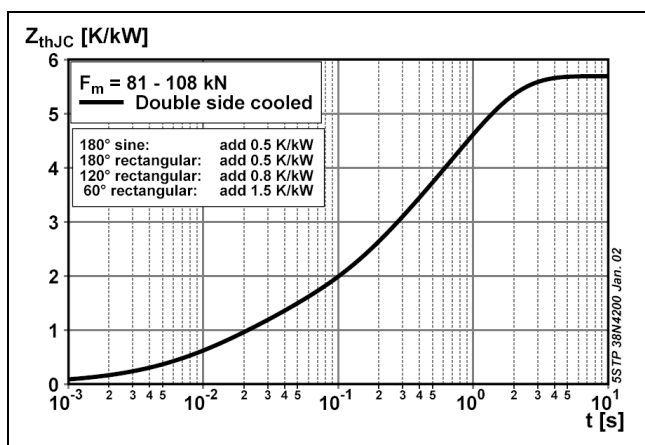
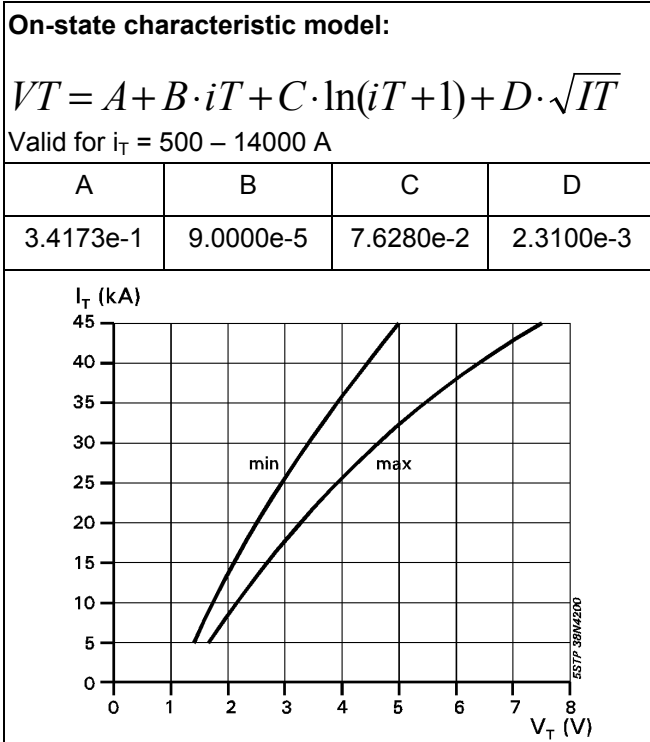
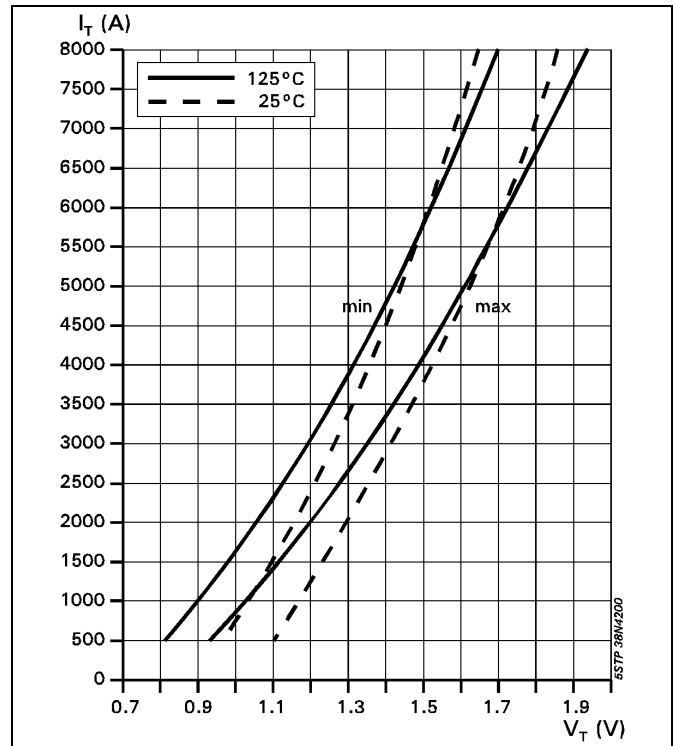


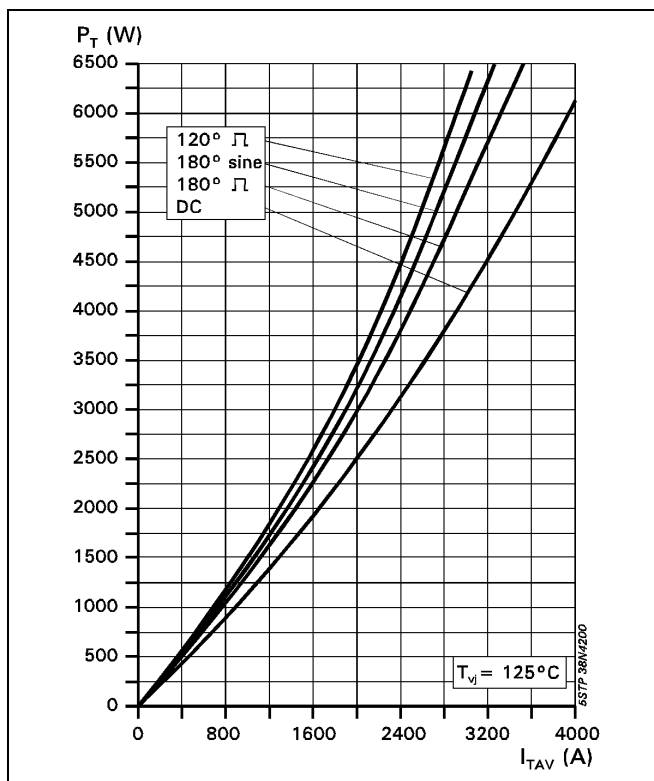
Fig. 1 Transient thermal impedance junction-to case.



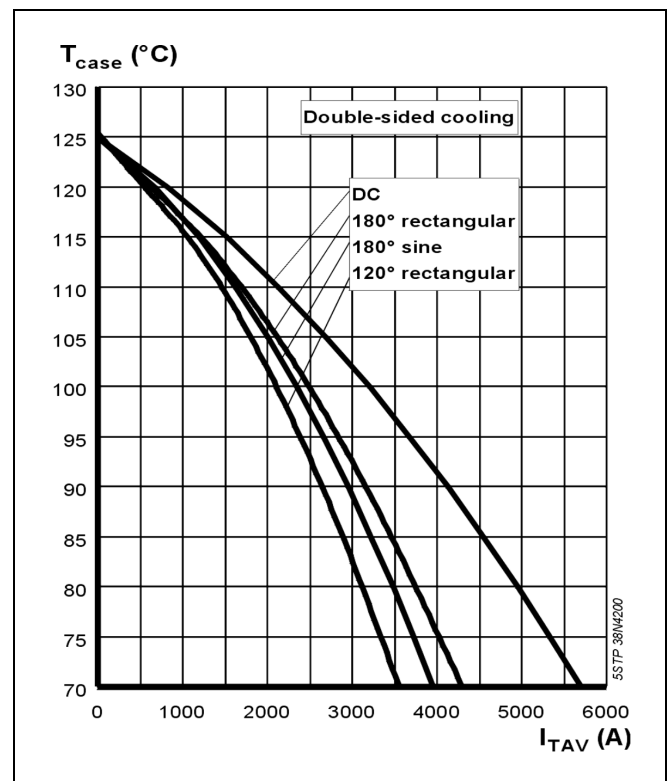
**Fig. 2** On-state characteristics.  
 $T_j = 125^\circ\text{C}$ , 10ms half sine



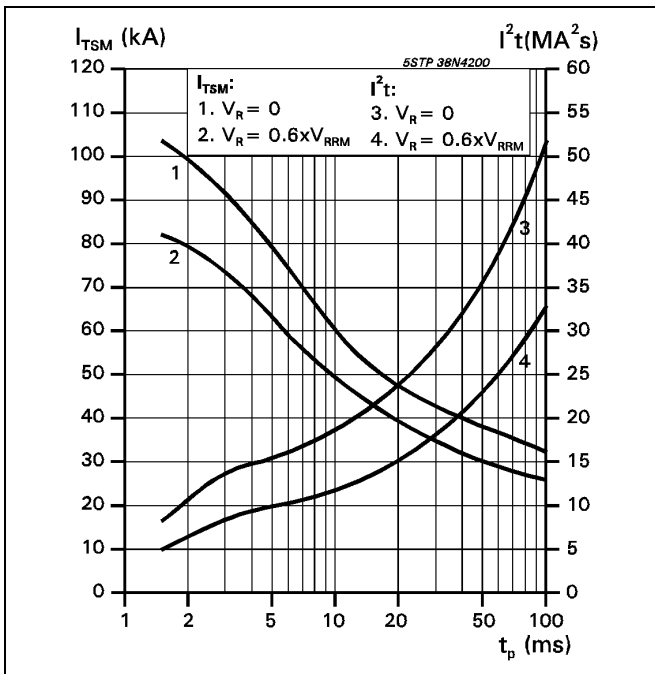
**Fig. 3** On-state characteristics.



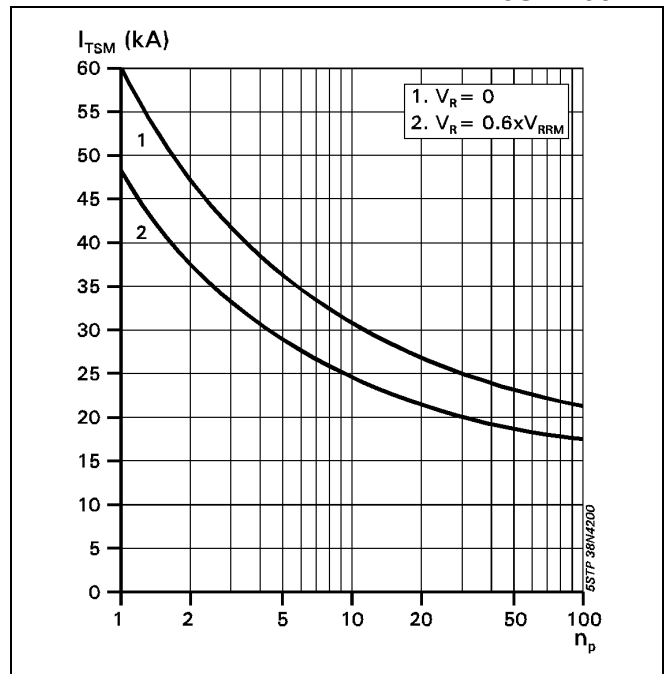
**Fig. 4** On-state power dissipation vs. mean on-state current. Turn - on losses excluded.



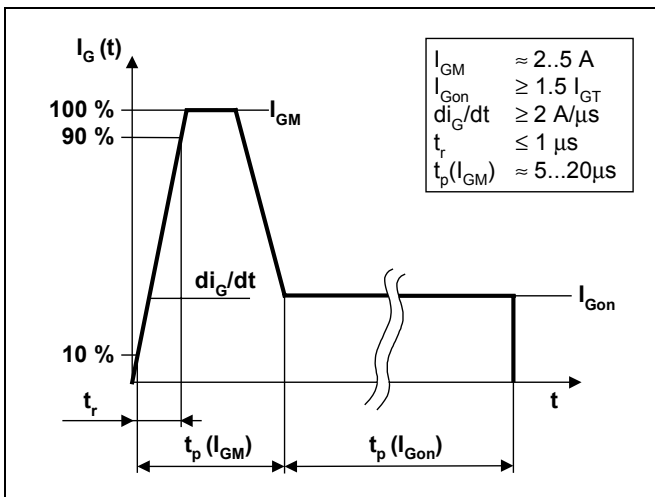
**Fig. 5** Max. permissible case temperature vs. mean on-state current.



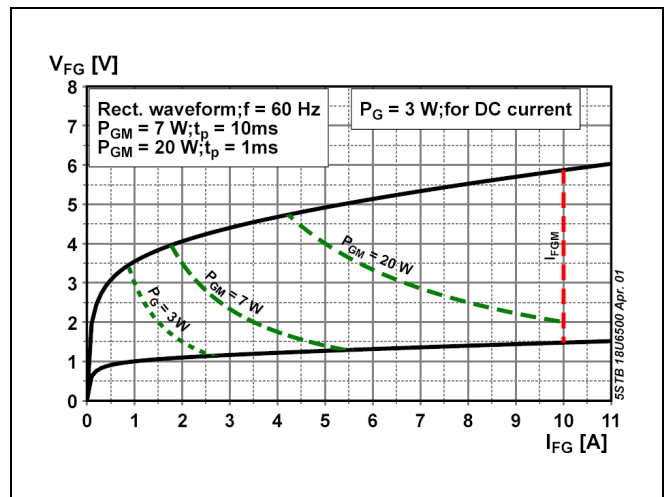
**Fig. 6** Surge on-state current vs. pulse length. Half-sine wave.



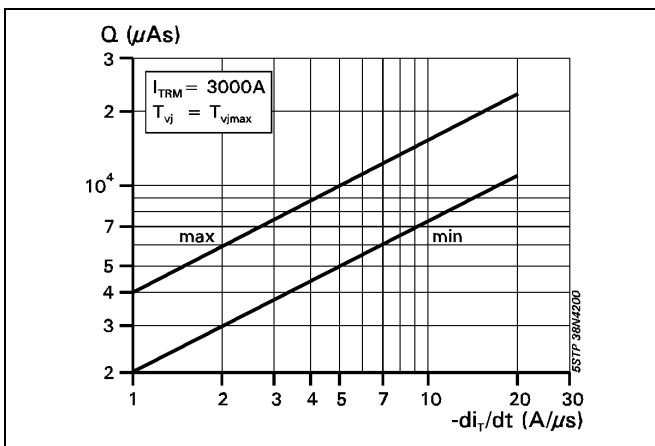
**Fig. 7** Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.



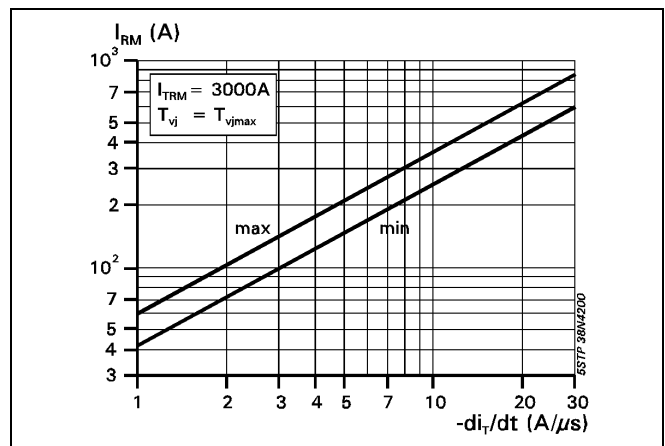
**Fig. 8** Recommended gate current waveform.



**Fig. 9** Max. peak gate power loss.



**Fig. 10** Recovery charge vs. decay rate of on-state current.



**Fig. 11** Peak reverse recovery current vs. decay rate of on-state current.

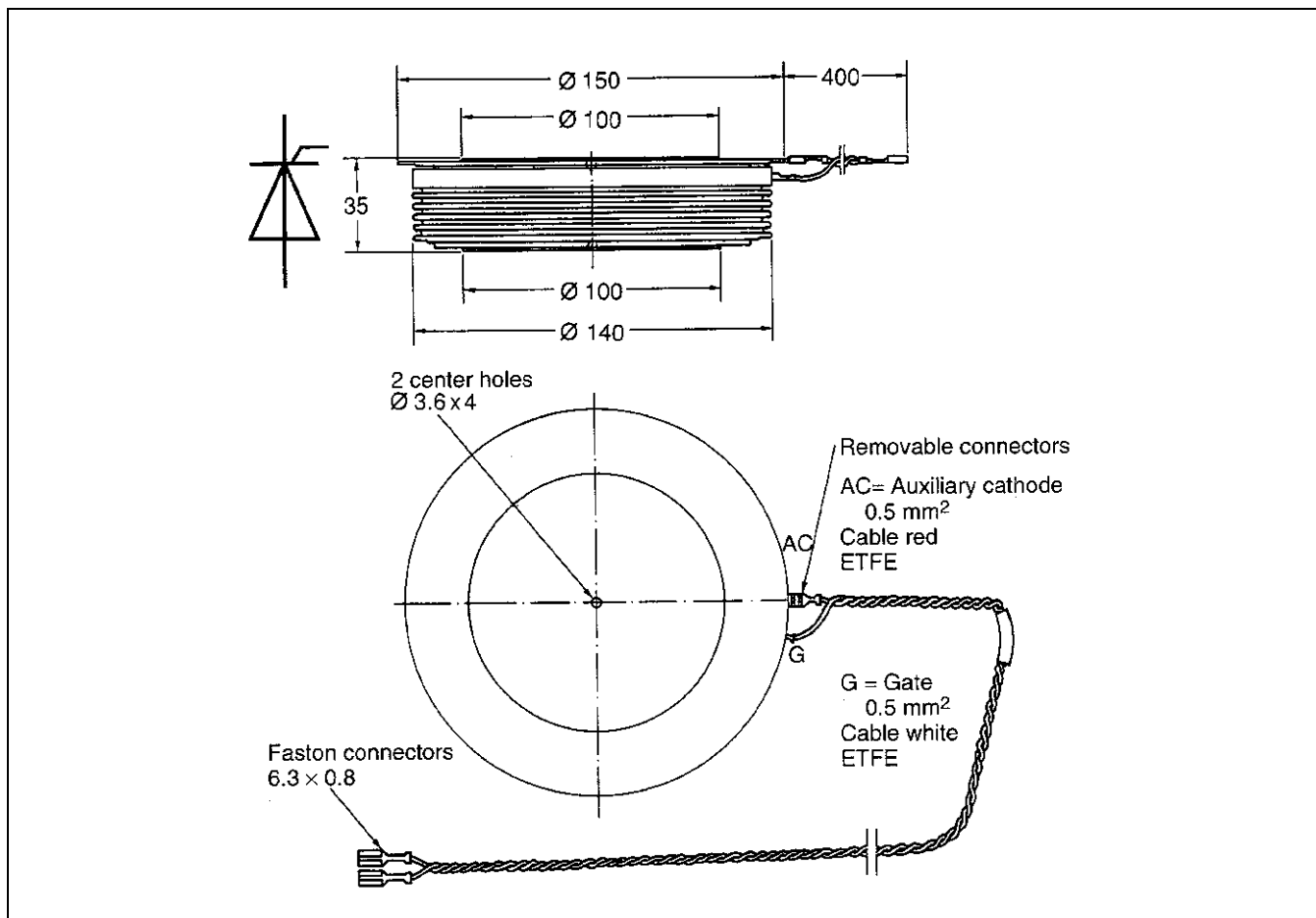


Fig. 12 Device Outline Drawing.

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