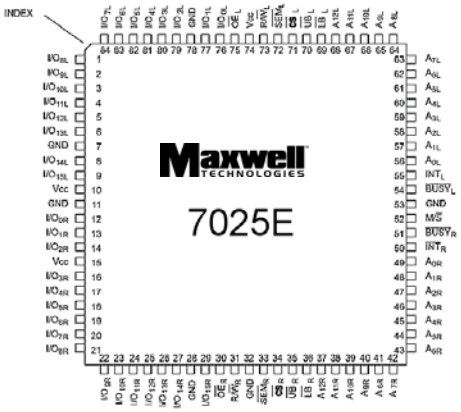
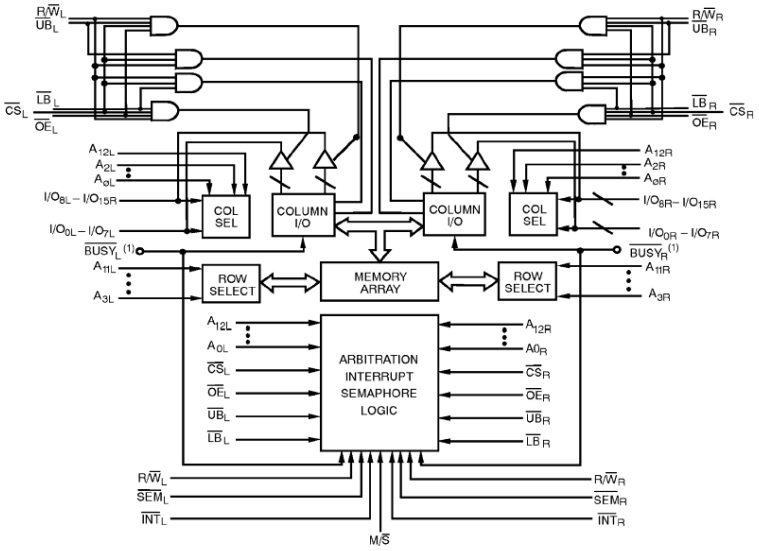
7025E
(8K x 16-Bit) Dual Port RAM
High-Speed CMOS





Logic Diagram

FEATURES:

- 8K x 16-bit dual port RAM
  - Stand Alone
  - Master Slave
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Excellent Single Event Effects:
  -SEL_{TH} LET = >100 MeV/mg/cm^2
  -SEU_{TH} LET = 7 MeV/mg/cm^2
- Package:
  -84 Pin RAD-PAK® quad flat pack
- Separate upper byte and lower byte control for multiplexed bus compatibility
- High speed access time: 35/45 ns
- Expandable to 32 bits or more using master/slave select when cascading
- High speed CMOS technology
  -TTL compatible, single 5V power supply
  -Interrupt flag for port-to-port communication
  -On chip port arbitration logic
  -Asynchronous operation from either port

DESCRIPTION:

Maxwell Technologies' 7025E Dual Port RAM High Speed CMOS® microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. The 7025E is designed to be used as a stand-alone 128k-bit Dual Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit or more word systems. This design results in full-speed, error-free operation without the need for additional discrete logic. The 7025E provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CS}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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TABLE 1. 7025E PINOUT DESCRIPTION

NAMES	LEFT PORT	RIGHT PORT
Chip Select	$\overline{CS}_L$	$\overline{CS}_R$
Read/Write Select	$\overline{R/W}_L$	$\overline{R/W}_R$
Output Select	$\overline{OS}_L$	$\overline{OS}_R$
Address	AO_L-$A12_L$	AO_R-$A12_R$
Data Input/Output	I/OO_L-$I/O15_L$	I/OO_R-$I/O15_R$
Semaphore Select	$\overline{SEM}_L$	$\overline{SEM}_R$
Upper Byte Select	$\overline{UB}_L$	$\overline{UB}_R$
Lower Byte Select	$\overline{LB}_L$	$\overline{LB}_R$
Interrupt Flag	$\overline{INT}_L$	$\overline{INT}_R$
Busy Flag	$\overline{BUSY}_L$	$\overline{BUSY}_R$
$\overline{M/S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

TABLE 2. 7025E ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage (Relative to V_{SS})	V_{CC}	-0.3	7.0	V
Operating Temperature Range	T_A	-55	125	˚C
Input or Output Voltage Applied	--	GND -0.3V	V_{CC}+ 0.3	V
Storage Temperature Range	T_{STG}	-65	150	˚C

TABLE 3. 7025E RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage Positive	V_{CC}	4.5	5.5	V
Input Voltage	V_{IL} V_{IH}	-0.5 2.2	0.8 6.0	V
Thermal Impedance	Θ_{JC}	--	1.02	°C/W
Operating Temperature Range	T_A	-55	125	˚C

TABLE 4. 7025E CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: V_{IN} = 0V[1]	C_{IN}	--	5	pF
Output Capacitance: V_{OUT} = 0V[1]	C_{OUT}	--	7	pF

1. Guaranteed by design.

TABLE 5. 7025E DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55 TO 125 ˚C UNLESS OTHERWISE)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Leakage Current [1]	I_{LI}	--	±10	µA
Output Leakage Current [2]	I_{LO}	--	±10	µA
Standby Supply Current, Both ports TTL level inputs	I_{CCSB}			mA
-35		--	50	
-45		--	50	
Standby Supply Current, Both ports CMOS level inputs	I_{CCSB1}			µA
-35		--	5000	
-45		--	5000	
Operating Supply Current, Both ports Active	I_{CCOP}			mA
-35		--	320	
-45		--	280	
Operating Supply Current, One Port Active, One Port Standby	I_{CCOP1}			mA
-35		--	190	
-45		--	180	
Input Low Voltage	V_{IL}	--	0.8	V
Input High Voltage	V_{IH}	2.2	--	
Output Low Voltage [3]	V_{OL}	--	0.4	V
Output High Voltage	V_{OH}	2.4	--	

1. VCC = 5.5V, VIN = GND to VCC, CS = VIH, VOUT = 0 to VCC.
2. VIH max = VCC + 0.3V, VIL min = -0.3V or -1V pulse width 50 ns.
3. V_{CC} min, I_{OL} = 4 mA, I_{OH} = -4 mA.

TABLE 6. 7025E AC ELECTRICAL CHARACTERISTICS FOR READ CYCLE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_A = -55 TO 125 ˚C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Read Cycle Time	t_{RC}			ns
-35		35	--	
-45		45	--	

TABLE 6. 7025E AC ELECTRICAL CHARACTERISTICS FOR READ CYCLE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_A = -55 TO 125 ˚C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Address Access Time	t_{AA}			ns
-35		--	35	
-45		--	45	
Chip Select Access Time [1]	t_{ACS}			ns
-35		--	35	
-45		--	45	
Byte Select Access Time [1]	t_{ABE}			ns
-35		--	35	
-45		--	45	
Output Select to Output Valid	t_{AOE}			ns
-35		--	20	
-45		--	25	
Output Low Z Time [2,3]	t_{LZ}			ns
-35		3	--	
-45		3	--	
Output High Z Time [2,3]	t_{HZ}			
-35		--	20	ns
-45		--	20	
Chip Enable to Power Up Time [2]	t_{PU}	0	--	ns
Chip Disable to Power Up Time [2]	t_{PD}	--	50	ns
Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	t_{SOP}	15	--	ns

1. To access RAM, $\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CS}$ = V_{IN} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
2. Guaranteed by design.
3. Transition is measured ± 500 mV from low or high impedance voltage with load.

TABLE 7. 7025E AC ELECTRICAL CHARACTERISTICS FOR WRITE CYCLE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_A = -55 TO 125 ˚C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Write Cycle Time	t_{WC}			ns
-35		35	--	
-45		45	--	
Address Valid to End of Write	t_{AW}			ns
-35		30	--	
-45		40	--	
Chip Select to End of Write [1]	t_{SW}			ns
-35		30	--	
-45		40	--	

TABLE 7. 7025E AC ELECTRICAL CHARACTERISTICS FOR WRITE CYCLE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_A = -55 TO 125 ˚C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Address Setup Time	t_{AS}			ns
-35		0	--	
-45		0	--	
Write Pulse Width	t_{WP}			ns
-35		30	--	
-45		35	--	
Write Recovery Time	t_{WR}			ns
-35		0	--	
-45		0	--	
Data Valid to End of Write	t_{DW}			ns
-35		25	--	
-45		25	--	
Output High Z Time [2,3]	t_{HZ}			ns
-35		--	20	
-45		--	20	
Data Hold Time	t_{DH}			ns
-35		0	--	
-45		0	--	
Write Select to Output in High Z [2,3]	t_{WZ}			ns
-35		--	20	
-45		--	20	
Output Active from End of Write [2,3,4]	t_{OW}			ns
-35		0	--	
-45		0	--	
SEM Flag Write to Read Time	t_{SWRD}			ns
-35		10	--	
-45		10	--	
SEM Flag Contention Window	t_{SPS}			ns
-35		10	--	
-45		10	--	

1. To access RAM, $\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CS}$ = V_{IN} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
2. Guaranteed by design.
3. Transition is measured ± 500 mV from low or high impedance voltage with load.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{DW}.

TABLE 8. 7025E AC ELECTRICAL CHARACTERISTICS FOR WRITE MASTER/SLAVE CONFIGURATION

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_A = -55 TO 125 ˚C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
For Master Only				
BUSY Access Time to Address Match	t_{BAA}			ns
-35		--	35	
-45		--	35	
BUSY Disable Time to Address Not Matched	t_{BDA}			ns
-35		--	30	
-45		--	30	
BUSY Access Time to Chip Select Low	t_{BAC}			ns
-35		--	30	
-45		--	30	
BUSY Disable Time to Chip Select High	t_{BDC}			ns
-35		--	25	
-45		--	25	
Write Pulse to Data Delay [1]	t_{WDD}			ns
-35		--	60	
-45		--	70	
Write Data Valid to Read Data Delay [1]	t_{DDD}			ns
-35		--	45	
-45		--	55	
Arbitration Priority Setup Time [2]	t_{APS}			ns
-35		5	--	
-45		5	--	
BUSY Disable to Valid Data	t_{BDD}			ns
-35		--	[3]	
-45		--	[3]	
For Slave Only				
Write to BUSY Input [4]	t_{WB}	0	--	ns
Write Hold after BUSY [5]	t_{WH}	25	--	ns
Write Pulse to Data Delay [1]	t_{WDD}			ns
-35		--	60	
-45		--	70	
Write Data Valid to Read Data Delay [1]	t_{DDD}			ns
-35		--	45	
-45		--	55	

1. Port to port timing delay through RAM cells from writing port to reading port.
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual) or t_{DDD} - t_{WD} (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.

TABLE 9. 7025E AC PARAMETERS FOR INTERRUPT TIMING

(V_{CC} = 5V ± 10%, T_A = -55 TO 125 ˚C, f = 1 MHz)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Address Setup Time	t_{AS}	0	--	ns
Write Recovery Time	t_{WR}	0	--	ns
Interrupt Set Time -35 -45	t_{INS}	 -- --	 30 35	ns
Interrupt Reset Time -35 -45	t_{INR}	 -- --	 30 35	ns

TABLE 10. 7025E TRUTH TABLE FOR INTERRUPT FLAG CONTROL [1]

FUNCTION	$\overline{R/W}$	$\overline{CS}$	$\overline{OS}$	A_0-A_{12}	$\overline{INT}$
Left Port					
Set right $\overline{INT}_L$ flag	L	L	X	1FFF	X
Reset right $\overline{INT}_L$ flag	X	X	X	X	X
Set left $\overline{INT}_L$ flag	X	X	X	X	L [2]
Reset left $\overline{INT}_L$ flag	X	L	L	1FFE	H [3]
Right Port					
Set right $\overline{INT}_R$ flag	X	X	X	X	L [3]
Reset right $\overline{INT}_R$ flag	X	L	L	1FFF	H [2]
Set left $\overline{INT}_R$ flag	L	L	X	1FFE	X
Reset left $\overline{INT}_R$ flag	X	X	X	X	X

1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_R$ = L, then no change.
3. If $\overline{BUSY}_L$ = L, then no change.

Table 11. 7025E Truth Table for Arbitration Options

Options	Inputs					Outputs	
	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	M/$\overline{S}$	$\overline{SEM}$	$\overline{BUSY}$	$\overline{INT}$
Busy Logic Master	L L	X L	L X	H H	H H	Output Signal	--
Busy Logic Slave	L L	X L	L X	L L	H H	Input Signal	--
Interrupt Logic	L L	X L	L X	X X	H H	--	Output Signal
Semaphore Logic	H H	X X	X X	H L	L L	H HI-Z	--

Table 12. 7025E Non-Contention Read/Write Control

Inputs [1]						Outputs		Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-I/O15	I/O0-I/O7	
H	X	X	X	X	H	HI-Z	HI-Z	Deselected power down
X	X	X	H	H	H	HI-Z	HI-Z	Both bytes deselected: Power down
L	L	X	L	H	H	DATAIN	HI-Z	Write to upper byte only
L	L	X	H	L	H	HI-Z	DATAIN	Write to lower byte only
L	L	X	L	L	H	DATAIN	DATAIN	Write to both bytes
L	H	L	L	H	H	DATAOUT	HI-Z	Read upper byte only
L	H	L	H	L	H	HI-Z	DATAOUT	Read lower byte only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read both bytes
X	X	H	X	X	X	HI-Z	HI-Z	Outputs disabled

1. AO_L - $A12_L$ ¼ AO_R-$A12_R$.

TABLE 13. 7025E SEMAPHORE READ/WRITE CONTROL [1]

INPUTS						OUTPUTS		MODE
$\overline{CS}$	$\overline{R/W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-I/O15	I/O0-I/O7	
H	H	L	X	X	L	DATAOUT	DATAOUT	Read data in semaphore flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read data in semaphore flag
H		X	X	X	L	DATAIN	DATAIN	Write DinO into semaphore flagf
X		X	H	H	L	DATAIN	DATAIN	Write DinO into semaphore flag
L	X	X	L	X	L	--	--	Not allowed
L	X	X	X	L	L	--	--	Not allowed

1. AO_L - $A12_L$ ¼ AO_R-$A12_R$.

FIGURE 1. TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2,3]

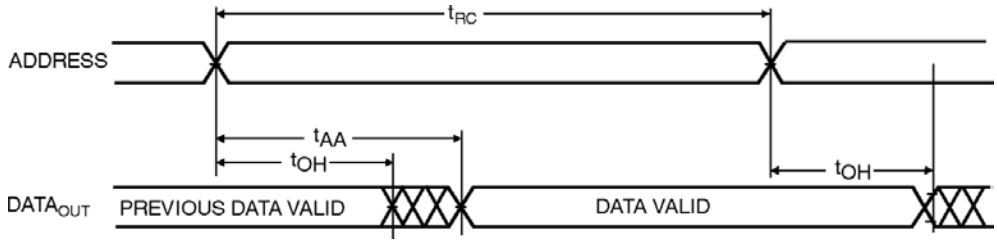
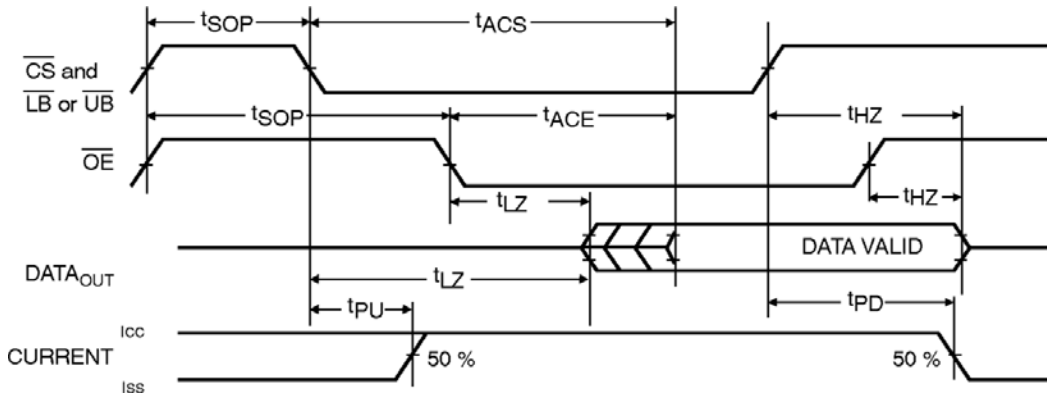


FIGURE 2. TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1,4,5]



1. F/$\overline{W}$ is high for read cycles.
2. Device is continuously enabled, $\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_L. This waveform cannot be used for semaphore reads.
3. $\overline{CE}$ = V_{IL}.
4. Addresses valid prior to or coincident with $\overline{CS}$ transition.
5. To access RAM, $\overline{CS}$ = V_L, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CS}$ = V_{IH}, $\overline{SEM}$ = V_{IL}.

FIGURE 3. TIMING WAVEFORM OF READ CYCLE NO. 3, EITHER SIDE[1,3,4,5]

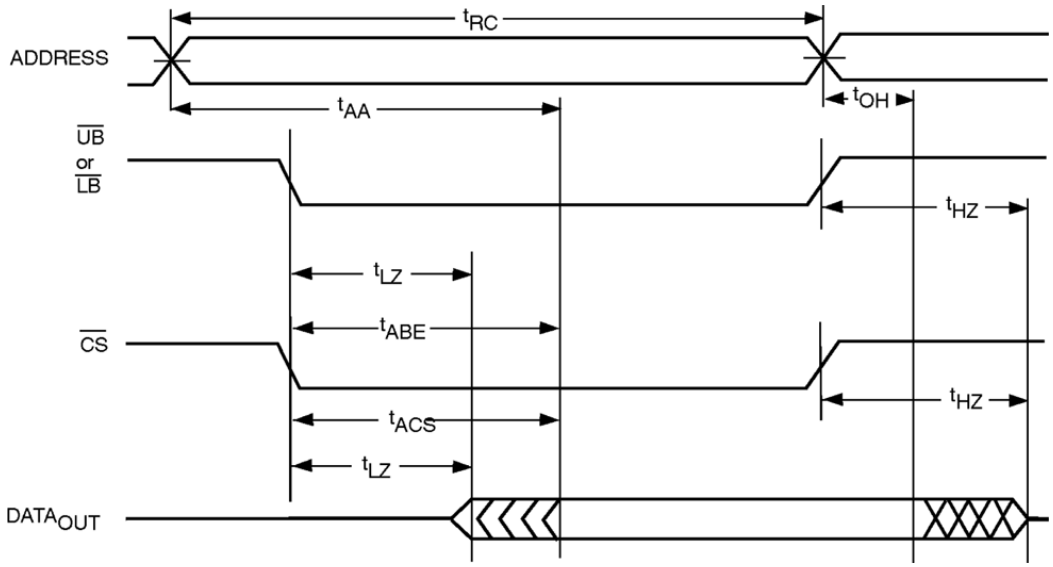
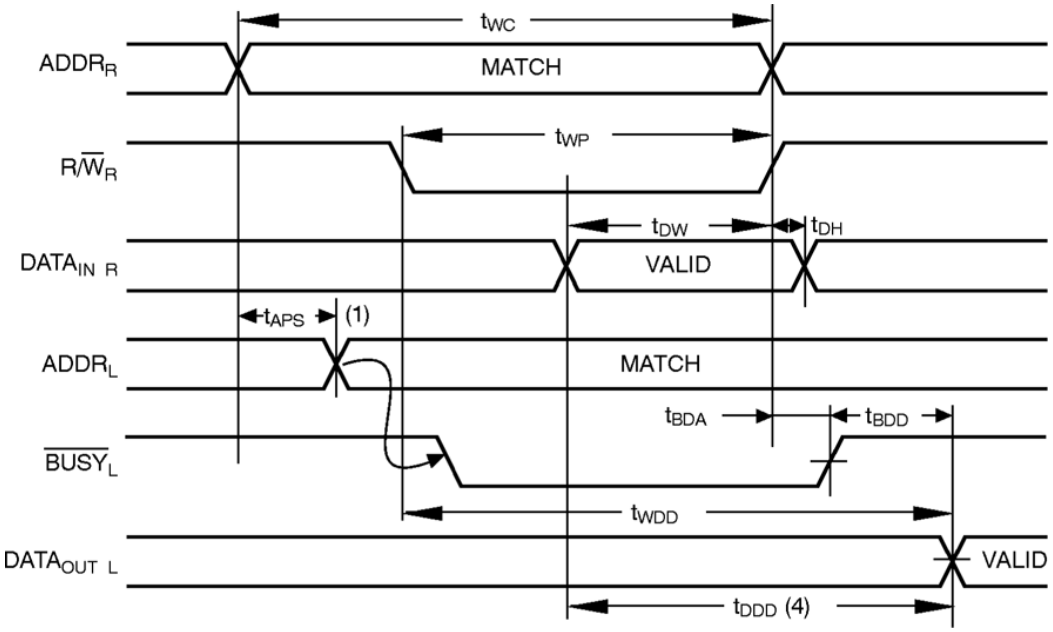
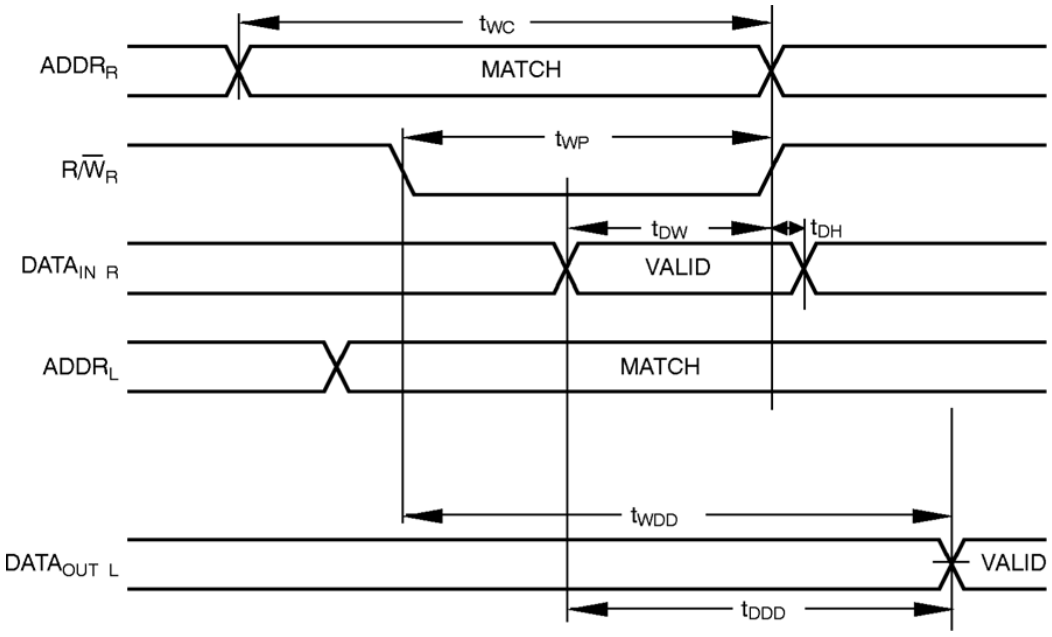


FIGURE 4. TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ [2,3,4] (FOR MASTER)



1. To ensure math, the earlier of the two ports wins.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enable for both ports.
4. $\overline{OE}$ = L for the reading port.

FIGURE 5. TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT [1,2,3] (FOR SLAVE ONLY)



1. Assume $\overline{BUSY}$ Input = H or the writing port, and $\overline{OE}$ = L for the reading port.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enable for both ports.

FIGURE 6. TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING[1,2,3,7]

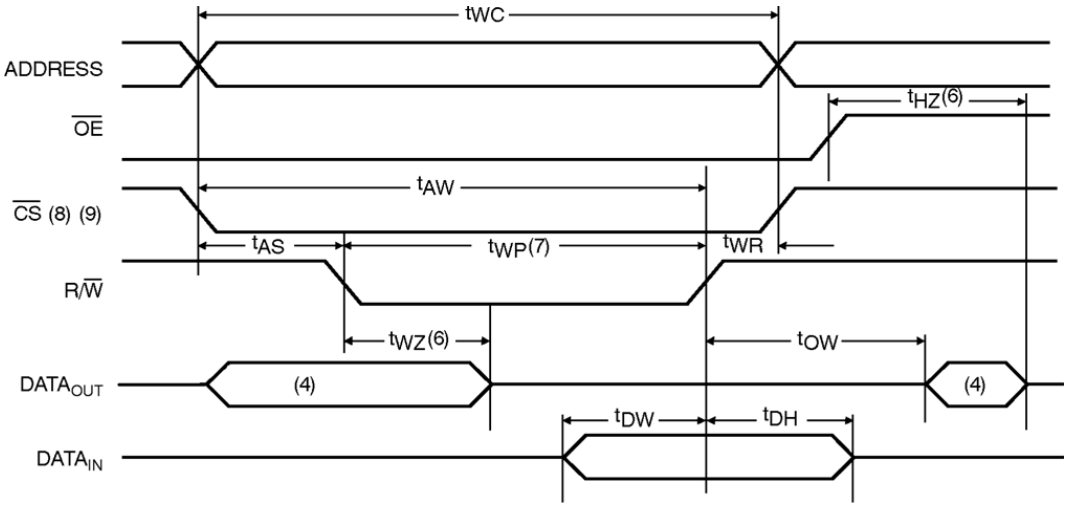


FIGURE 7. TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CS}$ CONTROLLED TIMING [1,2,3,5]

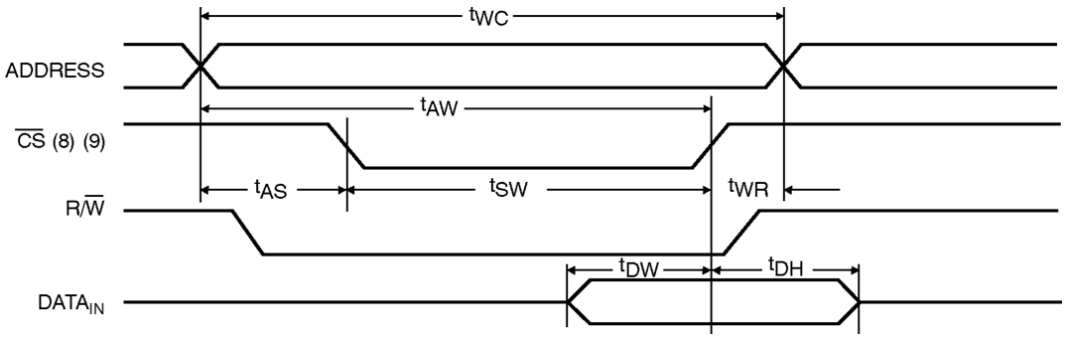
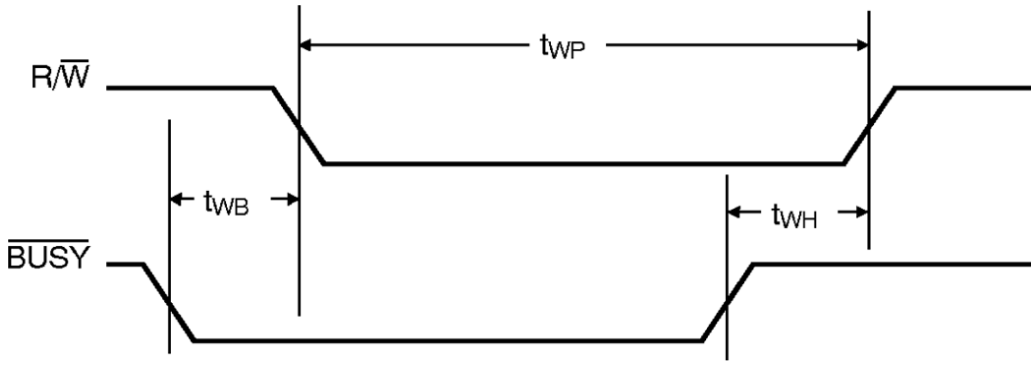


FIGURE 8. TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (FOR SLAVE)



1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{SW} to t_{WF}) of a low $\overline{CS}$ or $\overline{SEM}$ and a low R/$\overline{W}$.
3. $T_{.WF}$ is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transitions measured = 500 mV from steady state with a 5 pF load (including scope and jig). This parameter is sample and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of two or (t_{WZ} +t_{DW}) to allow the I/O driver to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. To access RAM, $\overline{CS}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
9. To access upper byte, $\overline{CS}$ = V_{IL}, $\overline{UB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
   To access lower byte, $\overline{CS}$ = V_{IL}, $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.

FIGURE 9. TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CS}$ ARBITRATION (FOR MASTER)

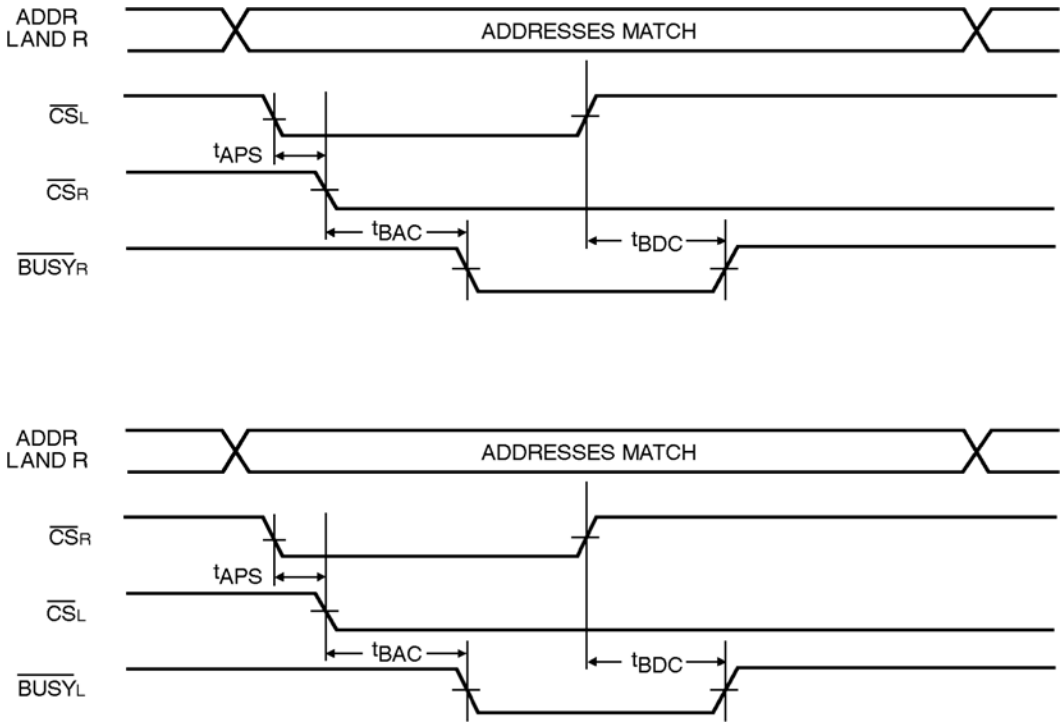
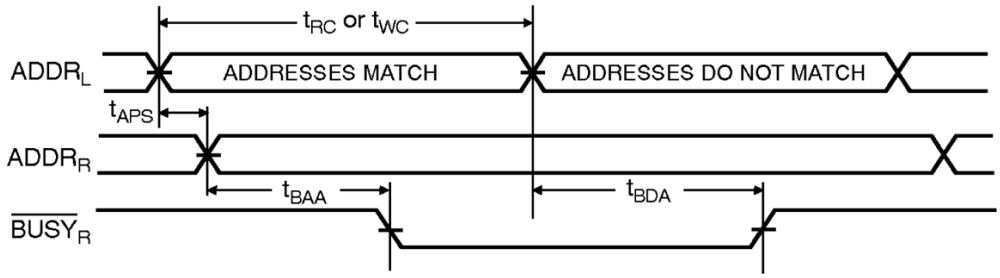
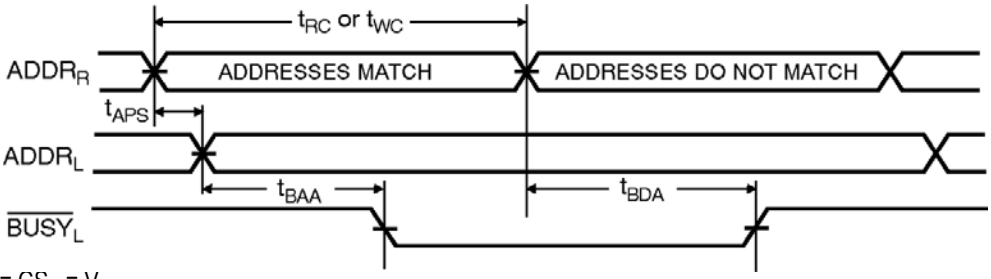


FIGURE 10. TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (FOR MASTER ONLY) [1]

LEFT ADDRESS VALID FIRST



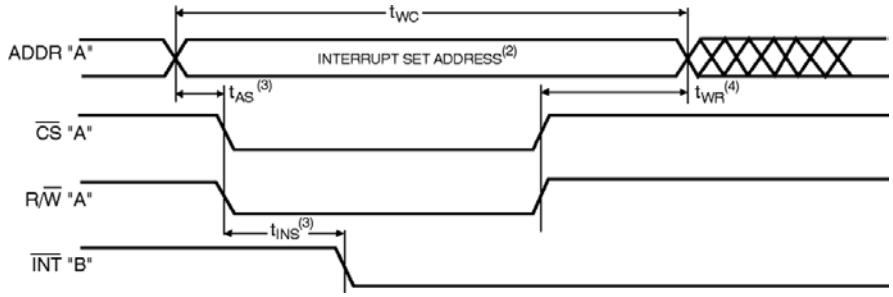
RIGHT ADDRESS VALID FIRST



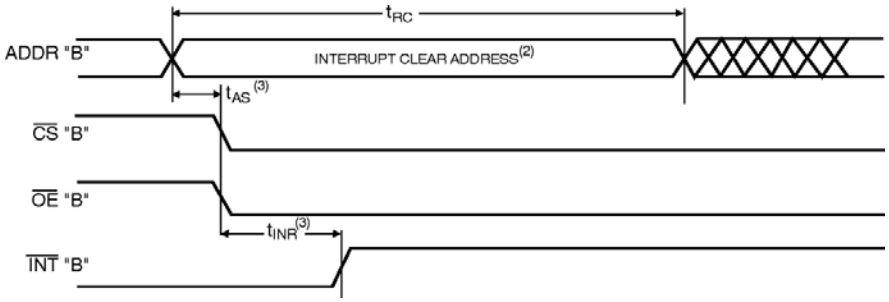
1. $\overline{CS}_L = CS_R = V_{IL}$.

FIGURE 11. WAVEFORM OF INTERRUPT TIMING [1]

SET ADDRESS

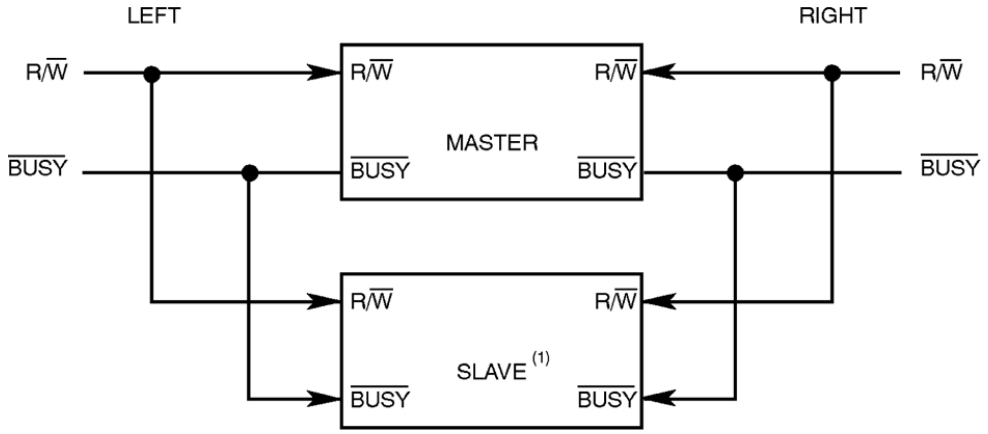


CLEAR ADDRESS



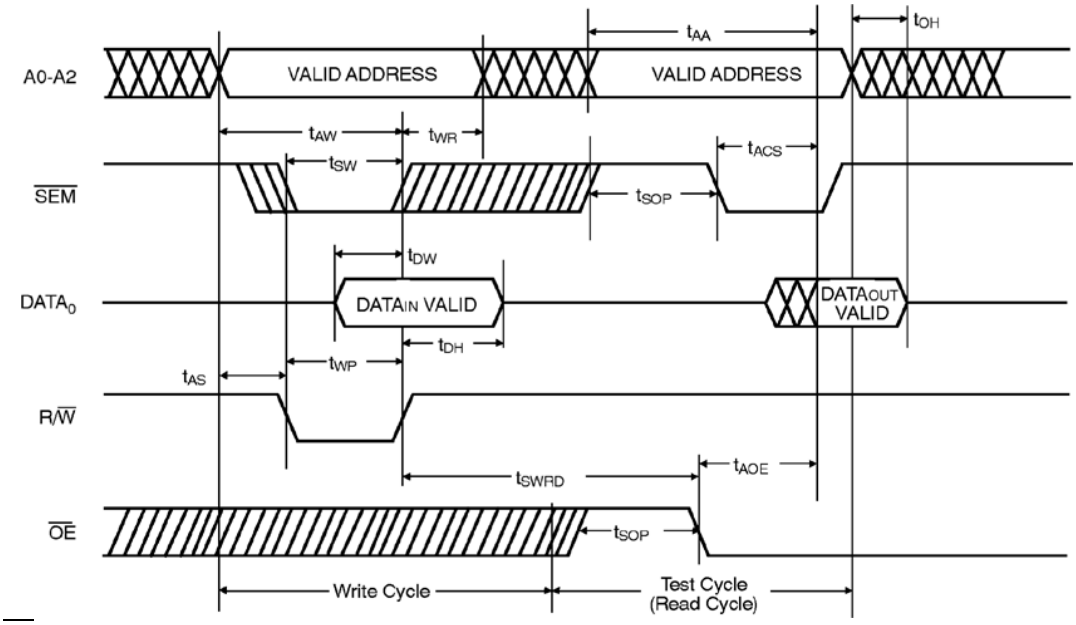
1. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from “A”.
2. See interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

FIGURE 12. 32-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



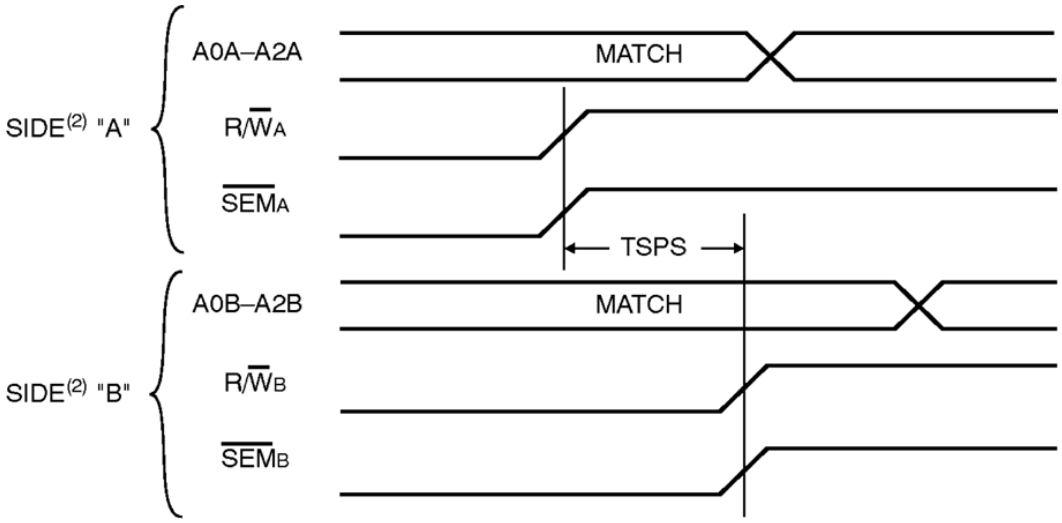
1. No arbitration in Master/Slave. $\overline{BUSY}$ - IN inhibits write in Master/Slave.

FIGURE 13. TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE [1]

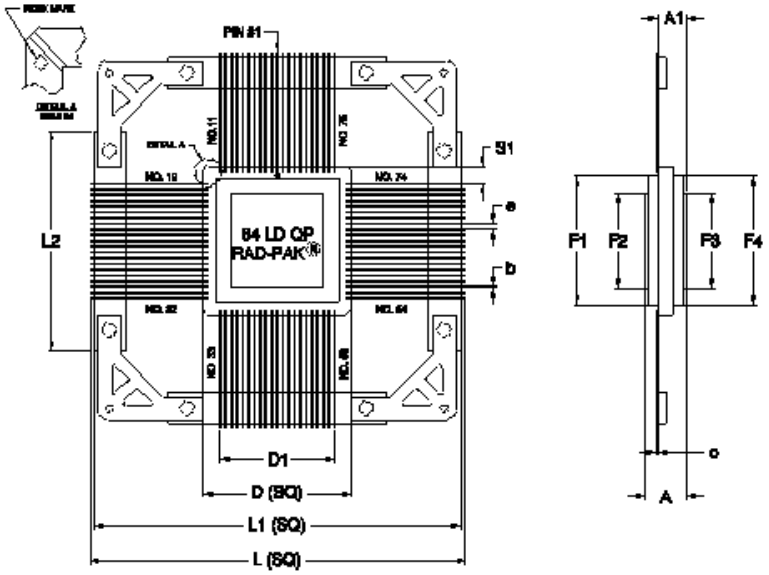


1. $\overline{CS}$ = V_{IH} for the duration of the above timing (both write and read cycle).

FIGURE 14. TIMING WAVEFORM OF SEMAPHORE CONTENTION [1,3,4]



1. $D_{OR} = D_{OL} = V_{IL}$, $\overline{CS}_R = \overline{CS}_L = V_{IH}$, semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. Either side “A” = left and side “B” = right, or side “A” = right and side “B” = left.
3. This parameter is measured from the point where $R/\overline{W}_A$ or $\overline{SEM}_A$ goes high until $R/\overline{W}_B$ or $\overline{SEM}_B$ goes high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guaranty which side will obtain the flag.



84 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.163	0.176	0.189
A1	0.113	0.123	0.133
b	0.006	0.010	0.014
c	0.004	0.006	0.010
D	0.635	0.650	0.665
D1	0.500 BSC		
e	0.025 BSC		
S1	0.005	0.070	--
F1	0.540	0.545	0.550
F2	0.415	0.420	0.425
F3	0.412	0.415	0.418
F4	0.560	0.565	0.570
L	--	1.620	1.635
L1	1.595	1.600	1.615
L2	0.940	0.950	0.960
N	84		

Q84-01

Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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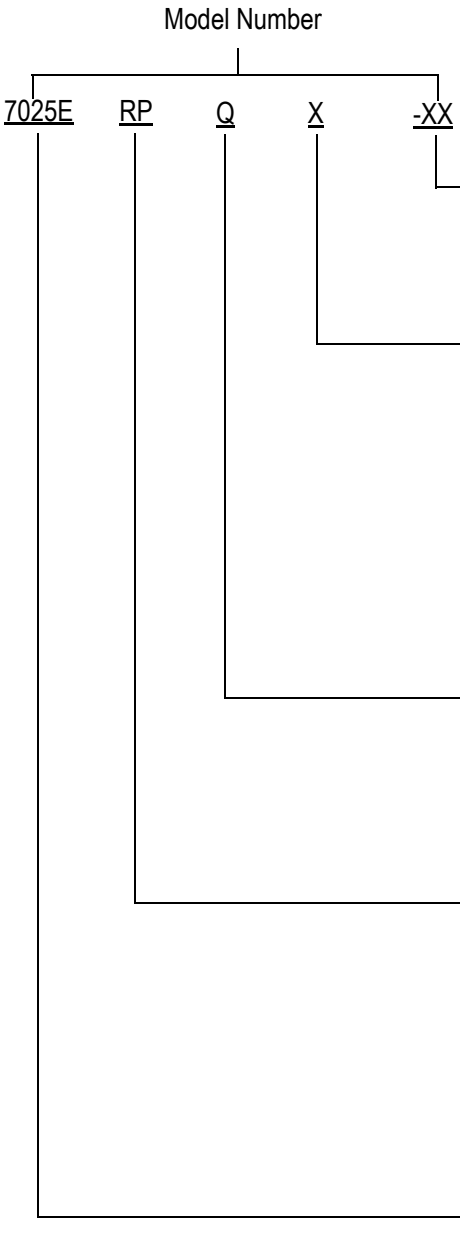
Product Ordering Options



Feature	Option Details
Access Time	35 = 35 ns 45 = 45 ns
Screening Flow	Monolithic S = Maxwell Class S B = Maxwell Class B E = Engineering (testing @ +25°C) I = Industrial (testing @ -55°C, +25°C, +125°C)
Package	Q = Quad Flat Pack
Radiation Feature	RP = RAD-PAK® package
Base Product Nomenclature	(8K x 16-Bit) Dual Port RAM High-Speed CMOS