DESCRIPTION

7314 is a four-channel input digital audio processor utilizing CMOS Technology. Volume, Bass, Treble and Balance are incorporated into a single chip. Loudness Function and Selectable Input Gain are also provided to build a highly effective electronic audio processor having the highest performance and reliability with the least external components. All functions are programmable using the I^2C Bus. The pin assignments and application circuit are optimized for easy PCB layout and cost saving advantage for audio application.

FEATURES

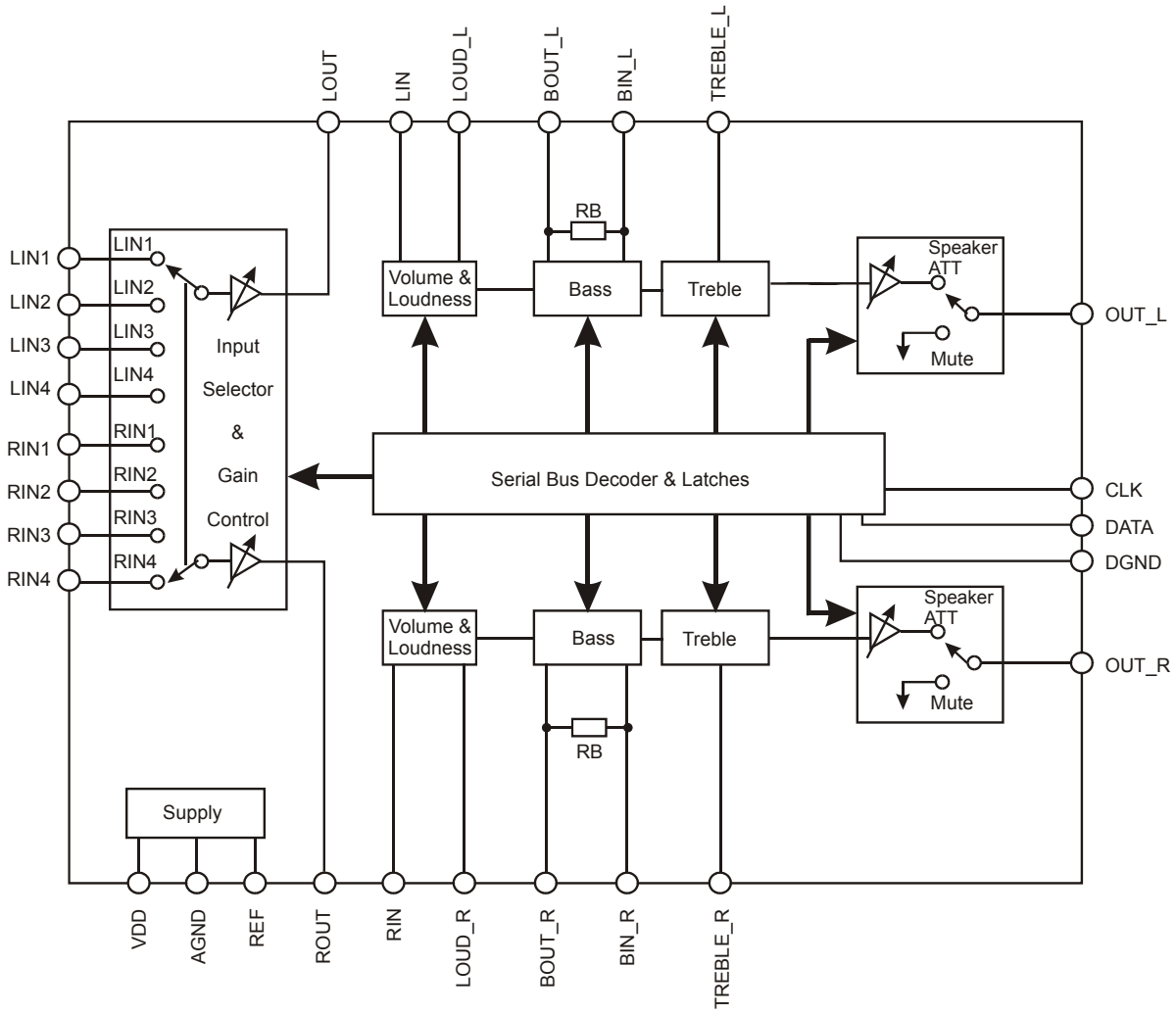
- CMOS technology
- Least external components
- Treble and bass control
- Loudness function
- 4 stereo inputs with selectable input gain
- Input/output for external noise reduction system/equalizer
- 2 independent speaker controls for balance control
- Independent mute function
- Volume control in 1.25 dB/step
- Low distortion
- Low noise and DC stepping
- Controlled by I^2C bus micro-processor interface
- Available in 28 Pins, DIP or SOP

APPLICATIONS

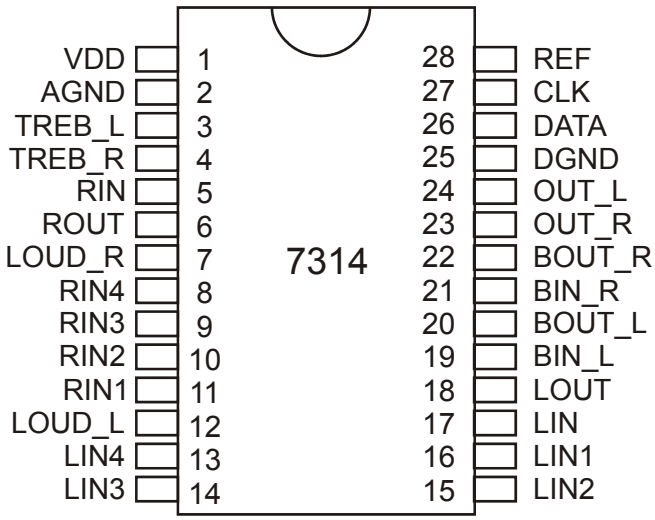
- Car stereo (Audio)
- Hi-Fi audio system

Note: Purchase of I^2C Component of Princeton Technology Corporation (PTC) conveys a license under Philips I^2C Patent Right to use these components in any I^2C System, provided that the system conforms to the I^2C Standard Specification defined by Philips

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
VDD	-	Supply Input Voltage	1
AGND	-	Analog Ground	2
TREB_L	I	Left Channel Input for Treble Controller	3
TREB_R	I	Right Channel Input for Treble Control	4
RIN	I	Audio Processor Right Channel Input	5
ROUT	O	Gain Output and Input Selector for Right Channel	6
LOUD_R	I	Right Channel Loudness Input	7
RIN4	I	Right Channel Input 4	8
RIN3	I	Right Channel Input 3	9
RIN2	I	Right Channel Input 2	10
RIN1	I	Right Channel Input 1	11
LOUD_L	I	Left Channel Loudness Input	12
LIN4	I	Left Channel Input 4	13
LIN3	I	Left Channel Input 3	14
LIN2	I	Left Channel Input 2	15
LIN1	I	Left Channel Input 1	16
LIN	I	Audio Processor Left Channel Input	17
LOUT	O	Gain Output and Input Selector for Left Channel	18
BIN_L	I	Left Channel Input for Bass Controller	19
BOUT_L	O	Left Bass Controller Output Channel	20
BIN_R	I	Right Channel Input for Bass Controller	21
BOUT_R	O	Right Channel Output for Bass Controller	22
OUT_R	O	Right Speaker Output	23
OUT_L	O	Left Speaker Output	24
DGND	-	Digital Ground	25
DATA	I	Control Data Input	26
CLK	I	Clock Input for Serial Data Transmission	27
REF	-	Analog Reference Voltage (1/2 VDD)	28

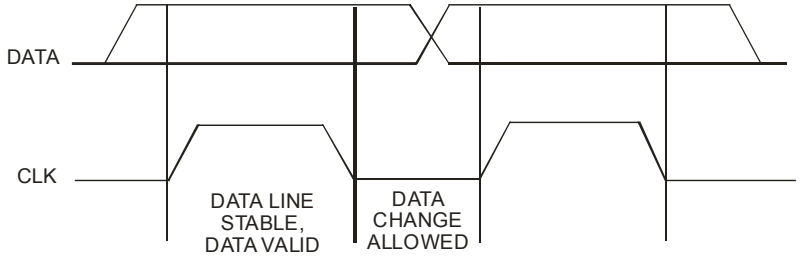
FUNCTIONAL DESCRIPTION

BUS INTERFACE

Data are transmitted to and from the microprocessor to the 7314 via the DATA and CLK. The DATA and CLK make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

DATA VALIDITY

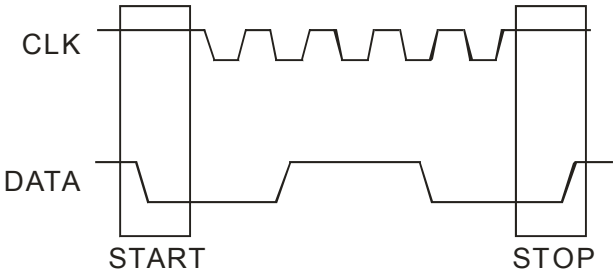
A data on the DATA Line is considered valid and stable only when the CLK Signal is in HIGH State. The HIGH and LOW State of the DATA Line can only change when the CLK signal is LOW. Please refer to the figure below.



START AND STOP CONDITIONS

A Start Condition is activated when
1) the CLK is set to HIGH and
2) DATA shifts from HIGH to LOW State.

The Stop Condition is activated when
1) CLK is set to HIGH and
2) DATA shifts from LOW to HIGH State. Please refer to the timing diagram below.

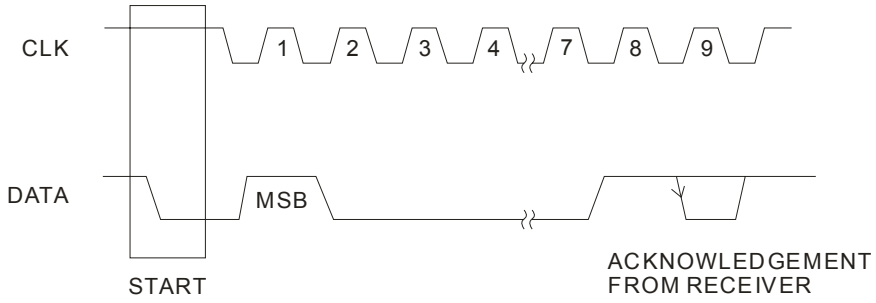


BYTE FORMAT

Every byte transmitted to the DATA Line consist of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μP) puts a resistive HIGH level on the DATA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the DATA line during the Acknowledge Clock Pulse so that the DATA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an acknowledge after receiving each byte, otherwise, the DATA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

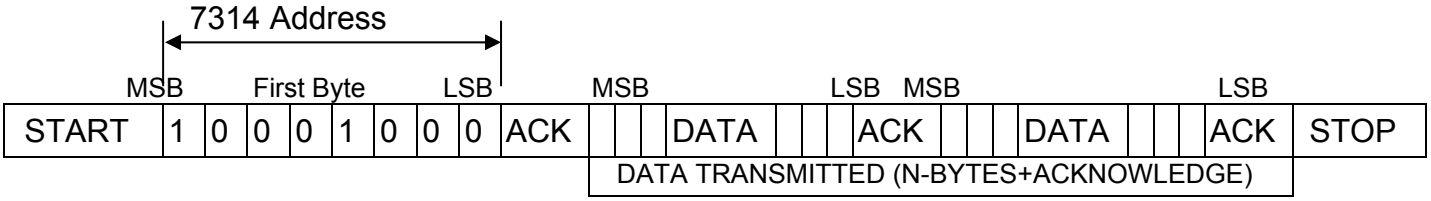
TRANSMISSION WITHOUT ACKNOWLEDGE

If you want to avoid the acknowledge detection of the audio processor, a simpler μP transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

INTERFACE PROTOCOL

The interface protocol consists of the following (see diagram below):

- A Start Condition
- A Chip Address Byte including the 7314 address. The 8th Bit of the Byte must be “0”. 7314 must always acknowledge the end of each transmitted byte.
- A Data Sequence (N-Bytes + Acknowledge)
- A Stop Condition



Note:
ACK = ACKNOWLEDGE
MAX. CLOCK SPEED = 100KBITS/S

SOFTWARE SPECIFICATION

7314 ADDRESS

7314 Address is shown below.

1 MSB	0	0	0	1	0	0	0 LSB

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT L
1	1	1	B1	B0	A2	A1	A0	Speaker ATT R
0	1	0	G1	G0	S2	S1	S0	Audio Switch
0	1	1	0	C3	C2	C1	C0	Bass Control
0	1	1	1	C3	C2	C1	C0	Treble Control

where Ax = 1.25 dB steps; Bx = 10 dB steps; Cx = 2 dB steps; Gx = 3.75 dB/steps

VOLUME

The table below gives a detailed description of the Volume Data Bytes. For example, a volume of -37.5 dB is given by 0 0 0 1 1 1 1 0.

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25 dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

SPEAKER ATTENUATORS

The table below gives a detailed description of the speaker attenuators data bytes. For example, an attenuation of 30dB on the Speaker R (Right) is given by: 1 1 1 1 1 0 0 0.

MSB							LSB	Function
1	1	0	B1	B0	A2	A1	A0	Speaker L
1	1	1	B1	B0	A2	A1	A0	Speaker R
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

AUDIO SWITCH DATA BYTE

The following table shows the detailed description of the Audio Switch Data Bytes. For example, a Stereo 1 Input with Gain of +11.25 dB Loudness ON is given by: 0 1 0 0 0 0 0 0.

MSB							LSB	Function
0	1	0	G1	G0	S2	S1	S0	Audio Switch
						0	0	Stereo 1
						0	1	Stereo 2
						1	0	Stereo 3
						1	1	Stereo 4
					0			Loudness ON
					1			Loudness OFF
			0	0				+11.25dB
			0	1				+7.5dB
			1	0				+3.75dB
			1	1				0dB

BASS AND TREBLE DATA BYTES

The following table shows a detailed description of the Bass and Treble Data Byte. For example a Treble at -12dB is given by: 0 1 1 1 0 0 0 1.

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

Unit: dB

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Operating supply voltage	Vs	10.5	V
Operating temperature	Topr	-40 to +85	℃
Storage temperature	Tstg	-65 to +150	℃

QUICK REFERENCE DATA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vs	6	9	10	V
Max. input signal handling	VCL	2	2.5		Vrms
Total harmonic distortion (V=1Vrms, f=1KHz)	THD		0.07	0.15	%
Signal to noise ratio	S/N		95		dB
Channel separation (f=1KHz)	Sc		85		dB
Volume control 1.25dB step		-75		0	dB
Bass & treble control 2dB step		-14		+14	dB
Balance control 1.25dB step		-37.5		0	dB
Input gain 3.75dB step		0		11.25	dB
Mute attenuation			85		dB

ELECTRICAL CHARACTERISTICS

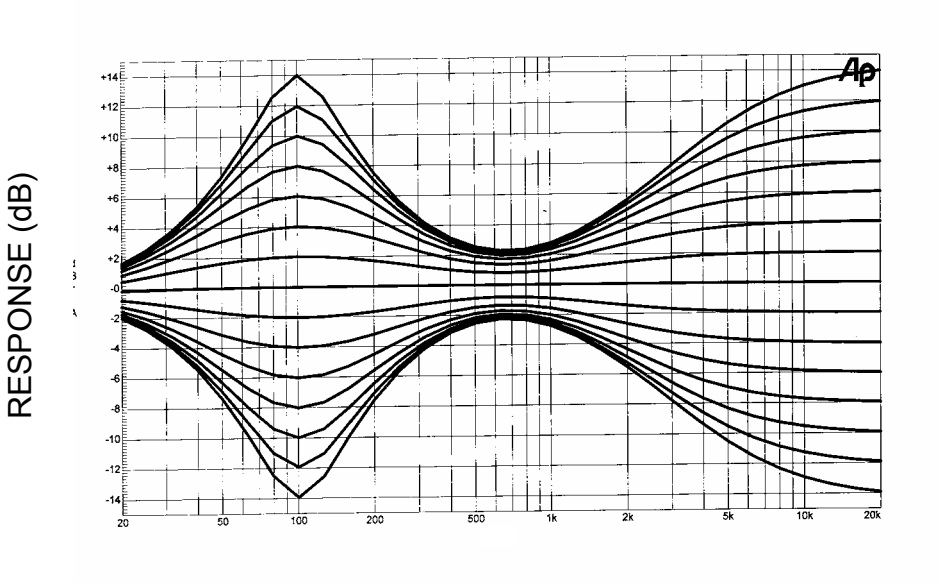
(Unless specified: Ta=25℃, Vc=9V, RL=10KΩ, Rg = 600Ω, all controls flat (G=0), f=1KHz)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply						
Supply voltage	Vcc		6	9	10	V
Supply current	Is			30	40	mA
Input Selectors						
Input resistance	R_{II}	Input 1,2,3	80	100	120	KΩ
Clipping level	V_{CL}	Av=-8.75 dB ; d=0.3%	2	2.5		Vrms
Input separation (2)	S_{IN}		80	100		dB
Min. input gain	G_{INmin}		-1	0	1	dB
Max. input gain	G_{INmax}			11.25		dB
Volume Control						
Input resistance	R_{IV}		30	40	50	KΩ
Control range	C_{RANGE}		65	70	75	dB
Min. attenuation	A_{VMIN}		-1	0	1	dB
Max. attenuation	A_{VMAX}		65	70	75	dB
Step resolution	A_{STEP}		0.5	1.25	1.75	dB
Attenuation set error	E_A	AV=0 to -20dB AV=-20 to –60dB	-1.25 -3.0	0	1.25 2	dB dB
Speaker Attenuators						
Control range	C_{RANGE}		35	37.5	40	dB
Step resolution	S_{STEP}		0.5	1.25	1.75	dB
Attenuation set error	E_A				1.5	dB
Output mute attenuation	A_{MUTE}		75	85		dB
Bass Control (1)						
Control range	Gb	Max. Boost/Cut	±12	±14	±16	dB
Step resolution	B_{STEP}		1	2	3	dB
Internal feedback resistance	R_B		34	44	58	KΩ
Treble Control (1)						
Control range	Gt	Max. Boost/Cut	±13	±14	±15	dB
Step resolution	T_{STEP}		1	2	3	dB

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Audio Outputs						
Clipping level	V_{OCL}	d=0.3%	2	2.5		Vrms
Output resistance	R_{OUT}		1.7	1.9	2.1	Ω
DC voltage level	V_{OUT}		4.2	4.5	4.8	V
General						
Output noise	e_{NO}	BW=20-20KHz, flat		-97		dB
		Output Muted All gains=0dB		-92		dB
		A Curve All Gains=0dB		-100		dB
Signal to noise ratio	S/N	All Gains=0dB Vo=1Vrms		95		dB
Distortion	d	AV=0, VIN=1Vrms		0.1	0.3	%
		AV=-8.75dB, VIN=1Vrms		0.07	0.15	%
		AV=-8.75dB, VIN=0.3Vrms		0.03	0.1	%
Channel separation left/right	Sc		80	90		dB
Bus Inputs						
Input low voltage	V_{IL}				1	V
Input high voltage	V_{IH}		3			V
Input current	I_{IN}		-5		+5	μA
Output voltage SDA acknowledge	Vo	Io=1.6mA			0.4	V

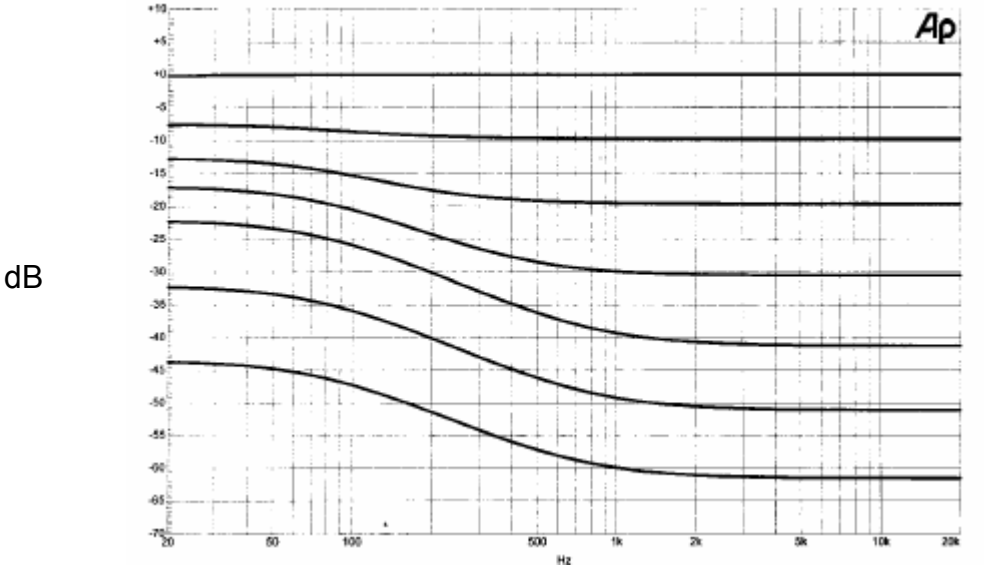
Notes:

1. For the Bass and Treble Response, please, refer to the diagram below. The center frequency and quality of the resonance behavior can be selected by the external circuitry. A standard first order bass response can realized by a standard feedback network.
2. The selected input is grounded thru the 2.2μF capacitor.



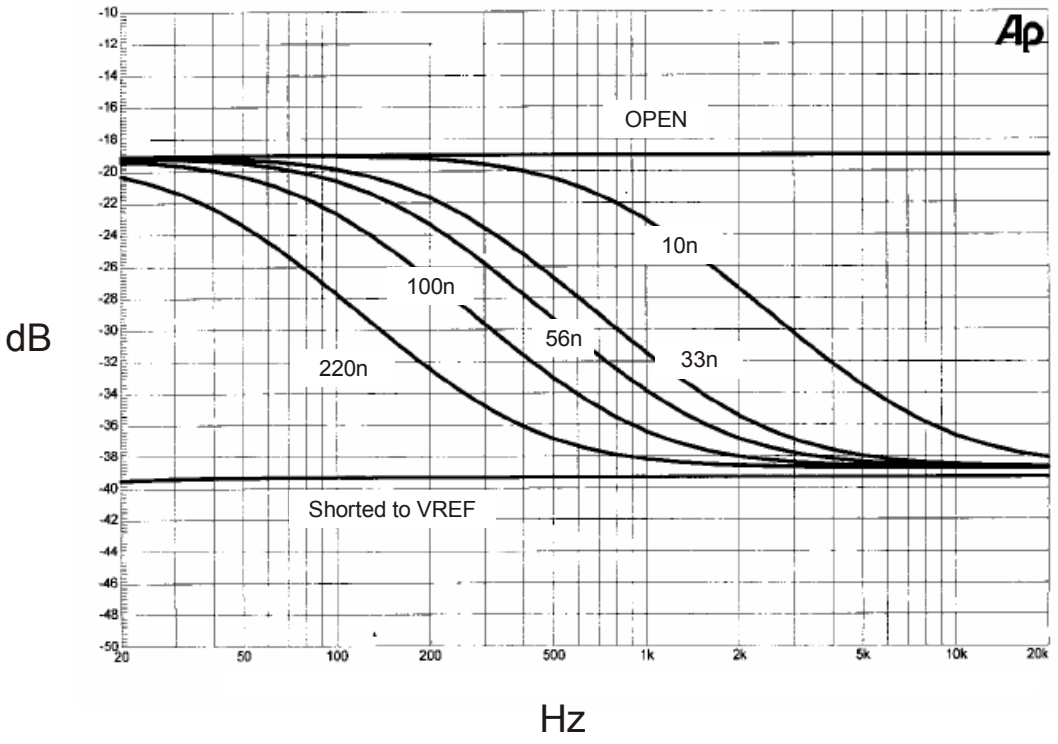
FREQUENCY (HZ)

Typical Tone Response (with the ext. Components indicated in the test circuit)



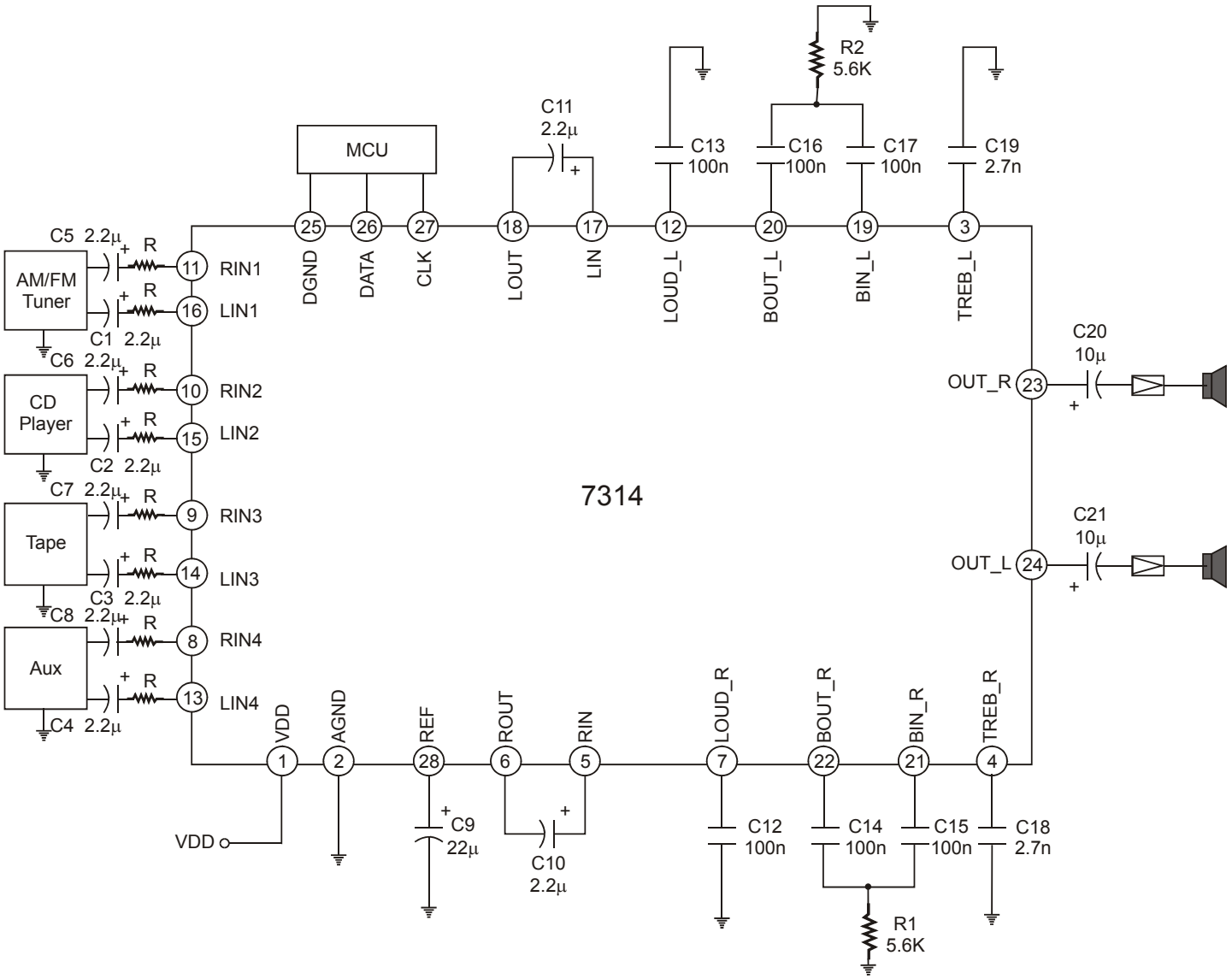
Hz

Loudness vs Volume Attenuation Frequency Response (C_{12}=C_{13}=100nF)



C12, C13 vs Loudness Frequency Response
(Volume=-40dB, All other controls are flat)

APPLICATION CIRCUIT



Notes:

1. It is suggested that you use Mylar Capacitor for capacitors, C12 ~ C19.
2. Resistor (R) Range = 2.0KΩ to 3.6KΩ
3. Recommended Value of Resistor (R) = 2.4KΩ

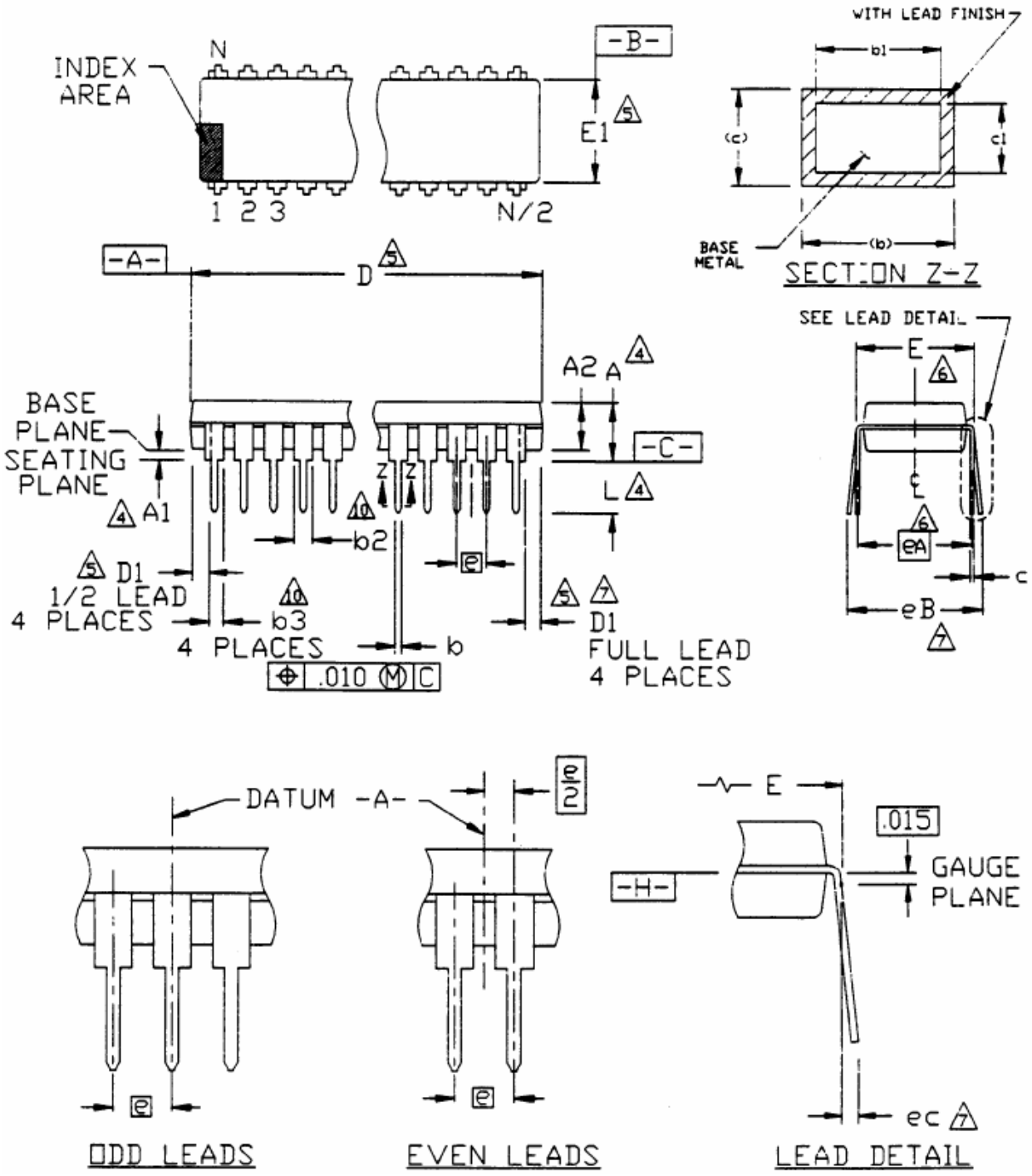
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
7314-D (L)	28 Pins, DIP, 300mil	7314-D
7314 (L)	28 Pins, SOP, 300mil	7314

Notes:
1. (L), (C) or (S) = Lead Free
2. The Lead Free mark is put in front of the date code.

PACKAGE INFORMATION

28 PINS, DIP, 300 MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	1.345	1.365	1.400
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 BSC		
eA	0.300 BSC		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. All dimensions are in INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. E and eA measured with the leads constrained to be perpendicular to datum -C-.
6. eB and eC are measured at the lead tips with the leads constrained. N is the number of terminal positions (N=28)
7. Pointed or rounded lead tips are preferred to ease insertion.
8. b2 and b3 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010” (0.25mm).
9. This variation is a ½ lead package.
10. Distance between leads including dambar protrusions to be 0.005 inch minimum.
11. Datum plane -H- coincident with the bottom of lead where lead exits body.
12. Refer to JEDEC MS-001 Variation BF.

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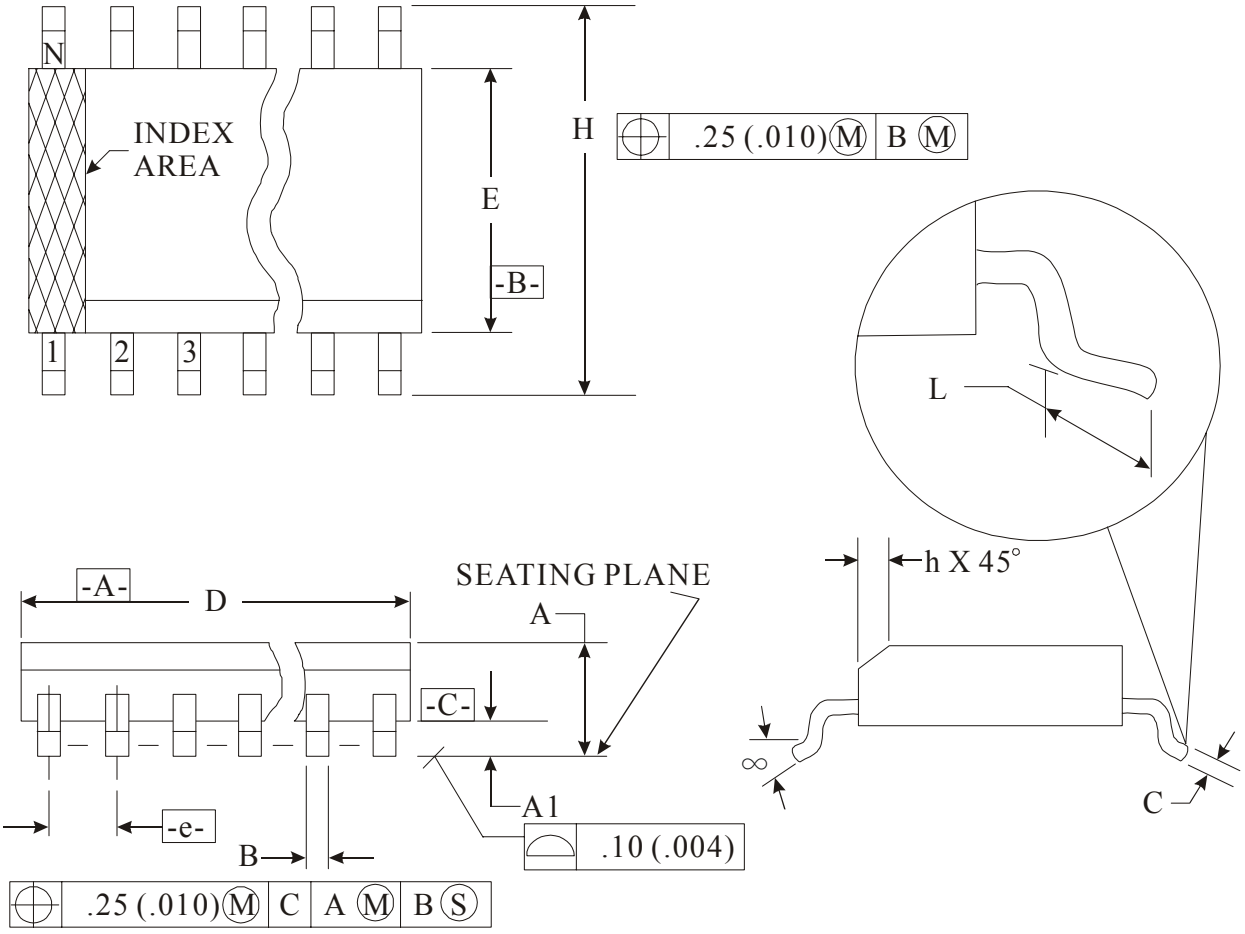
28 PINS, SOP, 300 MIL



Symbol	Min.	Nom.	Max.
A	2.35	-	2.65
A1	0.10	-	0.30
B	0.33	-	0.51
C	0.23	-	0.32
D	17.70	-	18.10
E	7.40	-	7.60
e	1.27 bsc.		
H	10.00	-	10.65
h	0.25	-	0.75
L	0.40	-	1.27
α	0°	-	8°

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension “E” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of the terminal for soldering to a substrate.
6. N is the number of the terminal positions (N=28)
7. The lead width “B” as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension：MILLIMETER.
9. Refer to JEDEC MS-013, Variation AE.

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