FAIRCHILD SEMICONDUCTOR™

August 1986
Revised September 1998

DM7490A
Decade and Binary Counter

General Description

The DM7490A monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The counter has a gated zero reset and also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

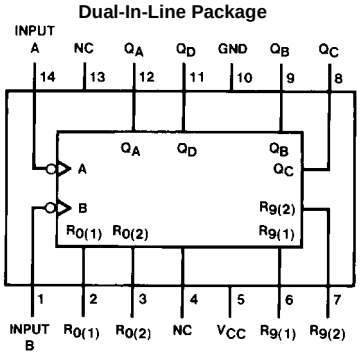
- Typical power dissipation
  - —90A 145 mW
- Count frequency 42 MHz

Ordering Code:

Order Number	Package Number	Package Description
DM7490AN	N14A	14-Lead Plastic Dual-In-Line Package, JECEC MS-001, 0.300" Wide

Connection Diagram

Dual-In-Line Package



Function Tables (Note 1)

BCD Count Sequence (Note 2)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BCD Bi-Quinary (5-2) (Note 3)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Reset/Count Function Table

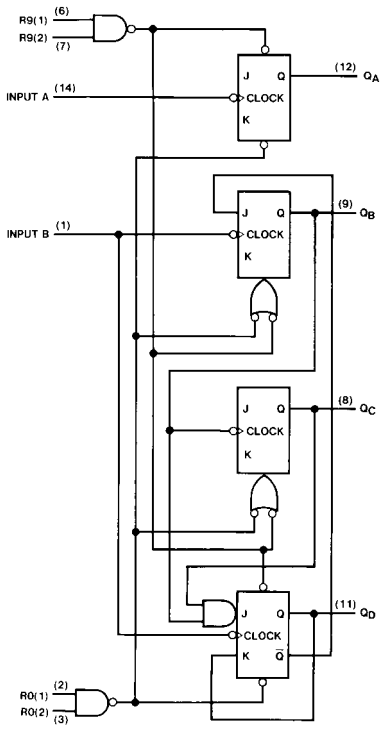
Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L		COUNT		
L	X	L	X		COUNT		
L	X	X	L		COUNT		
X	L	L	X		COUNT		

Note 1: H = High Level, L = Low Level, X = Don't Care.

Note 2: Output Q_A is connected to input B for BCD count.

Note 3: Output Q_D is connected to input A for bi-quinary count.

Logic Diagram



The J and K inputs shown without connection are for reference only and are functionally at a high level.

Absolute Maximum Ratings(Note 4)

Supply Voltage	7V	Operating Free Air Temperature Range	0°C to +70°C
Input Voltage	5.5V	Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				–0.8	mA
I_{OL}	Low Level Output Current				16	mA
f_{CLK}	Clock Frequency	A	0		32	MHz
	(Note 5)	B	0		16	
t_W	Pulse Width	A	15			ns
	(Note 5)	B	30			
		Reset	15			
t_{REL}	Reset Release Time (Note 5)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 4: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: $T_A = 25°C$ and $V_{CC} = 5V$.

DC Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –12 mA				–1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max (Note 7)			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	A			80	µA
			Reset			40	
			B			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A			–3.2	mA
			Reset			–1.6	
			B			–4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 8)	DM54	-20		-57	mA
			DM74	–18		–57	
I_{CC}	Supply Current	V_{CC} = Max (Note 9)			29	42	mA

Note 6: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 7: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

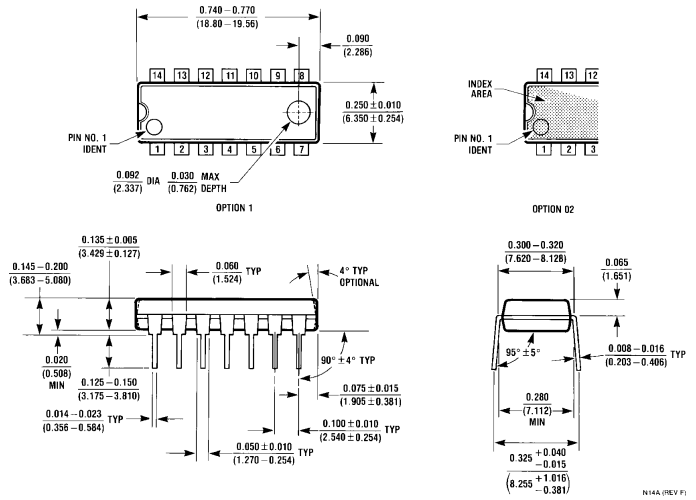
Note 8: Not more than one output should be shorted at a time.

Note 9: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

AC Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		MHz
		B to Q_B	16		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 Any Q		40	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package, JEDEC MS-001, 0.300" Wide
Package Number N14A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com