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Status	Product Specification
ACL Products	

# AC11543: Preliminary Specification

# ACT11543: Product Specification

## Octal latched transceiver with dual enable (3-State)

### FEATURES

- Combines '245 and '373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- 3-State buffers
- Output capability:  $\pm 24$  mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50 $\Omega$  incident wave switching
- Center-pin  $V_{CC}$  and ground configuration to minimize high-speed switching noise
- $I_{CC}$  category: MSI

### DESCRIPTION

The 74AC/ACT11543 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11543 Octal Latched Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ( $LE_{AB}$ ,  $LE_{BA}$ ) and Output Enable ( $OE_{AB}$ ,  $OE_{BA}$ ) inputs are provided for each register to permit inde-

*(continued)*

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS		TYPICAL		UNIT
		$T_{amb} = 25^{\circ}C; GND = 0V; V_{CC} = 5.0V$		AC	ACT	
$t_{PLH}/t_{PHL}$	Propagation delay $A_n$ to $B_n$ or $B_n$ to $A_n$	$C_L = 50pF$		5.5	6.4	ns
$C_{PD}$	Power dissipation capacitance per transceiver <sup>1</sup>	$f = 1MHz;$ $C_L = 50pF$	Enabled	45	47	pF
			Disabled	10	13	
$C_{IN}$	Input capacitance	$V_I = 0V$ or $V_{CC}$		4.5	4.5	pF
$C_{VO}$	I/O capacitance	$V_{VO} = 0V$ or $V_{CC};$ Disabled		12	12	pF
$I_{LATCH}$	Latch-up current	Per Jeduc JC40.2 Standard 17		500	500	mA

#### Note:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

$f_I$  = input frequency in MHz,  $C_L$  = output load capacitance in pF,

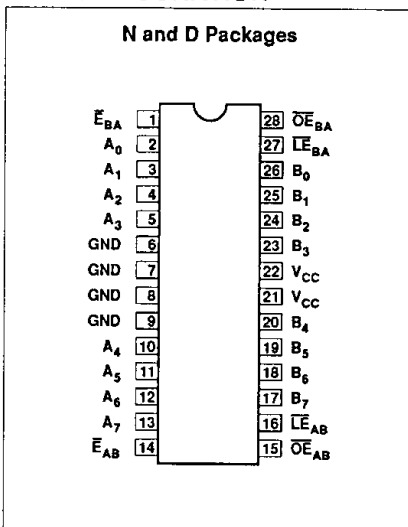
$f_O$  = output frequency in MHz,  $V_{CC}$  = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$  = sum of outputs

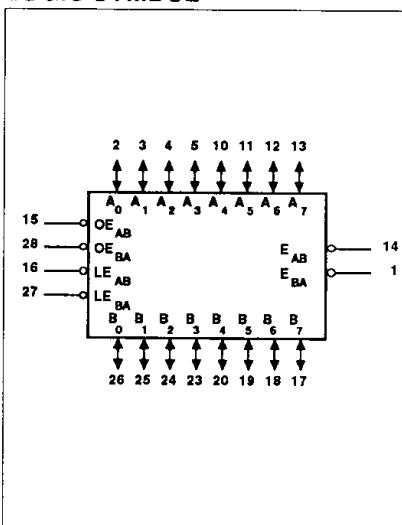
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11543N 74ACT11543N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11543D 74ACT11543D

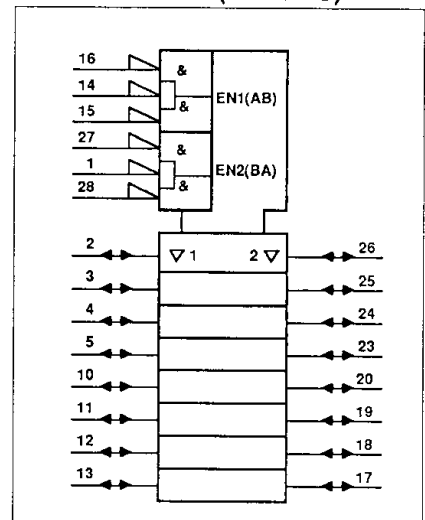
### PIN CONFIGURATION



### LOGIC SYMBOL



### LOGIC SYMBOL (IEEE/IEC)



# Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

pendent control of inputting and outputting in either direction of data flow.

## FUNCTIONAL DESCRIPTION

The 74AC/ACT11543 Octal Latched Transceiver contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B

Enable ( $\overline{E}_{AB}$ ) input must be Low in order to enter data from  $A_0 - A_7$  or take data from  $B_0 - B_7$  as indicated in the Function Table. With  $\overline{E}_{AB}$  Low, a Low signal on the A-to-B Latch Enable ( $\overline{LE}_{AB}$ ) input makes the A-to-B latches transparent; a subsequent Low-to-High transition of the  $\overline{LE}_{AB}$  signal puts the A latches in the storage mode and their

outputs no longer change with the A inputs. With  $\overline{E}_{AB}$  and  $\overline{OE}_{AB}$  both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the  $\overline{E}_{BA}$ ,  $\overline{LE}_{BA}$ , and  $\overline{OE}_{BA}$  inputs.

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
16	$\overline{LE}_{AB}$	A-to-B latch enable input (active Low)
27	$\overline{LE}_{BA}$	B-to-A latch enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	$A_0 - A_7$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	$B_0 - B_7$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	$V_{CC}$	Positive supply voltage

## FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs disabled
L	↑	L	h	Z	Diasabled + latched
L	↑	L	l	Z	
L	L	↑	h	H	Latch + display
L	L	↑	l	L	
L	L	L	H	H	Transparent
L	L	L	L	L	
L	L	H	X	NC	Hold

H = High voltage level

h = High state must be present one setup time before the Low-to-High transition of  $\overline{LE}_{XX}$  or  $\overline{E}_{XX}$  (XX = AB or BA)

L = Low voltage level

l = Low state must be present one setup time before the Low-to-High transition of  $\overline{LE}_{XX}$  or  $\overline{E}_{XX}$  (XX = AB or BA)

↑ = Low-to-High transition of  $\overline{LE}_{XX}$  or  $\overline{E}_{XX}$  (XX = AB or BA)

X = Don't care

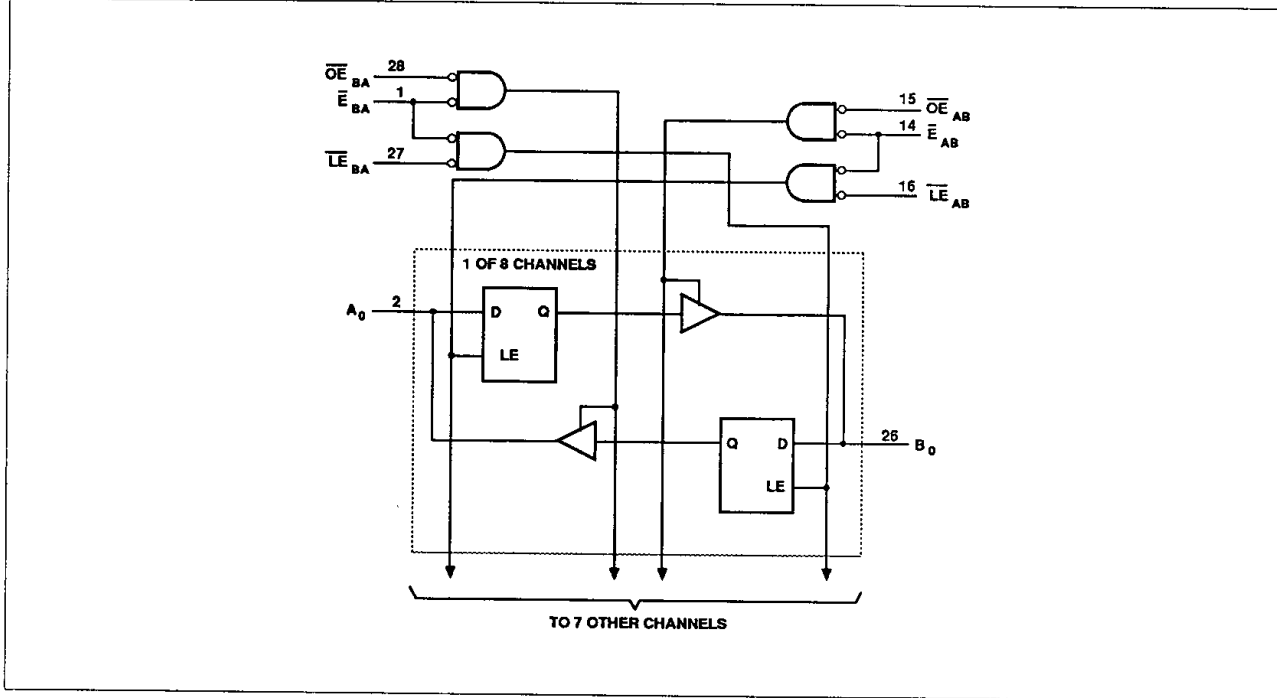
NC = No change

Z = High-impedance state

# Octal latched transceiver with dual enable (3-State)

**74AC/ACT11543**

## LOGIC DIAGRAM



# Octal latched transceiver with dual enable (3-State)

## 74AC/ACT11543

### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11543			74ACT11543			UNIT
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	DC supply voltage	3.0 <sup>1</sup>	5.0	5.5	4.5	5.0	5.5	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40		+85	-40		+85	°C

**NOTE:**

1. No electrical or switching characteristics are specified at  $V_{CC} < 3V$ . Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 TO +7.0	V
$I_{IK}$ or $V_I$	DC input diode current <sup>2</sup>	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{OK}$ or $V_O$	DC output diode current <sup>2</sup>	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current per output pin	$V_O = 0$ to $V_{CC}$	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ current		$\pm 400$	mA
	DC ground current		$\pm 400$	
$T_{STG}$	Storage temperature		-65 to 150	°C
$P_{TOT}$	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

**NOTES:**

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# Octal latched transceiver with dual enable (3-State)

## 74AC/ACT11543

### DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> V	74AC11543				74ACT11543				UNIT	
				T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C		T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V <sub>IL</sub>	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I <sub>OH</sub> = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
I <sub>OH</sub> = -75mA <sup>1</sup>	5.5			3.85				3.85					
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I <sub>OL</sub> = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I <sub>OL</sub> = 75mA <sup>1</sup>	5.5				1.65				1.65				
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I <sub>OZ</sub>	3-State output off-state current	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> , V <sub>O</sub> = V <sub>CC</sub> or GND	5.5		±0.5		5.0		±0.5		5.0	μA	
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI <sub>CC</sub>	Supply current, TTL inputs High <sup>2</sup>	One input at 3.4V, other inputs at V <sub>CC</sub> or GND	5.5						0.9		1.0	mA	

**NOTES:**

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V<sub>CC</sub>.

# Octal latched transceiver with dual enable (3-State)

## 74AC/ACT11543

### AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11543					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	1	2.9 4.0	7.6 8.8	9.2 10.6	2.9 4.0	10.4 11.9	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\overline{LE}_{BA}$ to A <sub>n</sub> or $\overline{LE}_{AB}$ to B <sub>n</sub>	2	3.5 4.3	8.8 9.7	10.7 12.0	3.5 4.3	12.0 13.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{OE}_{BA}$ to A <sub>n</sub> or $\overline{OE}_{AB}$ to B <sub>n</sub>	3	3.6 5.2	8.7 10.4	10.4 12.8	3.6 5.2	11.6 15.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{E}_{BA}$ to A <sub>n</sub> or $\overline{E}_{AB}$ to B <sub>n</sub>	3	4.1 5.7	9.6 11.3	11.4 14.1	4.1 5.7	12.7 16.7	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{OE}_{BA}$ to A <sub>n</sub> or $\overline{OE}_{AB}$ to B <sub>n</sub>	3	3.8 4.0	6.9 6.9	8.6 8.5	3.8 4.0	9.3 9.1	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{E}_{BA}$ to A <sub>n</sub> or $\overline{E}_{AB}$ to B <sub>n</sub>	3	4.3 4.3	7.7 7.6	9.4 9.8	4.3 4.3	10.1 10.4	ns
t <sub>S</sub>	Setup time, High or Low A <sub>n</sub> to $\overline{LE}_{AB}$ or B <sub>n</sub> to $\overline{LE}_{BA}$	4	3.0			3.0		ns
t <sub>H</sub>	Hold time, High or Low $\overline{LE}_{AB}$ to A <sub>n</sub> or $\overline{LE}_{BA}$ to B <sub>n</sub>	4	0.5			0.5		ns
t <sub>S</sub>	Setup time, High or Low A <sub>n</sub> to $\overline{E}_{AB}$ or B <sub>n</sub> to $\overline{E}_{BA}$	4	3.5			3.5		ns
t <sub>H</sub>	Hold time, High or Low $\overline{E}_{AB}$ to A <sub>n</sub> or $\overline{E}_{BA}$ to B <sub>n</sub>	4	0.0			0.0		ns
t <sub>W</sub>	Latch enable pulse width Low	2	400			4.0		ns

# Octal latched transceiver with dual enable (3-State)

## 74AC/ACT11543

### AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11543					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	1	2.3 3.3	4.8 6.1	6.8 8.0	2.3 3.3	7.5 8.9	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\overline{L}E_{BA}$ to A <sub>n</sub> or $\overline{L}E_{AB}$ to B <sub>n</sub>	2	3.0 3.7	5.6 6.6	7.6 8.9	3.0 3.7	8.4 9.9	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{O}E_{BA}$ to A <sub>n</sub> or $\overline{O}E_{AB}$ to B <sub>n</sub>	3	3.1 4.4	5.7 7.7	7.6 9.9	3.1 4.4	8.3 11.2	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{E}_{BA}$ to A <sub>n</sub> or $\overline{E}_{AB}$ to B <sub>n</sub>	3	3.6 4.9	6.2 8.3	8.3 10.6	3.6 4.9	9.1 12.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{O}E_{BA}$ to A <sub>n</sub> or $\overline{O}E_{AB}$ to B <sub>n</sub>	3	3.5 3.6	5.5 5.5	7.2 7.3	3.5 3.6	7.7 7.7	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{E}_{BA}$ to A <sub>n</sub> or $\overline{E}_{AB}$ to B <sub>n</sub>	3	3.9 4.0	6.0 6.0	7.7 8.1	3.9 4.0	8.3 8.5	ns
t <sub>S</sub>	Setup time, High or Low A <sub>n</sub> to $\overline{L}E_{AB}$ or B <sub>n</sub> to $\overline{L}E_{BA}$	4	2.0			2.0		ns
t <sub>H</sub>	Hold time, High or Low $\overline{L}E_{AB}$ to A <sub>n</sub> or $\overline{L}E_{BA}$ to B <sub>n</sub>	4	1.0			1.0		ns
t <sub>S</sub>	Setup time, High or Low A <sub>n</sub> to $\overline{E}_{AB}$ or B <sub>n</sub> to $\overline{E}_{BA}$	4	2.5			2.5		ns
t <sub>H</sub>	Hold time, High or Low $\overline{E}_{AB}$ to A <sub>n</sub> or $\overline{E}_{BA}$ to B <sub>n</sub>	4	0.5			0.5		ns
t <sub>W</sub>	Latch enable pulse width Low	2	4.0			4.0		ns

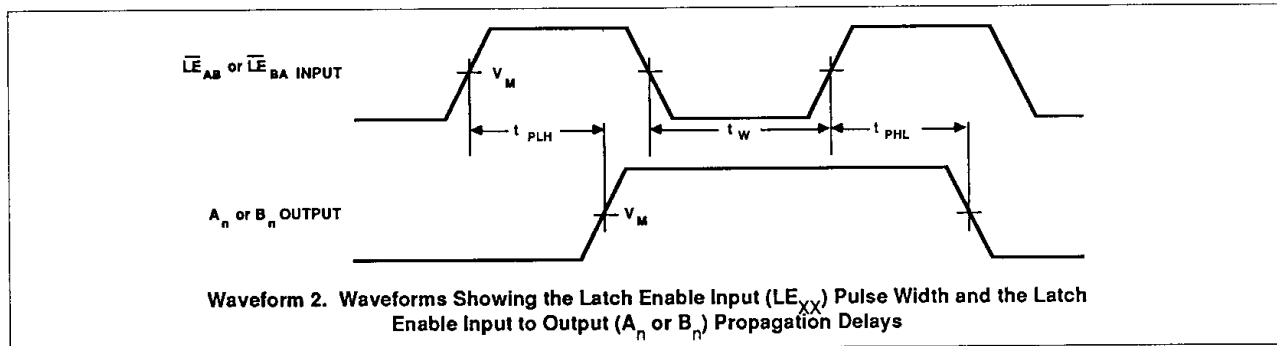
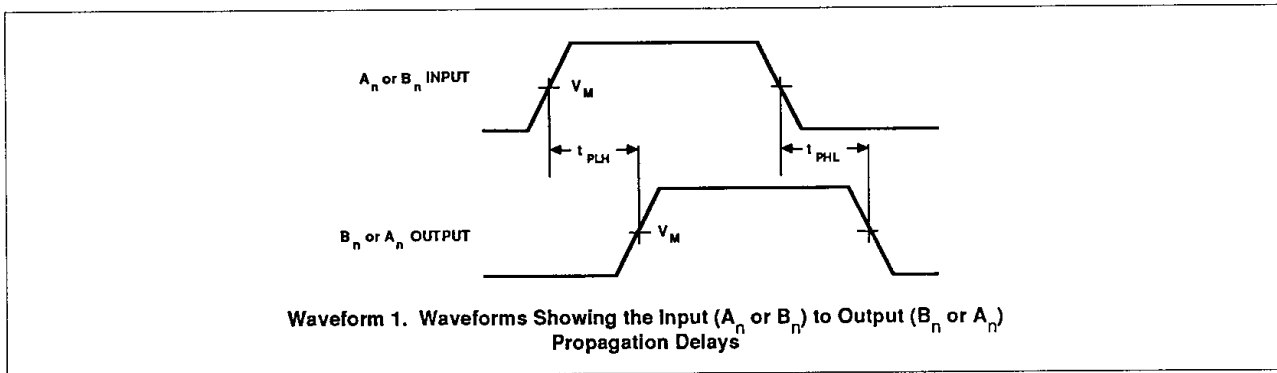
# Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

## AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11543					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	1	3.5 3.2	6.2 6.5	9.1 10.8	3.5 3.2	10.2 12.1	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\overline{LE}_{BA}$ to A <sub>n</sub> or $\overline{LE}_{AB}$ to B <sub>n</sub>	2	3.0 3.7	6.1 7.2	10.1 11.7	3.0 3.7	11.2 13.2	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{OE}_{BA}$ to A <sub>n</sub> or $\overline{OE}_{AB}$ to B <sub>n</sub>	3	3.3 3.0	6.4 8.0	10.5 12.8	3.3 3.0	11.5 15.3	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time $\overline{E}_{BA}$ to A <sub>n</sub> or $\overline{E}_{AB}$ to B <sub>n</sub>	3	3.5 3.2	6.7 8.4	11.1 13.4	3.5 3.2	12.2 16.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{OE}_{BA}$ to A <sub>n</sub> or $\overline{OE}_{AB}$ to B <sub>n</sub>	3	4.6 5.0	6.9 7.1	9.6 9.8	4.6 5.0	10.4 10.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time $\overline{E}_{BA}$ to A <sub>n</sub> or $\overline{E}_{AB}$ to B <sub>n</sub>	3	4.8 5.1	7.3 7.5	10.1 10.3	4.8 5.1	11.0 11.1	ns
t <sub>S</sub>	Setup time, High or Low A <sub>n</sub> to $\overline{LE}_{AB}$ or B <sub>n</sub> to $\overline{LE}_{BA}$	4	2.5			2.5		ns
t <sub>H</sub>	Hold time, High or Low $\overline{LE}_{AB}$ to A <sub>n</sub> or $\overline{LE}_{BA}$ to B <sub>n</sub>	4	2.0			2.0		ns
t <sub>S</sub>	Setup time, High or Low A <sub>n</sub> to $\overline{E}_{AB}$ or B <sub>n</sub> to $\overline{E}_{BA}$	4	3.0			3.0		ns
t <sub>H</sub>	Hold time, High or Low $\overline{E}_{AB}$ to A <sub>n</sub> or $\overline{E}_{BA}$ to B <sub>n</sub>	4	1.5			1.5		ns
t <sub>W</sub>	Latch enable pulse width Low	2	4.0			4.0		ns

### AC WAVEFORMS

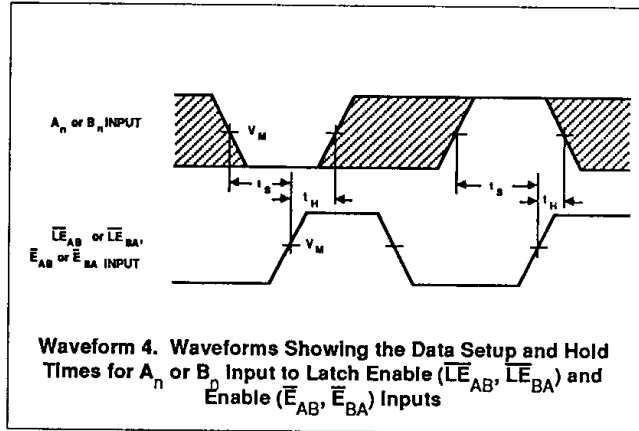
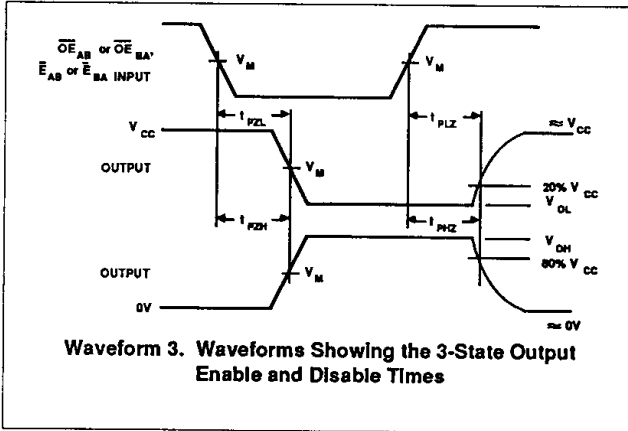




# Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

## AC WAVEFORMS (Continued)



## WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0\text{V}$ $V_M = 1.5\text{V}$	$V_M = 50\% V_{CC}$

## TEST CIRCUIT

**Test Circuit**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \cdot V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

**SWITCH POSITION**

**DEFINITIONS**

- $C_L$  = Load capacitance, 50pF; includes jig and probe capacitance
- $R_L$  = Load resistor, 500 $\Omega$
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators

Input pulses: PRR  $\leq$  10MHz  
 $t_r = t_f = 3\text{ns}$

# Definitions of Symbols

## ACL Products

### DEFINITIONS OF SYMBOLS AND TERMS USED IN ACL DATA SHEETS

#### Current

Positive current is defined as conventional current flow into a device.

Negative current is defined as conventional current flow out of a device.

$I_{CC}$  Quiescent power supply current; the current flowing into the  $V_{CC}$  supply terminal.

$\Delta I_{CC}$  Additional quiescent supply current per input pin at a specified input voltage and  $V_{CC}$ .

$I_{GND}$  Quiescent power supply current; the current flowing into the GND terminal.

$I_I$  Input leakage current; the current flowing into a device at a specified input voltage and  $V_{CC}$ .

$I_{IK}$  Input diode current; the current flowing into a device at a specified input voltage.

$I_{IO}$  Input/output source or sink current; the current flowing into a device at a specified input/output voltage.

$I_O$  Output source or sink current; the current flowing into a device at a specified output voltage.

$I_{OK}$  Output diode current; the current flowing into a device at a specified output voltage.

$I_{OZ}$  OFF-state output current; the leakage current flowing into the output of a 3-State device in the OFF-state, when the output is connected to  $V_{CC}$  or GND.

#### Voltages

All voltages are referenced to GND (ground), which is typically 0V.

$GND$  Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

$V_{CC}$  Supply voltage; the most positive potential on the device.

$V_{EE}$  Supply voltage; one of two (GND and  $V_{EE}$ ) negative power supplies.

$V_H$  Hysteresis voltage; difference between the trigger levels when applying a positive and a negative-going input signal.

$V_{IH}$  High-level input voltage; the range of input voltages that represents a logic High-level in the system.

$V_{IL}$  Low-level input voltage; the range of input voltages that represents a logic Low-level in the system.

$V_{OH}$  High-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a High-level at the output.

$V_{OL}$  Low-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a Low-level at the output.

$V_{T+}$  Trigger threshold voltage; positive-going signal.

$V_T$  Trigger threshold voltage; negative-going signal.

#### Capacitances

$C_I$  Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$  Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).

$C_L$  Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

$C_{PD}$  Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function when no extra load is provided to the device.

#### AC Switching Parameters

$f_i$  Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate High and Low for data input or using the toggle mode, whichever is applicable.

$f_O$  Output frequency; each output.

$f_{MAX}$  Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device function table.

$t_H$  Hold time; the interval immediately following the active transition of the timing pulse

## Definitions of Symbols

	(usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.	$t_{PLZ}$	3-State output disable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and a point representing 20% of the output swing on the output voltage waveform of a 3-State device, with the output changing from a Low-level ( $V_{OL}$ ) to a high-impedance OFF-state (Z).		input, normally measured at the 50% points for 74AC devices and the 1.5V points for the 74ACT devices on both input voltage waveforms.
$t_R, t_F$	Clock input rise and fall times; 10% and 90% values.			$t_S$	Setup time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval data to be recognized must be maintained at the input to ensure their recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
$t_{PHL}$	Propagation delay; the time between the specified reference points, normally the 50% points for 74AC devices on the input and output waveforms and the 1.5V points for the 74ACT devices, with the output changing from the defined High-level to the defined Low-level.	$t_{PZH}$	3-State output enable time; the time between the specified reference points, normally the 50% points for the 74AC devices and 1.5V points for the 74ACT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-State device, with the output changing from a high-impedance OFF-state (Z) to a High-level ( $V_{OH}$ ).	$t_{THL}$	Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High-to-Low.
$t_{PLH}$	Propagation delay; the time between the specified reference points, normally the 50% points for 74AC devices on the input and output waveforms and the 1.5V point for the 74ACT devices, with the output changing from the defined Low-level to the defined High-level.	$t_{PZL}$	3-State output enable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-State device with the output changing from a high-impedance OFF-state (Z) to a Low-level ( $V_{OL}$ ).	$t_{TLH}$	Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low-to-High.
$t_{PHZ}$	3-State output disable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and a point representing 20% of the output swing on the output voltage waveform of a 3-State device, with the output changing from a High-level ( $V_{OH}$ ) to a high-impedance OFF-state (Z).	$t_{REC}$	Recovery time; the time between the end of and overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock	$t_W$	Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for 74AC devices and at the 1.5V points for 74ACT devices.