

74AC541 • 74ACT541

Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The 74AC541 and 74ACT541 are octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

These devices are similar in function to the 74AC244 and 74ACTC244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

Features

- I_{CC} and I_{OZ} reduced by 50%
- 3-STATE outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24 mA
- 74AC541 is a non-inverting option of the 74AC540
- 74ACT541 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC541SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC541SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC541MTCX_NL (Note 1)	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC541PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT541SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT541MTCX_NL (Note 1)	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT541PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

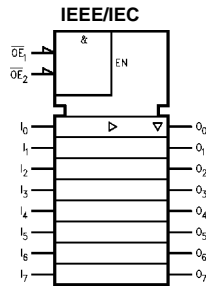
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

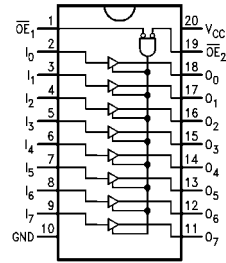
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74AC541 • 74ACT541 Octal Buffer/Line Driver with 3-STATE Outputs

Logic Symbol



Connection Diagram



Truth Table

Inputs			Outputs
\overline{OE}_1	\overline{OE}_2	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level

X = Immaterial

L = LOW Voltage Level

Z = High Impedance

Absolute Maximum Ratings ^(Note 2)		Recommended Operating Conditions	
Supply Voltage (V_{CC})	-0.5V to +7.0V	Supply Voltage (V_{CC})	AC 2.0V to 6.0V ACT 4.5V to 5.5V
DC Input Diode Current (I_{IK})		Input Voltage (V_I)	0V to V_{CC}
$V_I = -0.5V$	-20 mA	Output Voltage (V_O)	0V to V_{CC}
$V_I = V_{CC} + 0.5V$	+20 mA	Operating Temperature (T_A)	-40°C to +85°C
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$	Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
DC Output Diode Current (I_{OK})		AC: V_{IN} from 30% to 70% of V_{CC}	
$V_O = -0.5V$	-20 mA	V_{CC} @ 3.3V, 4.5V, 5.5V	
$V_O = V_{CC} + 0.5V$	+20 mA	ACT: V_{IN} from 0.8V to 2.0V	
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$	V_{CC} @ 4.5V, 5.5V	
DC Output Source or Sink Current (I_O)	± 50 mA		
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA		
Storage Temperature (T_{STG})	-65°C to +150°C		
Junction Temperature (T_J)			
PDIP	140°C		

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
			3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 3)}$
			4.5		3.86	3.76		
			5.5		4.86	4.76		
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
			3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 3)}$
			4.5		0.36	0.44		
			5.5		0.36	0.44		
I_{IN} (Note 5)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}, \text{ GND}$	
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		± 0.25	± 2.5	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}, \text{ GND}$ $V_O = V_{CC}, \text{ GND}$	
I_{OLD}	Minimum Dynamic Output Current (Note 4)	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$	
I_{OHD}	Output Current (Note 4)	5.5			-75	mA	$V_{OHD} = 3.85V \text{ Min}$	
I_{CC} (Note 5)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND	

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

AC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V) (Note 6)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	3.3	2.0	5.5	8.0	1.5	9.0	ns
	Data to Output	5.0	1.5	4.0	6.0	1.0	6.5	
t _{PHL}	Propagation Delay	3.3	2.0	5.5	8.0	1.5	8.5	ns
	Data to Output	5.0	1.5	4.0	6.0	1.0	6.5	
t _{PZH}	Output Enable Time	3.3	3.0	8.0	11.5	3.0	12.5	ns
		5.0	2.0	6.0	8.5	1.5	9.5	
t _{PZL}	Output Enable Time	3.3	2.5	7.0	10.0	2.5	11.5	ns
		5.0	1.5	5.5	7.5	1.0	8.5	
t _{PHZ}	Output Disable Time	3.3	3.5	9.0	12.5	2.5	14.0	ns
		5.0	2.0	7.0	9.5	1.0	10.5	
t _{PLZ}	Output Disable Time	3.3	2.5	6.5	9.5	2.0	10.5	ns
		5.0	2.0	5.5	7.5	1.0	8.5	

Note 6: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V _{IH}	Minimum HIGH Level	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1V or V _{CC} - 0.1V
	Input Voltage	5.5	1.5	2.0	2.0			
V _{IL}	Maximum LOW Level	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1V or V _{CC} - 0.1V
	Input Voltage	5.5	1.5	0.8	0.8			
V _{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9		V	I _{OUT} = -50 μA
	Output Voltage	4.5	4.49	4.4	4.4			
			4.5		3.86	3.76		V
V _{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA
	Output Voltage	4.5	0.001	0.1	0.1			
			4.5		0.36	0.44		V
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0		μA	V _I = V _{CC} , GND
I _{OZ}	Maximum 3-STATE Leakage Current	5.5		±0.25	±2.5		μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5		mA	V _I = V _{CC} - 2.1V
I _{OLD}	Minimum Dynamic	5.5			75		mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 8)	5.5			-75		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0		μA	V _{IN} = V _{CC} or GND

Note 7: All outputs loaded; thresholds on input associated with output under test.

Note 8: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for ACT

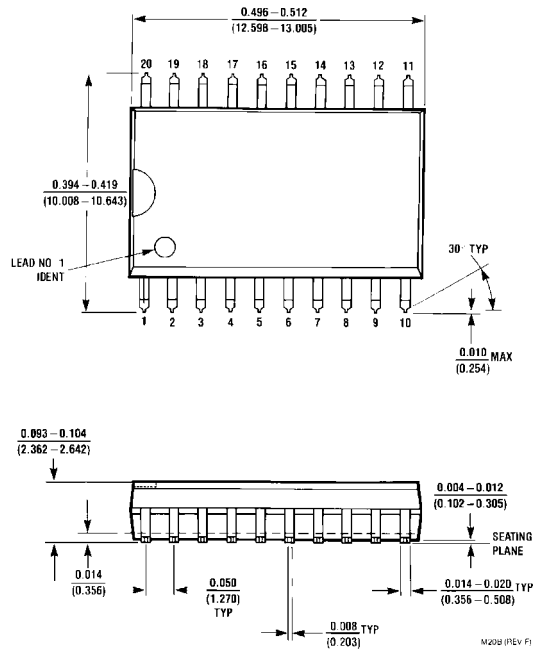
Symbol	Parameter	V _{CC} (V) (Note 9)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	5.0	2.0	4.5	7.0	2.0	7.5	ns
t _{PHL}	Data to Output		2.0	5.5	7.0	2.0	7.5	
t _{PZH}	Output Enable Time	5.0	2.0	5.0	9.0	2.0	9.5	ns
t _{PZL}			2.0	6.5	9.0	2.0	9.5	
t _{PHZ}	Output Disable Time	5.0	1.5	5.5	7.5	1.5	8.0	ns
t _{PLZ}			1.5	5.5	7.5	1.5	8.0	

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

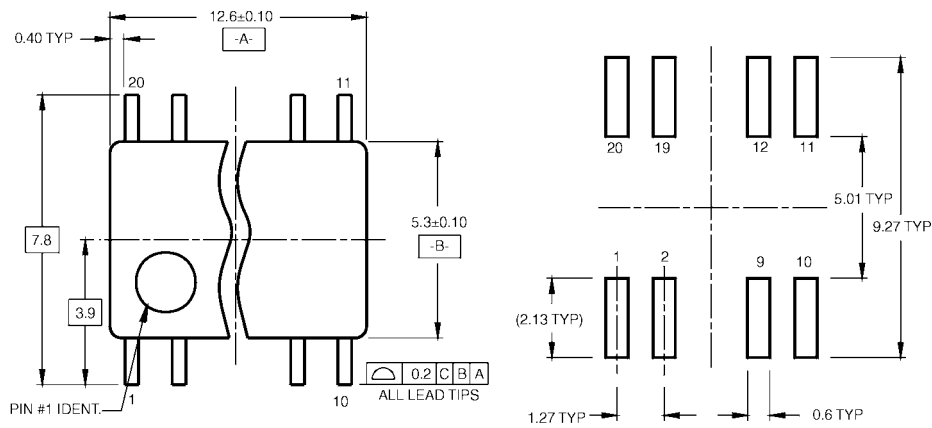
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance for AC	30.0	pF	V _{CC} = 5.0V
	Power Dissipation Capacitance for ACT	70.0		

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

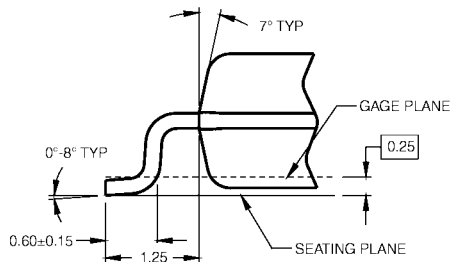
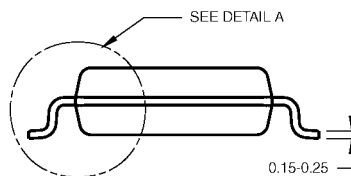
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



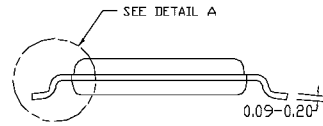
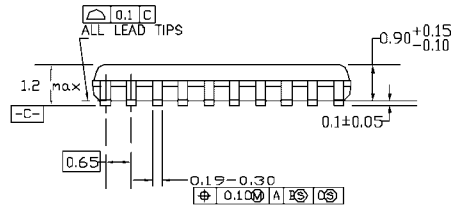
DETAIL A

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

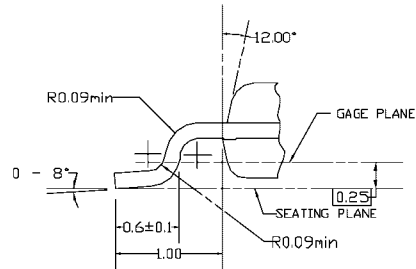
M20DRevB1

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

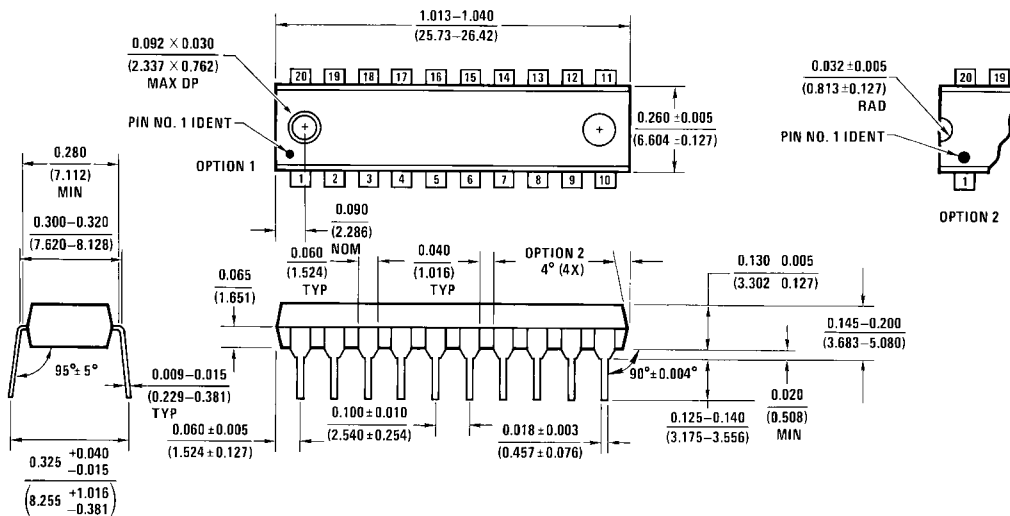
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N20A

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