

# 74ACT652 Transceiver/Register

## General Description

The ACT652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

## Features

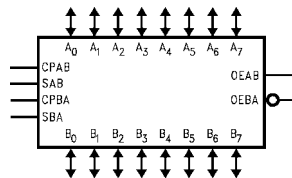
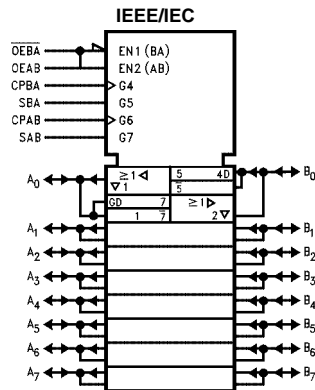
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Outputs source/sink 24 mA
- TTL-compatible inputs

## Ordering Code:

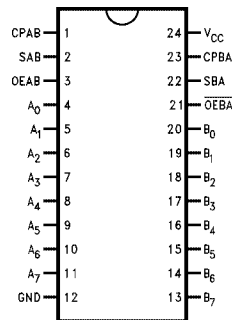
Order Number	Package Number	Package Description
74ACT652SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACT652MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT652SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

## Logic Symbols



## Connection Diagram



## Pin Descriptions

Pin Names	Description
A <sub>0</sub> -A <sub>7</sub> , B <sub>0</sub> -B <sub>7</sub>	A and B Inputs/3-STATE Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, OEBA	Output Enable Inputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

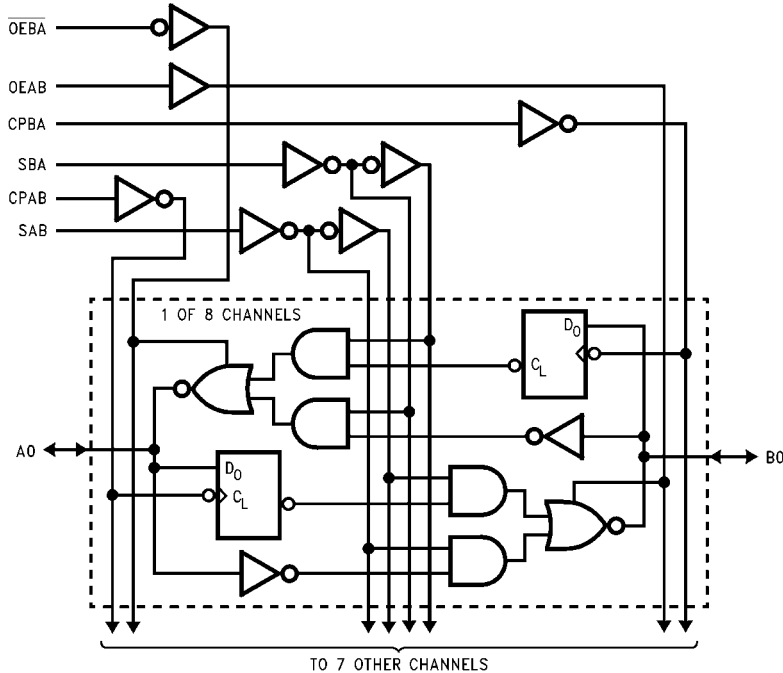
### Function Table

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A <sub>0</sub> thru A <sub>7</sub>	B <sub>0</sub> thru B <sub>7</sub>	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Clock Transition

**Note 1:** The data output functions may be enabled or disabled by various signals at OEAB or  $\overline{OEBA}$  inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

Data on the A or B data bus, or both can be stored in the internal D-type flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and  $\overline{\text{OEBA}}$ . In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

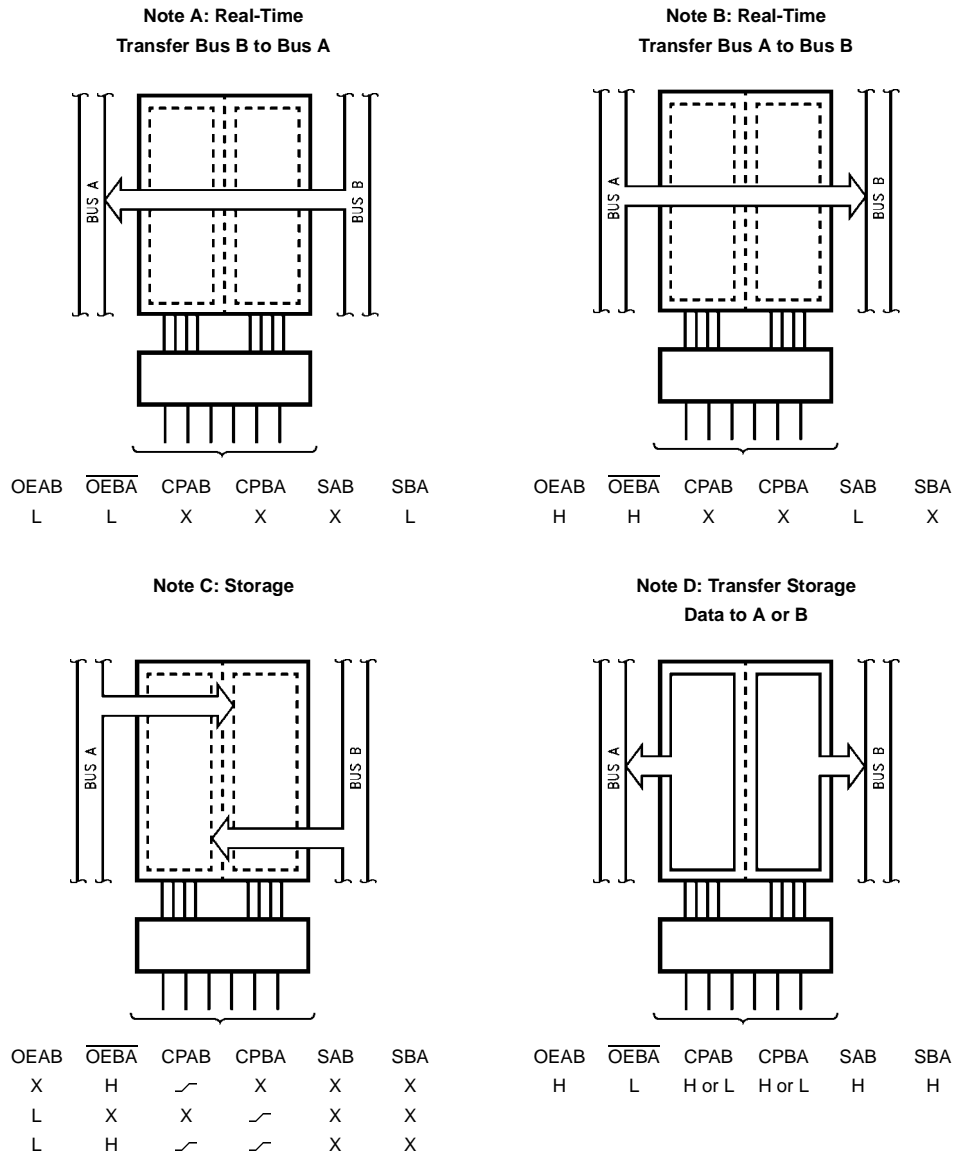


FIGURE 1.

**Absolute Maximum Ratings**(Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current	
per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source	
or Sink Current	$\pm 300$ mA
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0			
$V_{IL}$	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8			
$V_{OH}$	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4		V	$I_{OUT} = -50 \mu\text{A}$
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76			
		5.5		4.86	4.76			$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ (Note 3)
$V_{OL}$	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1		V	$I_{OUT} = 50 \mu\text{A}$
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44			
		5.5		0.36	0.44			$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ (Note 3)
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$		$\mu\text{A}$	$V_I = V_{CC}, \text{GND}$
$I_{OZT}$	Maximum I/O Leakage Current	5.5		$\pm 0.6$	$\pm 6.0$		$\mu\text{A}$	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$
$I_{CCT}$	Maximum $I_{CC}$ /Input	5.5	0.6		1.5		mA	$V_I = V_{CC} - 2.1V$
$I_{OLD}$	Minimum Dynamic	5.5			75		mA	$V_{OLD} = 1.65V \text{ Max}$
$I_{OHD}$	Output Current (Note 4)	5.5			-75		mA	$V_{OHD} = 3.85V \text{ Min}$
$I_{CC}$	Maximum Quiescent Supply Current	5.5		8.0	80.0		$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Max. Clock Frequency	5.0						MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Bus	5.0	2.0	7.0	9.5	2.0	10.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Bus to Bus	5.0	2.0	6.5	9.0	2.0	9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SBA or SAB to A or B	5.0	2.5	6.5	10.0	2.5	10.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Enable Time OEBA to A (Note 5)	5.0	2.0	7.0	10.5	2.0	11.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable Time OEBA to A (Note 5)	5.0	1.0	5.0	8.0	1.0	8.5	
t <sub>PZH</sub> t <sub>PZL</sub>	Enable Time OEAB to B	5.0	2.0	7.0	10.5	2.0	11.0	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable Time OEAB to B	5.0	1.0	5.0	8.0	1.0	8.5	ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW, Bus to Clock	5.0	3.0			3.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW, Bus to Clock	5.0	1.5			1.5		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	Clock Pulse Width HIGH or LOW	5.0	4.0			4.0		ns

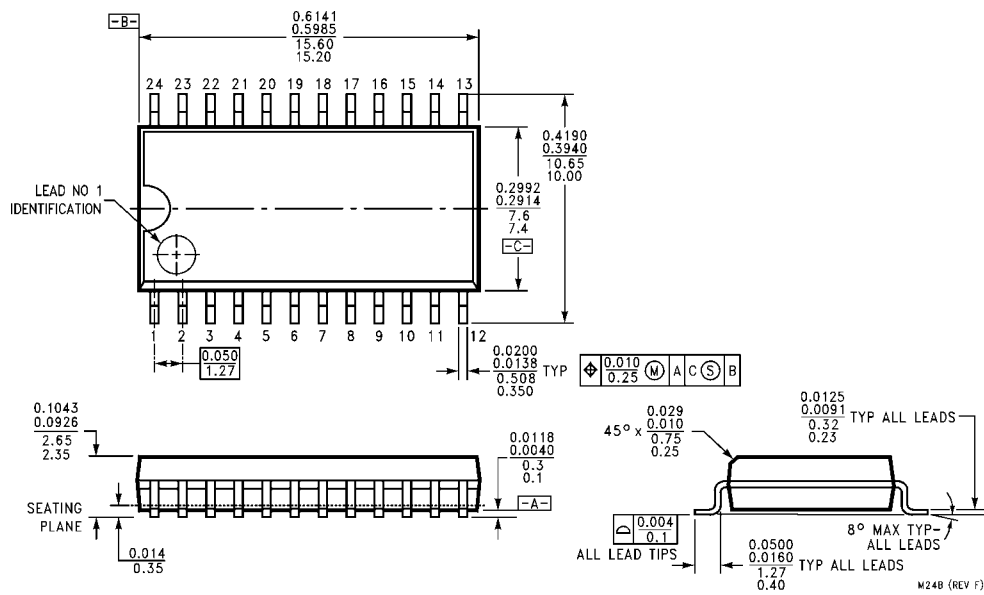
**Note 5:** Voltage Range 5.0 is 5.0V ± 0.5V.

### Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	54	pF	V <sub>CC</sub> = 5.0V

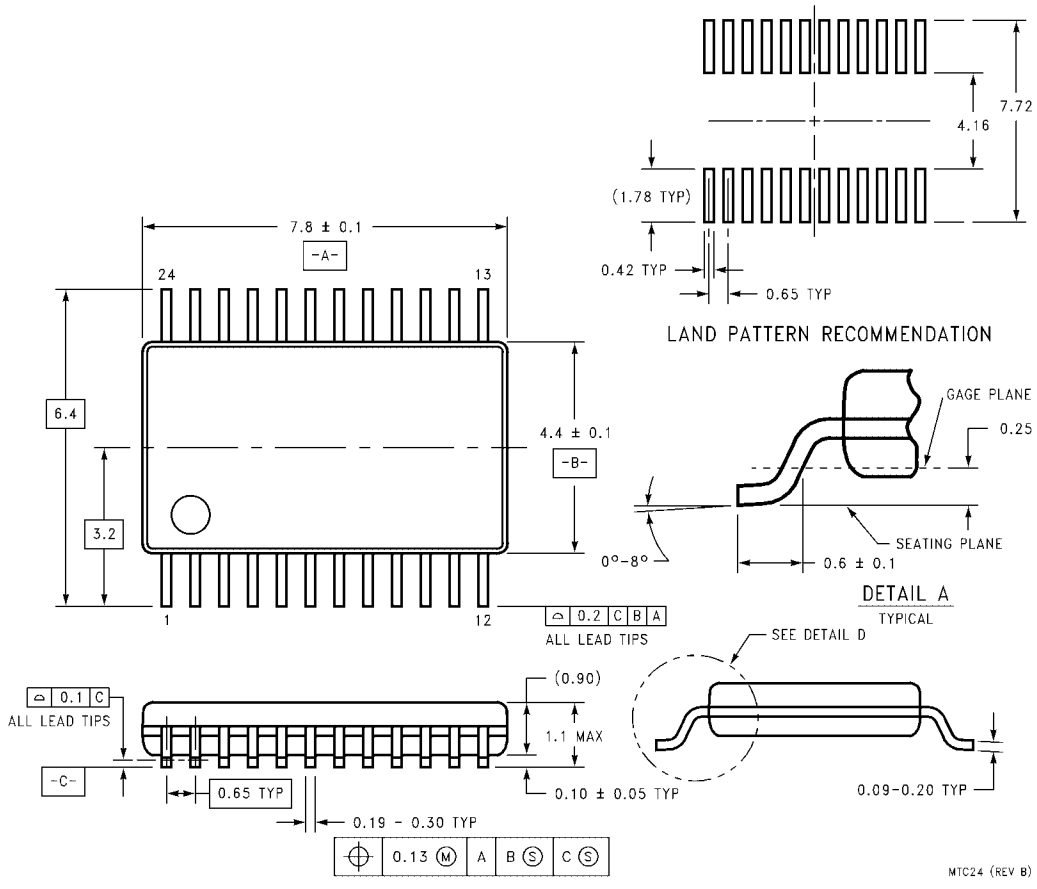
74ACT652

### Physical Dimensions inches (millimeters) unless otherwise noted



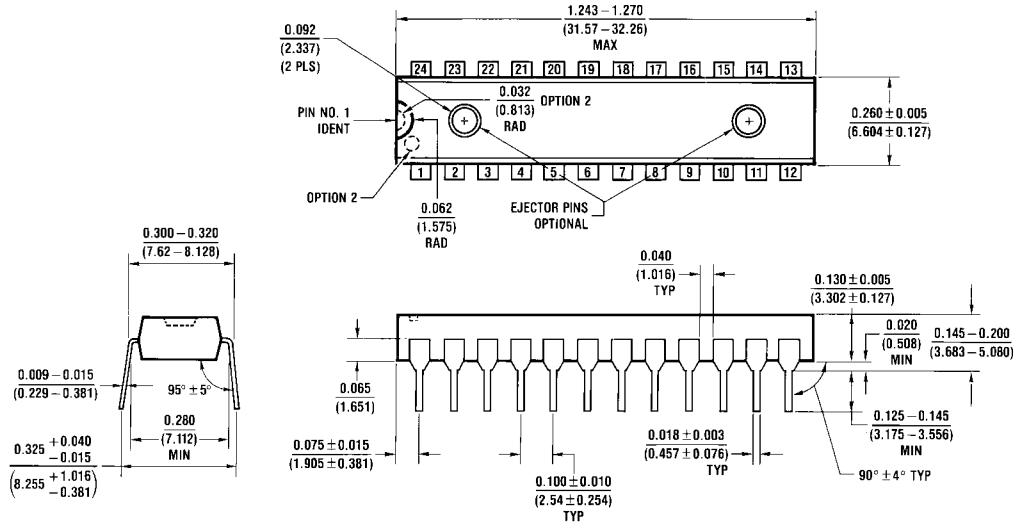
24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M24B

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC24**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)