

74F10

Triple 3-Input NAND Gate

General Description

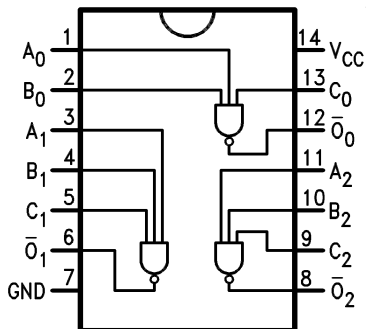
This device contains three independent gates, each of which performs the logic NAND function.

Ordering Information

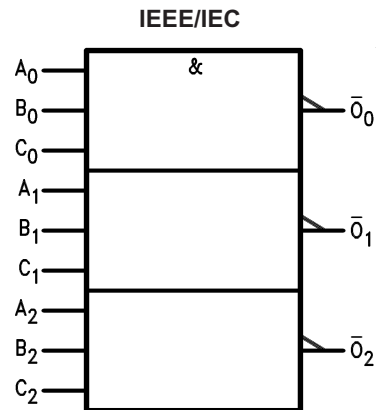
Order Number	Package Number	Package Description
74F10SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F10SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

Connection Diagram



Logic Symbol



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} , Output I_{OH}/I_{OL}
A_n, B_n, C_n	Inputs	1.0 / 1.0	20 μ A / -0.6mA
\bar{O}_n	Outputs	50 / 33.3	-1mA / 20mA

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T_{STG}	Storage Temperature	-65°C to $+150^{\circ}\text{C}$
T_A	Ambient Temperature Under Bias	-55°C to $+125^{\circ}\text{C}$
T_J	Junction Temperature Under Bias	-55°C to $+150^{\circ}\text{C}$
V_{CC}	V_{CC} Pin Potential to Ground Pin	-0.5V to $+7.0\text{V}$
V_{IN}	Input Voltage ⁽¹⁾	-0.5V to $+7.0\text{V}$
I_{IN}	Input Current ⁽¹⁾	-30mA to $+5.0\text{mA}$
V_O	Voltage Applied to Output in HIGH State (with $V_{CC} = 0\text{V}$)	
	Standard Output	-0.5V to V_{CC}
	3-STATE Output	-0.5V to 5.5V
	Current Applied to Output in LOW State (Max.)	twice the rated I_{OL} (mA)

Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T_A	Free Air Ambient Temperature	0°C to $+70^{\circ}\text{C}$
V_{CC}	Supply Voltage	$+4.5\text{V}$ to $+5.5\text{V}$

DC Electrical Characteristics

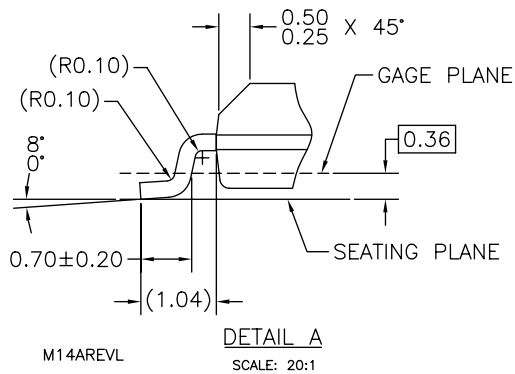
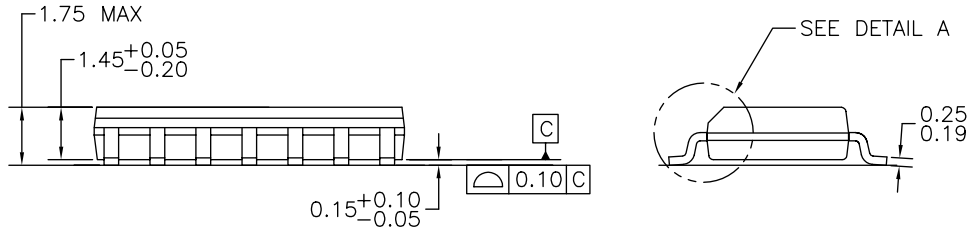
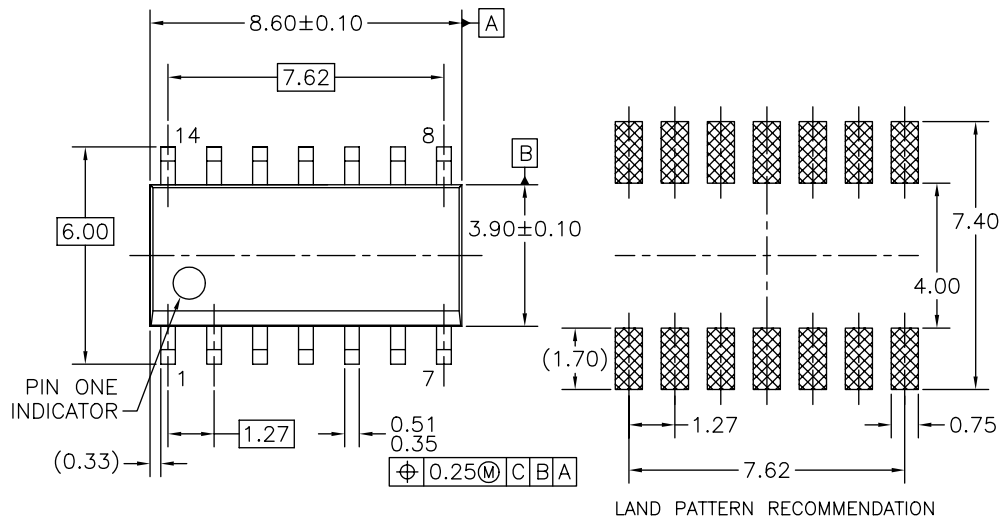
Symbol	Parameter		V _{CC}	Conditions	Min.	Typ.	Max.	Units
V _{IH}	Input HIGH Voltage			Recognized as a HIGH Signal	2.0			V
V _{IL}	Input LOW Voltage			Recognized as a LOW Signal			0.8	V
V _{CD}	Input Clamp Diode Voltage		Min.	I _{IN} = -18mA			-1.2	V
V _{OH}	Output HIGH Voltage	10% V _{CC}	Min.	I _{OH} = -1mA	2.5			V
		5% V _{CC}		I _{OH} = -1mA	2.7			
V _{OL}	Output LOW Voltage	10% V _{CC}	Min.	I _{OL} = 20mA			0.5	V
I _{IH}	Input HIGH Current		Max.	V _{IN} = 2.7V			5.0	μA
I _{BVI}	Input HIGH Current Breakdown Test		Max.	V _{IN} = 7.0V			7.0	μA
I _{CEx}	Output HIGH Leakage Current		Max.	V _{OUT} = V _{CC}			50	μA
V _{ID}	Input Leakage Test		0.0	I _{ID} = 1.9μA, All other pins grounded	4.75			V
I _{OD}	Output Leakage Circuit Current		0.0	V _{IOD} = 150mV, All other pins grounded			3.75	μA
I _{IL}	Input LOW Current		Max.	V _{IN} = 0.5V			-0.6	mA
I _{OS}	Output Short-Circuit Current		Max.	V _{OUT} = 0V	-60		-150	mA
I _{CCH}	Power Supply Current		Max.	V _O = HIGH		1.4	2.1	mA
I _{CCL}	Power Supply Current		Max.	V _O = LOW		5.1	7.7	mA

AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C, V _{CC} = +5.0V, C _L = 50pF			T _A = -55°C to +125°C, V _{CC} = +5.0V, C _L = 50 pF		T _A = 0°C to +70°C, V _{CC} = +5.0V, C _L = 50pF		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay, A _n , B _n , C _n to \overline{O}_n	2.4	3.7	5.0	2.0	7.0	2.4	6.0	ns
t _{PHL}		1.5	3.2	4.3	1.5	6.5	1.5	5.3	

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



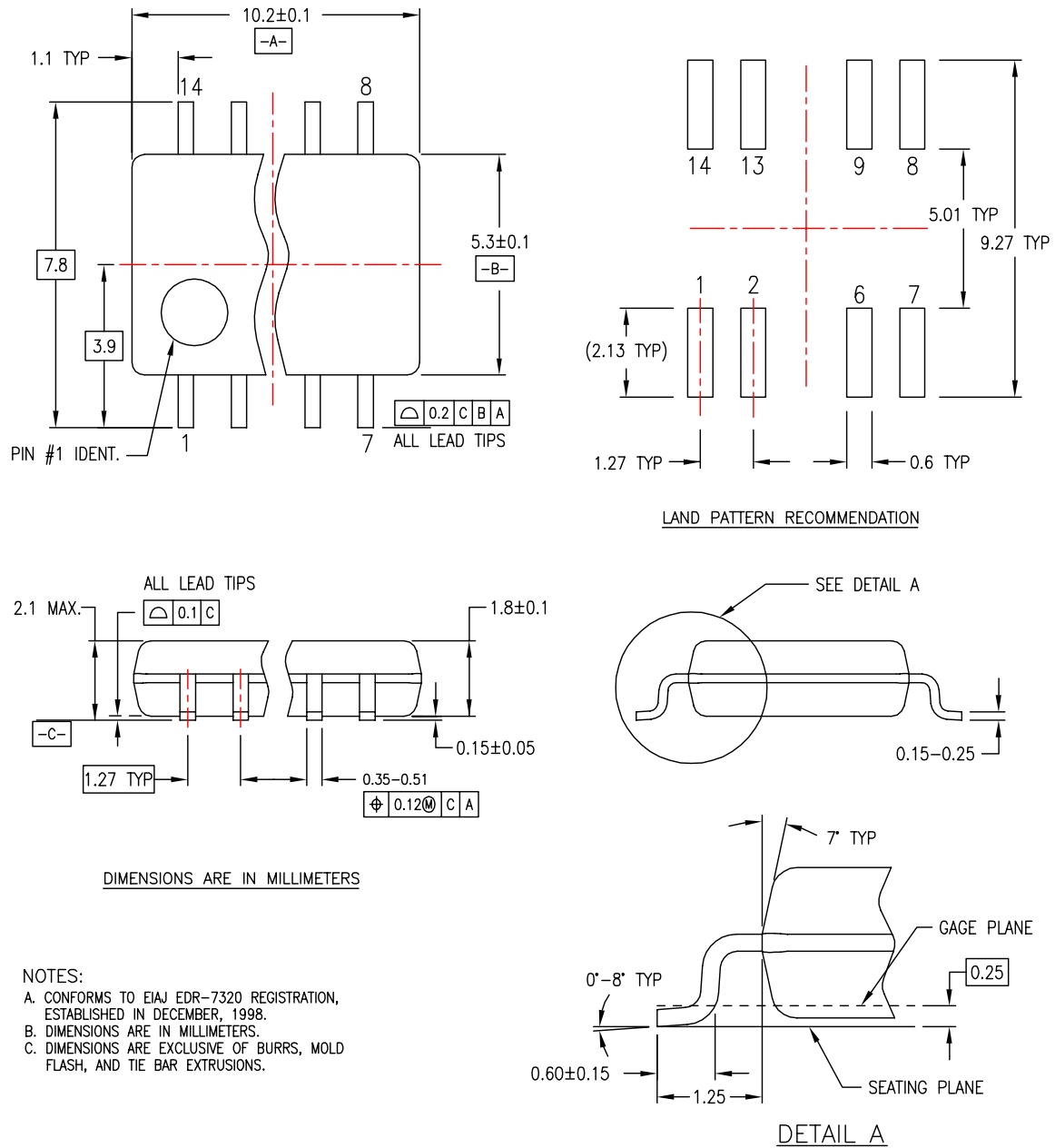
NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.


M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D



TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx [®]	<i>i-Lo</i> [™]	Power-SPM [™]	TinyBoost [™]
Across the board. Around the world. [™]	ImpliedDisconnect [™]	PowerTrench [®]	TinyBuck [™]
ActiveArray [™]	IntelliMAX [™]	Programmable Active Droop [™]	TinyLogic [®]
Bottomless [™]	ISOPLANAR [™]	QFET [®]	TINYOPTO [™]
Build it Now [™]	MICROCOUPLER [™]	QS [™]	TinyPower [™]
CoolFET [™]	MicroPak [™]	QT Optoelectronics [™]	TinyWire [™]
CROSSVOLT [™]	MICROWIRE [™]	Quiet Series [™]	TruTranslation [™]
CTL [™]	Motion-SPM [™]	RapidConfigure [™]	μSerDes [™]
Current Transfer Logic [™]	MSX [™]	RapidConnect [™]	UHC [®]
DOME [™]	MSXPro [™]	ScalarPump [™]	UniFET [™]
E ² CMOS [™]	OCX [™]	SMART START [™]	VCX [™]
EcoSPARK [®]	OCXPro [™]	SPM [®]	Wire [™]
EnSigna [™]	OPTOLOGIC [®]	STEALTH [™]	
FACT Quiet Series [™]	OPTOPLANAR [®]	SuperFET [™]	
FACT [®]	PACMAN [™]	SuperSOT [™] -3	
FAST [®]	PDP-SPM [™]	SuperSOT [™] -6	
FASTr [™]	POP [™]	SuperSOT [™] -8	
FPS [™]	Power220 [®]	SyncFET [™]	
FRFET [®]	Power247 [®]	TCM [™]	
GlobalOptoisolator [™]	PowerEdge [™]	The Power Franchise [®]	
GTO [™]	PowerSaver [™]		
HiSeC [™]			

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. 126