

April 1988 Revised March 1999

74F151A 8-Input Multiplexer

General Description

The F151A is a high-speed 8-input digital multiplexer. It provides in one package the ability to select one line of data from up to eight sources. The F151A can be used as a

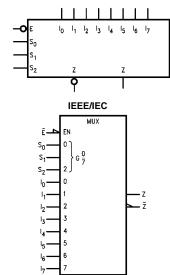
universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

Ordering Code:

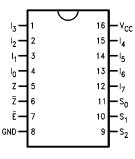
| Order Number | Package Number | Package Description | | | | | |
|--------------|----------------|---|--|--|--|--|--|
| 74F151ASC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow | | | | | |
| 74F151ASJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide | | | | | |
| 74F151APC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide | | | | | |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

| Pin Names | | U.L. | Input I _{IH} /I _{IL} | |
|--------------------------------|---------------------------|----------|---|--|
| | Description | HIGH/LOW | Output I _{OH} /I _{OL} | |
| I ₀ –I ₇ | Data Inputs | 1.0/1.0 | 20 μA/-0.6 mA | |
| S ₀ -S ₂ | Select Inputs | 1.0/1.0 | 20 μA/-0.6 mA | |
| Ē | Enable Input (Active LOW) | 1.0/1.0 | 20 μA/–0.6 mA | |
| Z | Data Output | 50/33.3 | –1 mA/20 mA | |
| Z | Inverted Data Output | 50/33.3 | −1 mA/20 mA | |

Functional Description

The F151A is a logic implementation of a single pole, 8position switch with the switch position controlled by the state of three Select inputs, S₀, S₁, S₂. Both assertion and negation outputs are provided. The Enable input (\overline{E}) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$\begin{split} Z &= \overline{E} \bullet (I_0 \ \overline{S}_2 \ \overline{S}_1 \ \overline{S}_0 + I_1 \ \overline{S}_2 \ \overline{S}_1 \ S_0 + I_2 \ \overline{S}_2 \ S_1 \ \overline{S}_0 + \\ I_3 \ \overline{S}_2 \ S_1 \ S_0 + I_4 \ S_2 \ \overline{S}_1 \ \overline{S}_0 + I_5 \ S_2 \ \overline{S}_1 \ S_0 + \\ I_6 \ S_2 \ S_1 \ \overline{S}_0 + I_7 \ S_2 \ S_1 \ S_0) \end{split}$$

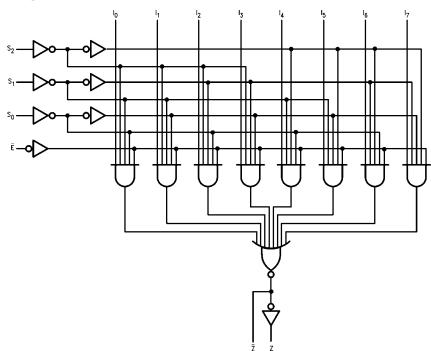
The F151A provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the F151A can provide any logic function of four variables and its negation.

Truth Table

| | Inj | Out | puts | | |
|---|----------------|----------------|----------------|----------------|----------------|
| Ē | S ₂ | S ₁ | S ₀ | Z | z |
| Н | Х | Х | Х | Н | L |
| L | L | L | L | Ī ₀ | I ₀ |
| L | L | L | Н | Ī ₁ | I ₁ |
| L | L | Н | L | Ī ₂ | l ₂ |
| | | | | | |
| L | L | Н | Н | Ī ₃ | I ₃ |
| L | Н | L | L | Ī ₄ | I ₄ |
| L | Н | L | Н | Ī ₅ | I ₅ |
| L | Н | Н | L | Ī ₆ | I ₆ |
| L | Н | Н | Н | Ī ₇ | I ₇ |

H = HIGH Voltage Level L = LOW Voltage Level

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

X = Immaterial

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

 $\begin{array}{ll} \mbox{Storage Temperature} & -65\mbox{°C to } +150\mbox{°C} \\ \mbox{Ambient Temperature under Bias} & -55\mbox{°C to } +125\mbox{°C} \\ \end{array}$

Junction Temperature under Bias —55°C to +175°C

Plastic -55°C to +150°C

V_{CC} Pin Potential to

 $\begin{array}{lll} \mbox{Ground Pin} & -0.5\mbox{V to } +7.0\mbox{V} \\ \mbox{Input Voltage (Note 2)} & -0.5\mbox{V to } +7.0\mbox{V} \\ \mbox{Input Current (Note 2)} & -30\mbox{ mA to } +5.0\mbox{ mA} \\ \end{array}$

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC} 3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) $\qquad \qquad \text{twice the rated I}_{\text{OL}} \, (\text{mA})$

Free Air Ambient Temperature 0°C to +70°C Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation

under these conditions is not implied.

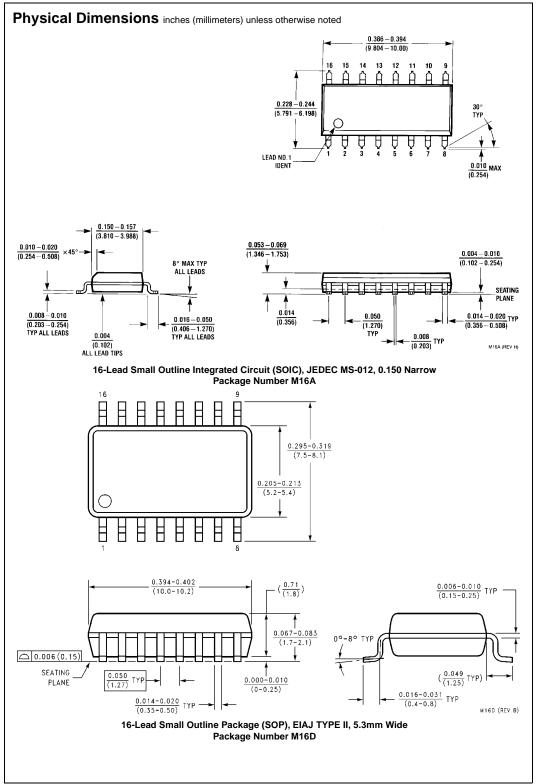
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | | Min | Тур | Max | Units | V _{CC} | Conditions | |
|------------------|------------------------------|--------------------|------|------|------|-------|-----------------|-----------------------------|--|
| V _{IH} | Input HIGH Voltage | | 2.0 | | | V | | Recognized as a HIGH Signal | |
| V _{IL} | Input LOW Voltage | | | | 0.8 | V | | Recognized as a LOW Signal | |
| V _{CD} | Input Clamp Diode Voltage | | | | -1.2 | V | Min | I _{IN} = -18 mA | |
| V _{OH} | Output HIGH 10 | 0% V _{CC} | 2.5 | | | V | Min | I _{OH} = -1 mA | |
| | Voltage 59 | % V _{CC} | 2.7 | | | V | IVIIN | $I_{OH} = -1 \text{ mA}$ | |
| V _{OL} | Output LOW | | | | | | | | |
| | Voltage 10 | 0% V _{CC} | | | 0.5 | V | Min | I _{OL} = 20 mA | |
| I _{IH} | Input HIGH | | | | | | | | |
| | Current | | | | 5.0 | μΑ | Max | $V_{IN} = 2.7V$ | |
| I _{BVI} | Input HIGH Current | | | | | | | | |
| | Breakdown Test | | | | 7.0 | μΑ | Max | $V_{IN} = 7.0V$ | |
| I _{CEX} | Output HIGH | | | | | | | | |
| | Leakage Current | | | | 50 | μΑ | Max | $V_{OUT} = V_{CC}$ | |
| V _{ID} | Input Leakage | | 4.75 | | | V | 0.0 | $I_{ID} = 1.9 \mu A$ | |
| | Test | | | | | | | All Other Pins Grounded | |
| I _{OD} | Output Leakage | | | | 3.75 | μΑ | 0.0 | V _{IOD} = 150 mV | |
| | Circuit Current | | | | | | | All Other Pins Grounded | |
| I _{IL} | Input LOW Current | | | | -0.6 | mA | Max | $V_{IN} = 0.5V$ | |
| Ios | Output Short-Circuit Current | | -60 | | -150 | mA | Max | V _{OUT} = 0V | |
| I _{CC} | Power Supply Current | | | 13.5 | 21.0 | mA | Max | $V_{O} = HIGH$ | |

AC Electrical Characteristics

| Symbol | Parameter | | $T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$ | | | $T_A = 0^{\circ}C$ to $+70^{\circ}C$ $C_L = 50 \text{ pF}$ | |
|------------------|-------------------------|-----|---|------|-----|--|-----|
| | | Min | Тур | Max | Min | Max | |
| t _{PLH} | Propagation Delay | 4.0 | 6.2 | 9.0 | 3.5 | 9.5 | |
| t _{PHL} | S_n to \overline{Z} | 3.2 | 5.2 | 7.5 | 3.2 | 7.5 | ns |
| t _{PLH} | Propagation Delay | 4.5 | 7.5 | 10.5 | 4.5 | 12.0 | ns |
| t _{PHL} | S _n to Z | 4.0 | 6.2 | 9.0 | 4.0 | 9.0 | 115 |
| t _{PLH} | Propagation Delay | 3.0 | 4.7 | 6.1 | 3.0 | 7.0 | ns |
| t _{PHL} | E to Z | 3.0 | 4.4 | 6.0 | 2.5 | 6.0 | |
| t _{PLH} | Propagation Delay | 5.0 | 7.0 | 9.5 | 4.0 | 10.5 | ns |
| t _{PHL} | E to Z | 3.5 | 5.3 | 7.0 | 3.0 | 7.5 | |
| t _{PLH} | Propagation Delay | 3.0 | 4.8 | 6.5 | 3.0 | 7.0 | ns |
| t _{PHL} | I_n to \overline{Z} | 1.5 | 2.5 | 4.0 | 1.5 | 5.0 | |
| t _{PLH} | Propagation Delay | 3.0 | 4.8 | 6.5 | 2.5 | 7.5 | ns |
| t _{PHL} | I _n to Z | 3.7 | 5.5 | 7.0 | 3.7 | 7.5 | |



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.780 0.090 (18.80 - 19.81)(2.286)**16 15 14 13 12 11 10 9** 16 T5 F INDEX AREA 0.250 ± 0.010 $\overline{(6.350 \pm 0.254)}$ PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 8 1 2 OPTION 01 OPTION 02 $\frac{0.065}{(1.651)}$ $\frac{0.130 \pm 0.005}{(3.302 \pm 0.127)}$ $\frac{0.060}{(1.524)}$ TYP 4° TYP 0.300 - 0.320OPTIONAL (7.620 - 8.128)0.145 - 0.200 $\overline{(3.683 - 5.080)}$ 95°±5° 0.008 = 0.016 (0.203 = 0.406) TYP 0.020 0.280 (7.112) (0.508)0.125 - 0.150 (3.175 - 3.810) 0.030 ± 0.015 (0.762 ± 0.381) 0.014 = 0.023 (0.356 = 0.584) $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)}$ (0.325 +0.040 -0.015 0.050 ± 0.010 N16E (REV F) TYP (1.270 ± 0.254)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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