FAIRCHILD SEMICONDUCTOR™

April 1988
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74F191
Up/Down Binary Counter with Preset and Ripple Clock

General Description

The 74F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 74F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

Features

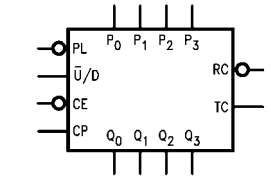
- High-Speed—125 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable

Ordering Code:

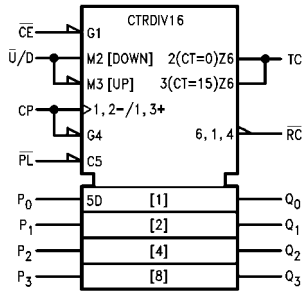
Order Number	Package Number	Package Description
74F191SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F191SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F191PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

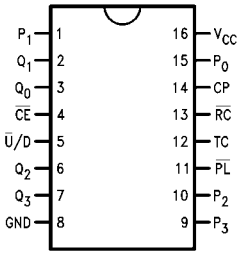
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{CE}$	Count Enable Input (Active LOW)	1.0/3.0	20 µA/–1.8 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{U}$/D	Up/Down Count Control Input	1.0/1.0	20 µA/–0.6 mA
Q_0–Q_3	Flip-Flop Outputs	50/33.3	–1 mA/20 mA
$\overline{RC}$	Ripple Clock Output (Active LOW)	50/33.3	–1 mA/20 mA
TC	Terminal Count Output (Active HIGH)	50/33.3	–1 mA/20 mA

Functional Description

The 74F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figure 1 and Figure 2. In Figure 1, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure 2. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure 3 avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figure 1 and Figure 2 doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

Mode Select Table

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ Truth Table

Inputs			Output
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⌐‾⌐	⌐‾⌐
H	X	X	H
X	L	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
⌐‾⌐ = LOW Pulse

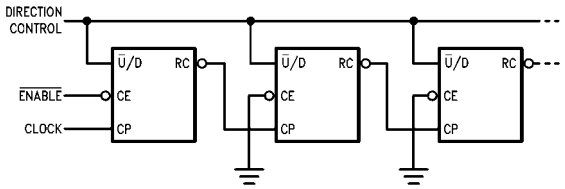


FIGURE 1. n-Stage Counter Using Ripple Clock

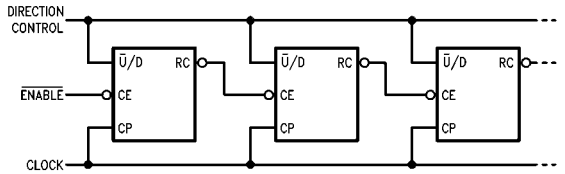


FIGURE 2. Synchronous n-Stage Counter Using Ripple Carry/Borrow

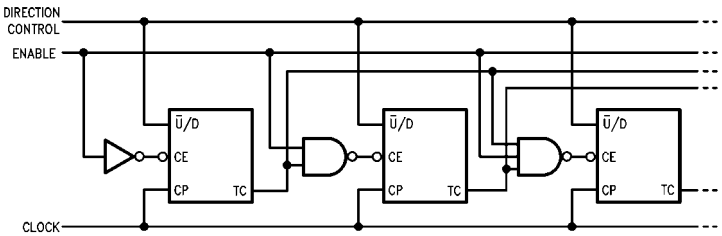
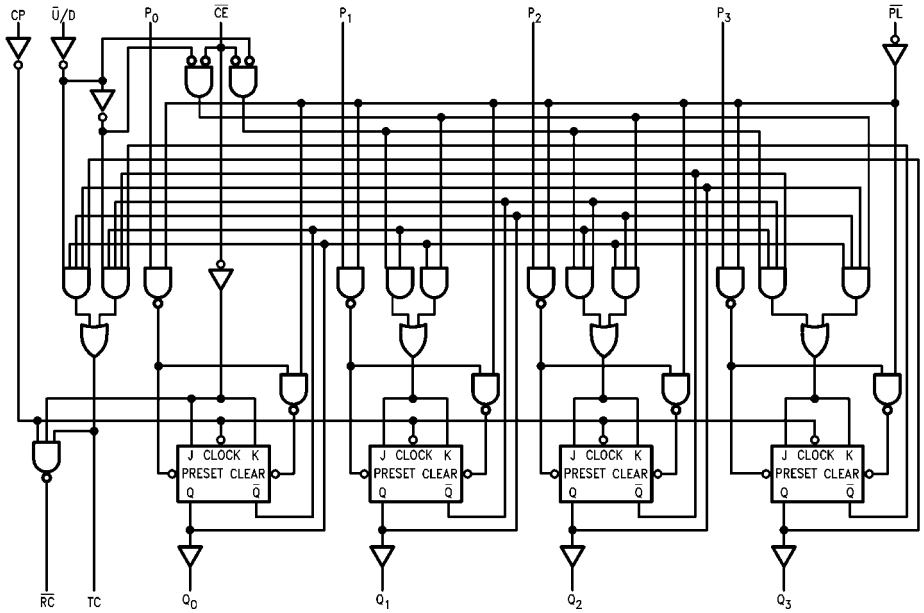


FIGURE 3. Synchronous n-Stage Counter with Gated Carry/Borrow

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
	Voltage 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW 10% V_{CC} Voltage			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current			5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA, All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current			3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current			−0.6	mA	Max	V_{IN} = 0.5V (except $\overline{CE}$)
				−1.8			V_{IN} = 0.5V ($\overline{CE}$)
I_{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current		38	55	mA	Max	

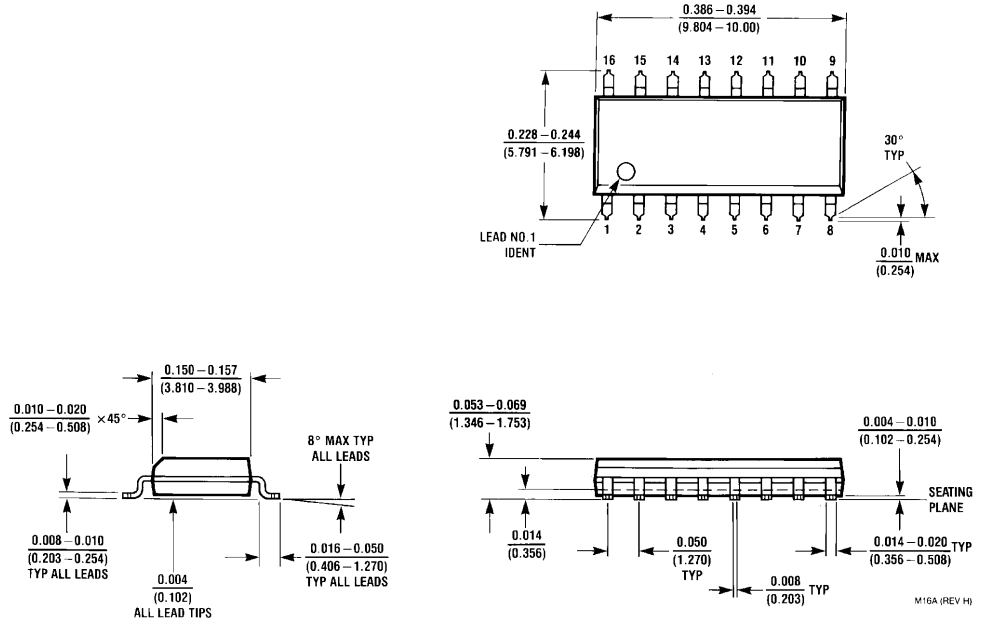
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Count Frequency	100	125		75		90		MHz
t_{PLH}	Propagation Delay	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns
t_{PHL}	CP to Q_n	5.0	8.5	11.0	5.0	13.5	5.0	12.0	
t_{PLH}	Propagation Delay	6.0	10.0	13.0	6.0	16.5	6.0	14.0	
t_{PHL}	CP to TC	5.0	8.5	11.0	5.0	13.5	5.0	12.0	
t_{PLH}	Propagation Delay	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns
t_{PHL}	CP to $\overline{RC}$	3.0	5.0	7.0	3.0	9.0	3.0	8.0	
t_{PLH}	Propagation Delay	3.0	5.0	7.0	3.0	9.0	3.0	8.0	
t_{PHL}	$\overline{CE}$ to $\overline{RC}$	3.0	5.5	7.0	3.0	9.0	3.0	8.0	
t_{PLH}	Propagation Delay	7.0	11.0	18.0	7.0	22.0	7.0	20.0	ns
t_{PHL}	$\overline{U}$/D to $\overline{RC}$	5.5	9.0	12.0	5.5	14.0	5.5	13.0	
t_{PLH}	Propagation Delay	4.0	7.0	10.0	4.0	13.5	4.0	11.0	
t_{PHL}	$\overline{U}$/D to TC	4.0	6.5	10.0	4.0	12.5	4.0	11.0	
t_{PLH}	Propagation Delay	3.0	4.5	7.0	3.0	9.0	3.0	8.0	ns
t_{PHL}	P_n to Q_n	6.0	10.0	13.0	6.0	16.0	6.0	14.0	
t_{PLH}	Propagation Delay	5.0	8.5	11.0	5.0	13.0	5.0	12.0	ns
t_{PHL}	$\overline{PL}$ to Q_n	5.5	9.0	12.0	5.5	14.5	5.5	13.0	
t_{PLH}	Propagation Delay	5.0		14.0			5.0	15.0	ns
t_{PHL}	P_n to TC	6.5		13.0			6.0	14.0	
t_{PLH}	Propagation Delay	6.5		19.0			6.5	20.0	ns
t_{PHL}	P_n to $\overline{RC}$	6.0		14.0			6.0	15.0	
t_{PLH}	Propagation Delay	8.0		16.5			8.0	17.5	ns
t_{PHL}	$\overline{PL}$ to TC	6.0		13.5			6.0	14.5	
t_{PLH}	Propagation Delay	10.0		20.0			10.0	21.0	ns
t_{PHL}	$\overline{PL}$ to $\overline{RC}$	9.0		15.5			9.0	16.0	

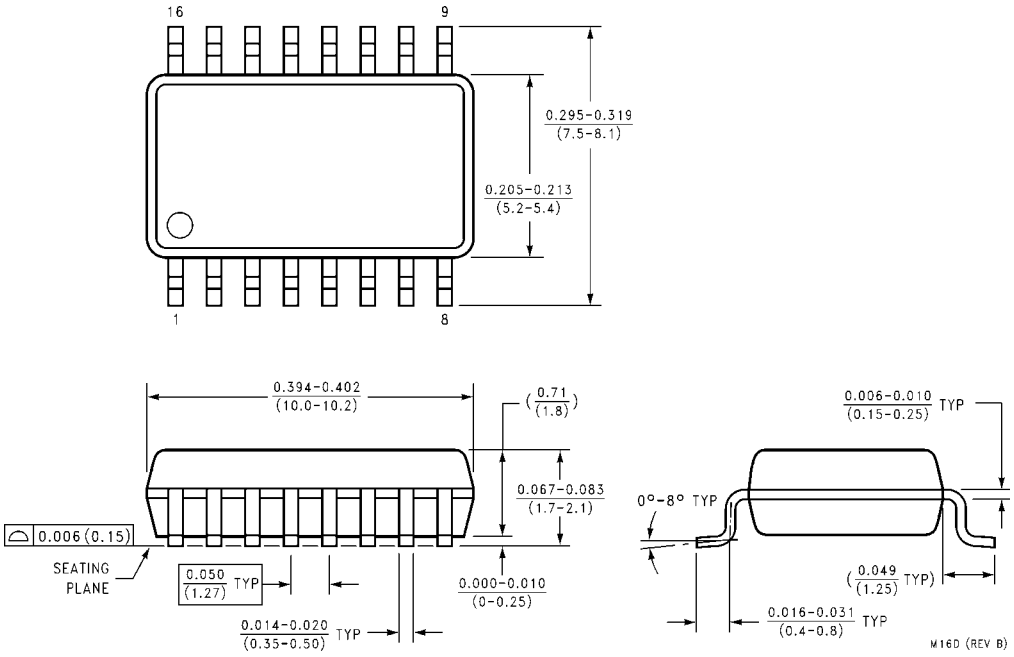
AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.5		6.0		5.0		ns
$t_S(L)$	P_n to $\overline{PL}$	4.5		6.0		5.0		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0		
$t_H(L)$	P_n to $\overline{PL}$	2.0		2.0		2.0		
$t_S(L)$	Setup Time LOW	10.0		10.5		10.0		ns
	$\overline{CE}$ to CP							
$t_H(L)$	Hold Time LOW	0		0		0		
	$\overline{CE}$ to CP							
$t_S(H)$	Setup Time, HIGH or LOW	12.0		12.0		12.0		ns
$t_S(L)$	$\overline{U}$/D to CP	12.0		12.0		12.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		0		
$t_H(L)$	$\overline{U}$/D to CP	0		0		0		
$t_W(L)$	$\overline{PL}$ Pulse Width LOW	6.0		8.5		6.0		ns
$t_W(L)$	CP Pulse Width LOW	5.0		7.0		5.0		ns
t_{REC}	Recovery Time	6.0		7.5		6.0		ns
	$\overline{PL}$ to CP							

Physical Dimensions inches (millimeters) unless otherwise noted

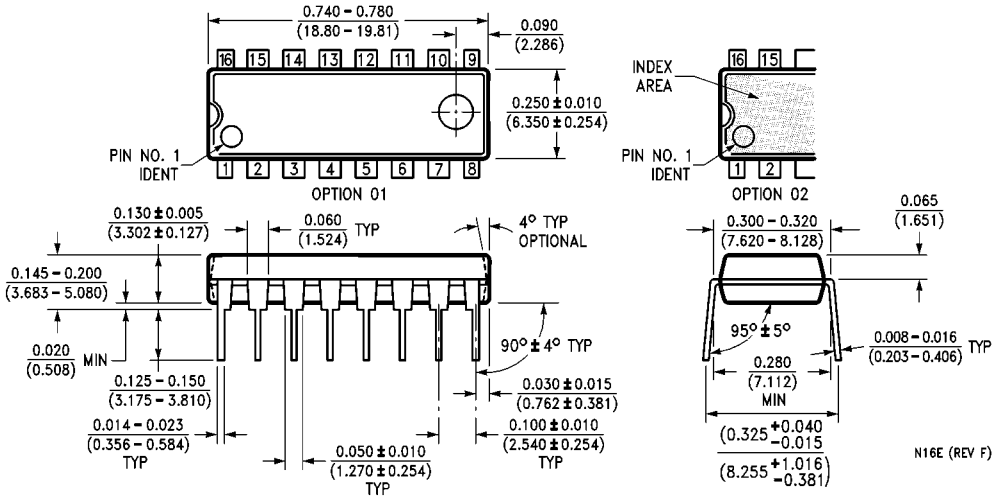


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E