DATA SHEET

74F524

8-bit register comparator (open-collector + 3-State)

Product specification

1990 Aug 07

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

8-bit register comparator (open collector + 3-State) 74F524

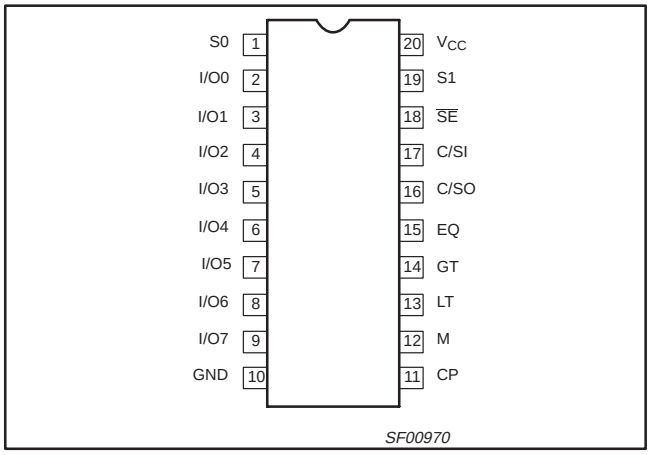
FEATURES

- 8-Bit bidirectional register with bus-oriented input-output
- Independent serial input-output to register
- Register bus comparator with ‘equal to’, ‘greater than’ and ‘less than’ outputs
- Cascadable in groups of 8-bits
- Open collector comparator outputs for AND-wired expansion
- Two’s complement or magnitude compare

DESCRIPTION

The 74F524 is an 8-bit bidirectional register with parallel input and output, plus serial input and output progressing from MSB to LSB. All data inputs, serial and parallel, are loaded by the rising edge of the clock. The device functions are controlled by two control lines (S0, S1) to execute shift, load, hold and read out. An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-High, open collector outputs representing ‘register equal to bus’, ‘register greater than bus’ and ‘register less than bus’ are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow Two’s Complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F524	65MHz	110mA

ORDERING INFORMATION

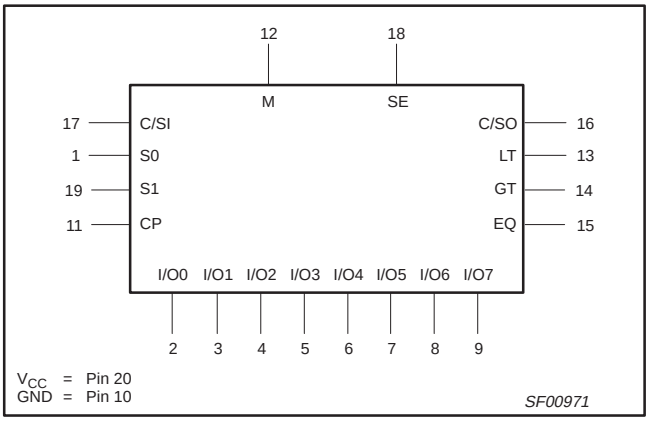
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F524N	SOT146-1
20-pin plastic SOL	N74F524D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

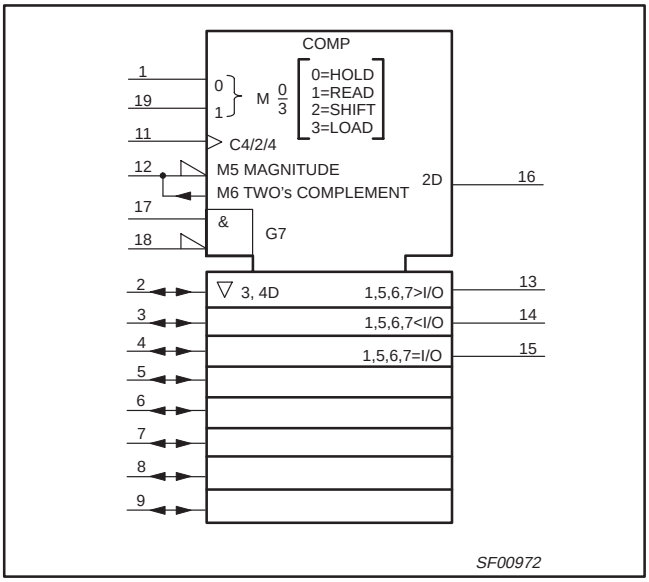
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/On	Parallel data inputs	3.5/1.0	70µA/0.6mA
S0, S1	Mode select inputs	1.0/1.0	20µA/0.6mA
C/SI	Status priority or serial data input	1.0/1.0	20µA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SE}$	Status enable input (active Low)	1.0/1.0	20µA/0.6mA
M	Compare mode select input	1.0/1.0	20µA/0.6mA
I/On	3-state parallel data outputs	150/40	3.0mA/24mA
C/SO	Status priority or serial data output	50/33	1.0mA/20mA
LT	Register less than bus output	OC/33	OC/20mA
EQ	Register equal to bus output	OC/33	OC/20mA
GT	Register greater than bus output	OC/33	OC/20mA

NOTE:
One (1.0) FAST Unit Load (U.L.) is defined as 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

LOGIC SYMBOL for 74F456



LOGIC SYMBOL (IEEE/IEC) for 74F456



FUNCTIONAL DESCRIPTION

The 74F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus I/O0–I/O7. Serial data is loaded into the register from the C/SI input and may be shifted through the register and out through the C/SO output. Both parallel and serial data entry occurs on the rising edge of the clock (CP). The operation of the shift register is controlled by two signals, S0 and S1, according to the Select Function Table. The 3-State parallel output buffers are enabled only in the READ mode.

SELECT FUNCTION TABLE

S0	S1	OPERATION
L	L	HOLD–Retains data in shift register
L	H	READ–Read contents in register onto data bus
H	L	SHIFT–Allows serial shifting on next rising clock edge
H	H	LOAD–Load data on bus into register

H = High voltage level
L = Low voltage level

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF Open Collector outputs indicate whether the contents held in the shift register are ‘greater than’ (GT). ‘less than’ (LT), or ‘equal to’ (EQ) the data on the input bus. A High signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A mode control (M) input allows selection between a straightforward magnitude compare or a comparison between Two’s complement numbers.

NUMBER REPRESENTATION SELECT TABLE

M	OPERATION
L	Magnitude compare
H	Two’s Complement compare

H = High voltage level
L = Low voltage level

For ‘greater than’ or ‘less than’ detection, the C/SI input must be held High, as indicated in the Function Table. The internal logic is arranged such that a Low signal on the C/SI input places the ‘greater than’ and ‘less than’ outputs in their off state. (Note that this off state serves also as the active state when C/SI is High. It is intended for use in expansion to word lengths greater than 8 bits using multiple 74S524s as explained in the next 3 paragraphs.) The C/SO output will be forced High if the ‘equal to’ status condition exists; otherwise, C/SO will be held Low.

Word length expansion (in groups of 8 bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see Application Figure 1). The CS/I input of the most significant device is held High while the $\overline{SE}$ input of the least significant device is held Low. The corresponding status outputs are AND-wired together. In the case of two’s complement number compare, only the Mode input to the most significant device should be High. the Mode inputs to all other cascaded devices are held Low.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, then the EQ and LT outputs will be pulled Low, whereas the GT output will float High. Also, the

CS/O output of the most significant device will be forced Low, disabling the subsequent devices but enabling its own status outputs. The corrected status condition is thus indicated. The same applies if the register byte is less than the data byte, only in this case the EQ and GT outputs go Low, whereas the LT output floats High.

If an equality condition is detected in the most significant device, its C/SO output is forced High. This enables the next less significant device and disables its own status outputs. In this way, the status output proximity is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving 'n' cascaded 74F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35+6(n–2) ns.

APPLICATION

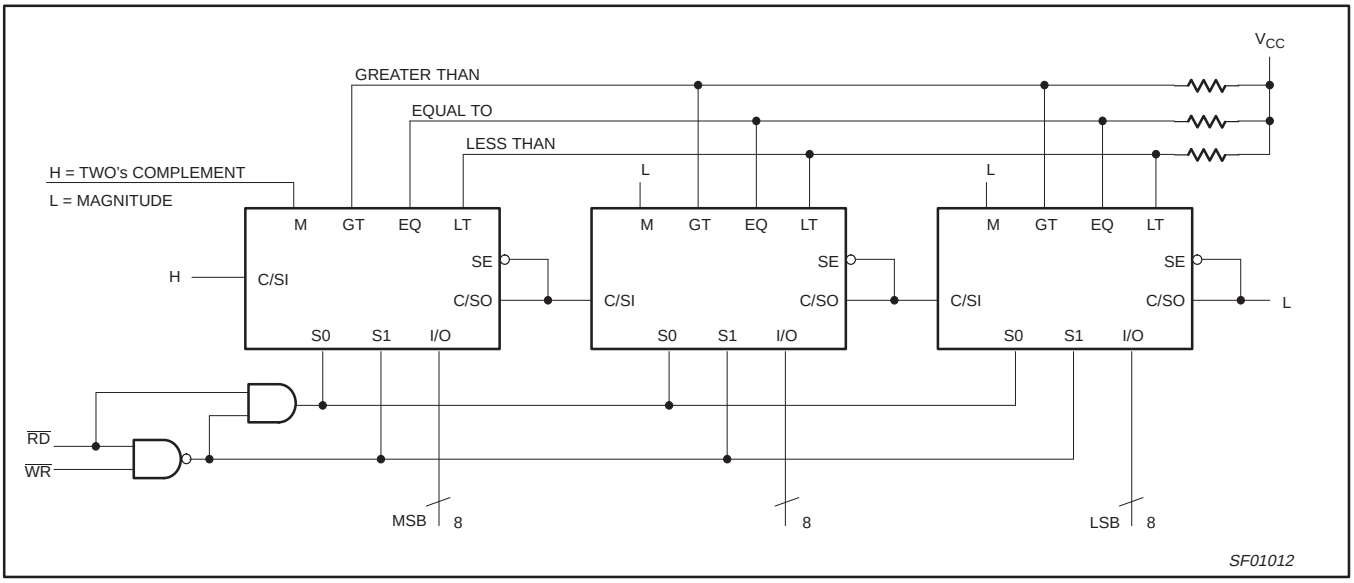


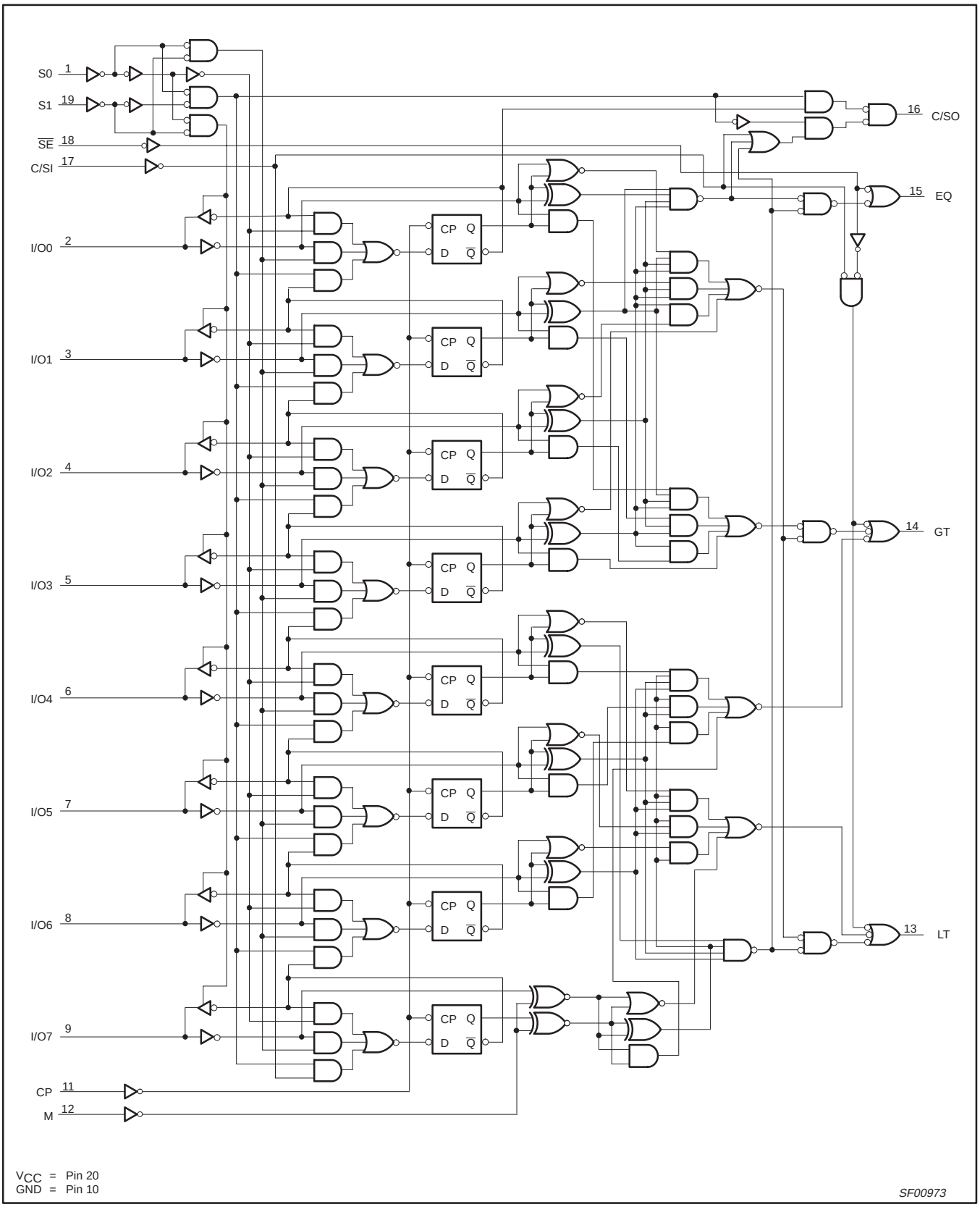
Figure 1. Cascading 74F524s for Comparing Longer Words

FUNCTION TABLE

INPUTS					OUTPUTS				OPERATING MODE
$\overline{SE}$	C/SI	S0	S1	Data comparison	EQ	GT	LT	C/SO	
H	H	L	L	X	H	H	H	(1)	Hold
H	L	L	L	X	H	H	H	L	
H	X	H	L	X	H	H	H	Q0	Shift
H	H	L	H	X	H	H	H	(1)	Read
H	L	L	H	X	H	H	H	L	
H	H	H	H	X	H	H	H	(1)	Load
H	L	H	H	X	H	H	H	L	
L	L	H or L[2]	H or L[2]	OA–OH > I/O0–I/O7	L	H	H	L	Compare (GT=CT=off)
L	L	H or L[2]	H or L[2]	OA–OH = I/O0–I/O7	H	H	H	L	
L	L	H or L[2]	H or L[2]	OA–OH < I/O0–I/O7	L	H	H	L	
L	H	H or L[2]	H or L[2]	OA–OH > I/O0–I/O7	L	H	L	L	Compare (GT=CT=on)
L	H	H or L[2]	H or L[2]	OA–OH = I/O0–I/O7	H	L	L	H	
L	H	H or L[2]	H or L[2]	OA–OH < I/O0–I/O7	L	L	H	L	

(1) = High if I/On=Dn, otherwise Low
2 = Must meet setup and hold time requirements
H = High voltage level
L = Low voltage level
X = Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All except I/O	40	mA
		I/O only	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
V_{OH}	High-level output voltage	LT, EQ, GT only			4.5	V
I_{OH}	High-level output current	Not LT, EQ, GT, C/SO			–3	mA
		C/SO only			–1	mA
I_{OL}	Low-level output current	All except I/O			20	mA
		I/O only			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[NO TAG]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
I_{OH}	High-level output current	LT, EQ, GT only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OH}	High-level output voltage	C/SO only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.5			V
		I/On only			±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	I/On	V_{CC} = MAX, V_I = 5.5V					1	mA
		Except I/On	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	Except I/On	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_{OZH}	Off-state output current High-level voltage applied	I/On only	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–0.6	mA
I_{OS}	Short-circuit output current[3]	Except LT, EQ, GT	V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				110	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

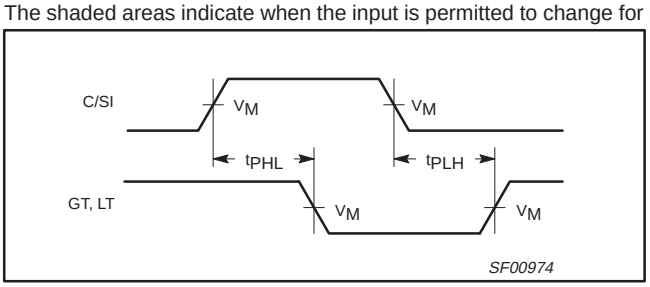
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 4	50	65		45		MHz
t_{PLH} t_{PHL}	Propagation delay I/On to EQ	Waveform 2	9.0 4.5	11.5 7.5	17.0 11.0	9.0 4.5	18.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay I/On to GT	Waveform 2	8.5 6.5	11.0 9.5	17.0 15.5	8.5 6.5	18.0 16.5	ns
t_{PLH} t_{PHL}	Propagation delay I/On to LT	Waveform 2	8.0 6.0	11.0 10.5	17.0 14.0	8.0 6.0	18.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay I/On to C/SO	Waveform 2	7.0 6.5	13.0 9.0	16.0 14.0	7.0 5.5	17.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to EQ	Waveform 4	11.0 4.0	17.0 8.0	22.0 14.0	10.0 4.0	23.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to GT	Waveform 4	11.0 10.0	16.0 16.5	20.0 21.0	10.0 10.0	21.0 22.0	ns
t_{PHL} t_{PLH}	Propagation delay CP to LT	Waveform 4	11.0 8.0	16.0 14.0	23.0 18.0	10.0 8.0	24.0 19.0	ns
t_{PLH}	Propagation delay CP to C/SO (Load)	Waveform 4	10.0	16.0	20.0	10.0	21.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to C/SO (Serial shift)	Waveform 4	5.0 4.5	10.0 9.0	13.0 11.5	5.0 4.5	14.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to GT	Waveform 1	8.0 3.0	10.5 4.5	16.0 8.5	9.0 2.5	17.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to LT	Waveform 1	8.0 3.0	10.5 6.0	17.0 8.5	8.0 2.5	18.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay Sn to C/SO	Waveform 2	6.5 5.5	8.0 10.0	14.5 17.0	6.5 5.5	15.5 18.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to EQ	Waveform 2	3.5 2.5	7.0 4.5	10.5 8.0	3.5 2.5	11.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to GT	Waveform 2	6.0 3.5	8.0 5.0	13.0 8.0	6.0 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to LT	Waveform 2	5.0 3.5	8.0 5.5	12.0 8.0	5.0 3.0	13.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to C/SO	Waveform 2	4.0 4.0	7.0 7.0	11.0 11.0	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay M to GT	Waveform 2	8.0 8.0	13.0 10.0	18.0 15.5	8.0 8.0	19.0 16.5	ns
t_{PLH} t_{PHL}	Propagation delay M to LT	Waveform 2	10.0 6.0	15.0 8.0	20.0 12.0	10.0 5.0	21.0 13.0	ns
t_{PZH} t_{PZL}	Output Enable time Sn to I/On	Waveform NO TAG Waveform NO TAG	4.5 5.5	7.0 9.0	13.0 15.0	4.5 5.5	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output Disable time Sn to I/On	Waveform NO TAG Waveform NO TAG	3.0 4.5	5.0 8.0	12.0 12.5	2.0 4.5	13.0 13.5	ns

AC SETUP REQUIREMENTS

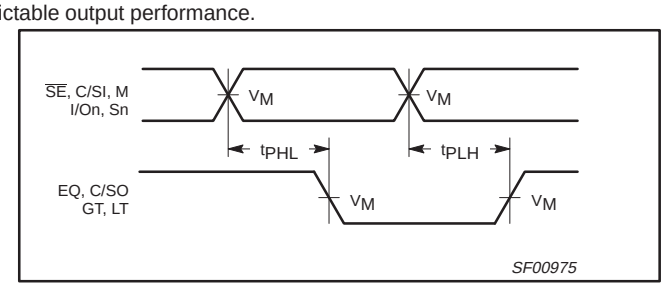
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/On to CP	Waveform 3	6.0 6.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/On to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S0, S1 to CP	Waveform 3	13.5 10.0			15.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S0, S1 to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low C/SI to CP	Waveform 3	7.0 7.0			7.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low C/SI to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 4	5.0 10.0			5.0 10.0		ns

AC WAVEFORMS

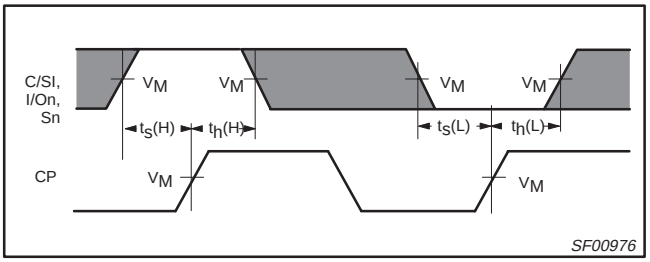
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



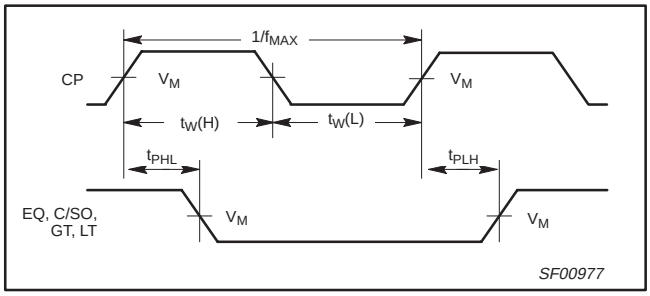
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting Outputs



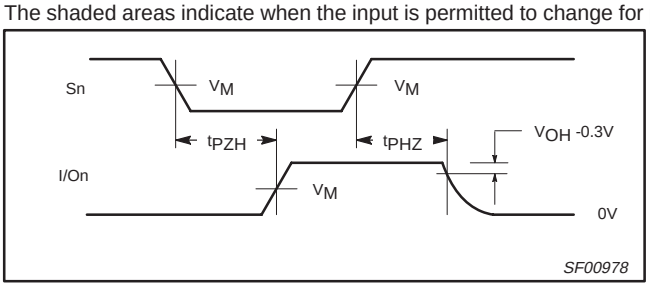
Waveform 3. Setup and Hold Times



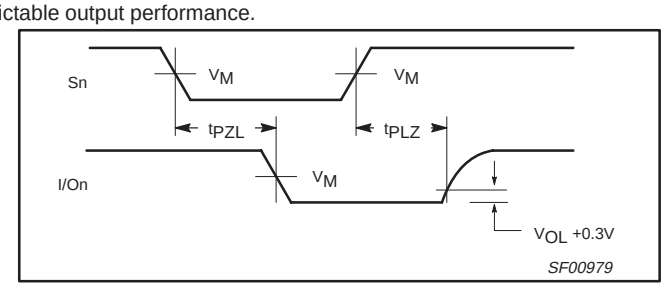
Waveform 4. Propagation Delay, Clock to Output, Clock Pulse Width, and Maximum Clock Frequency

AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

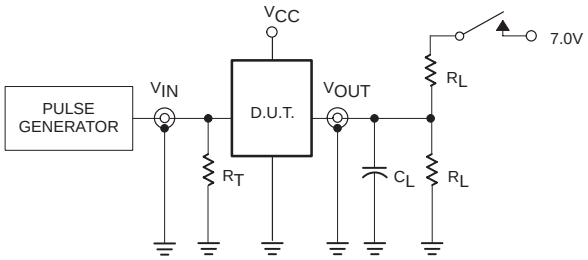


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

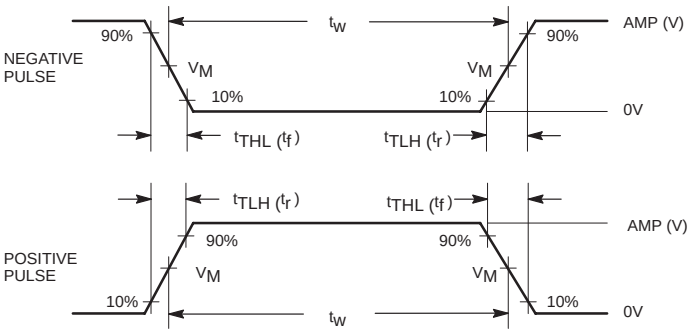


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
Open Collector	closed
All other	open

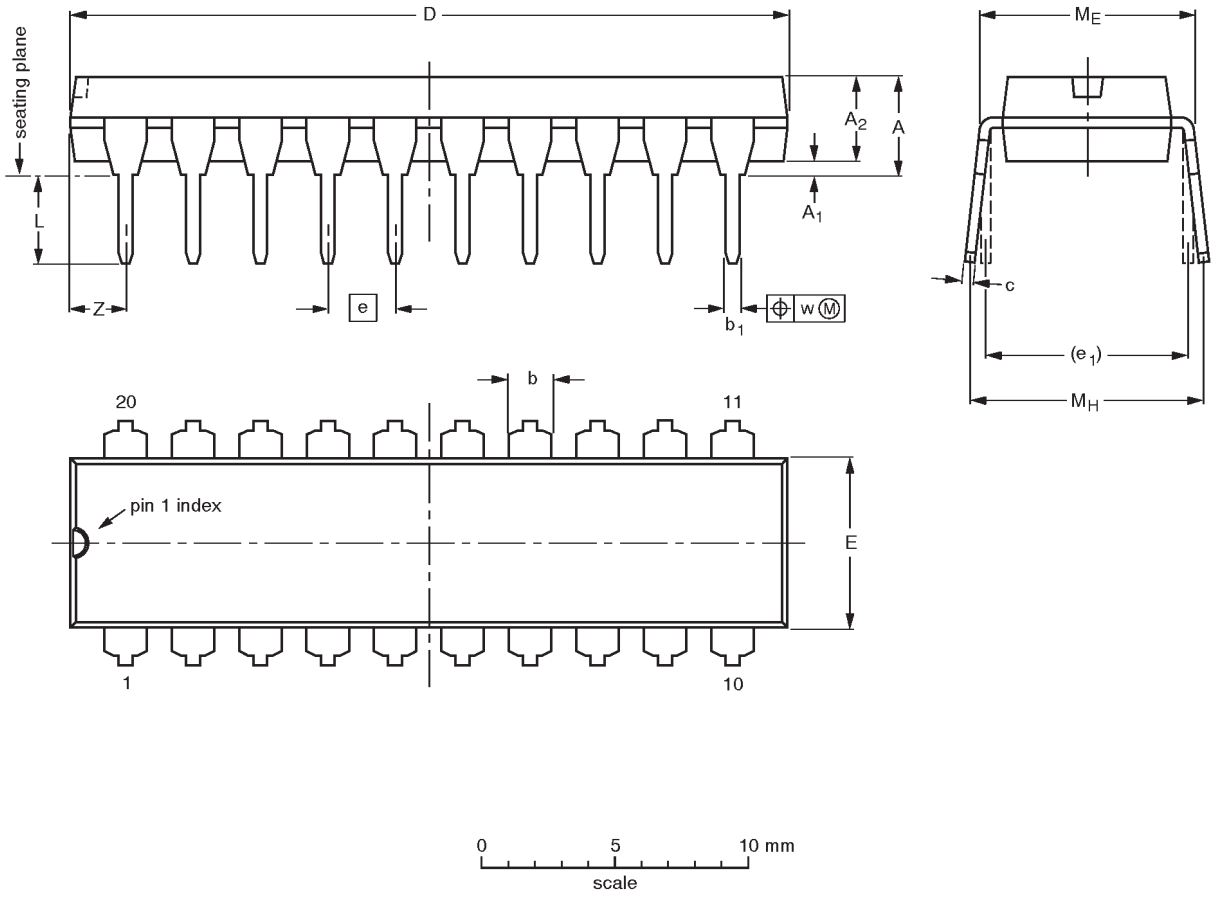
DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00980

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

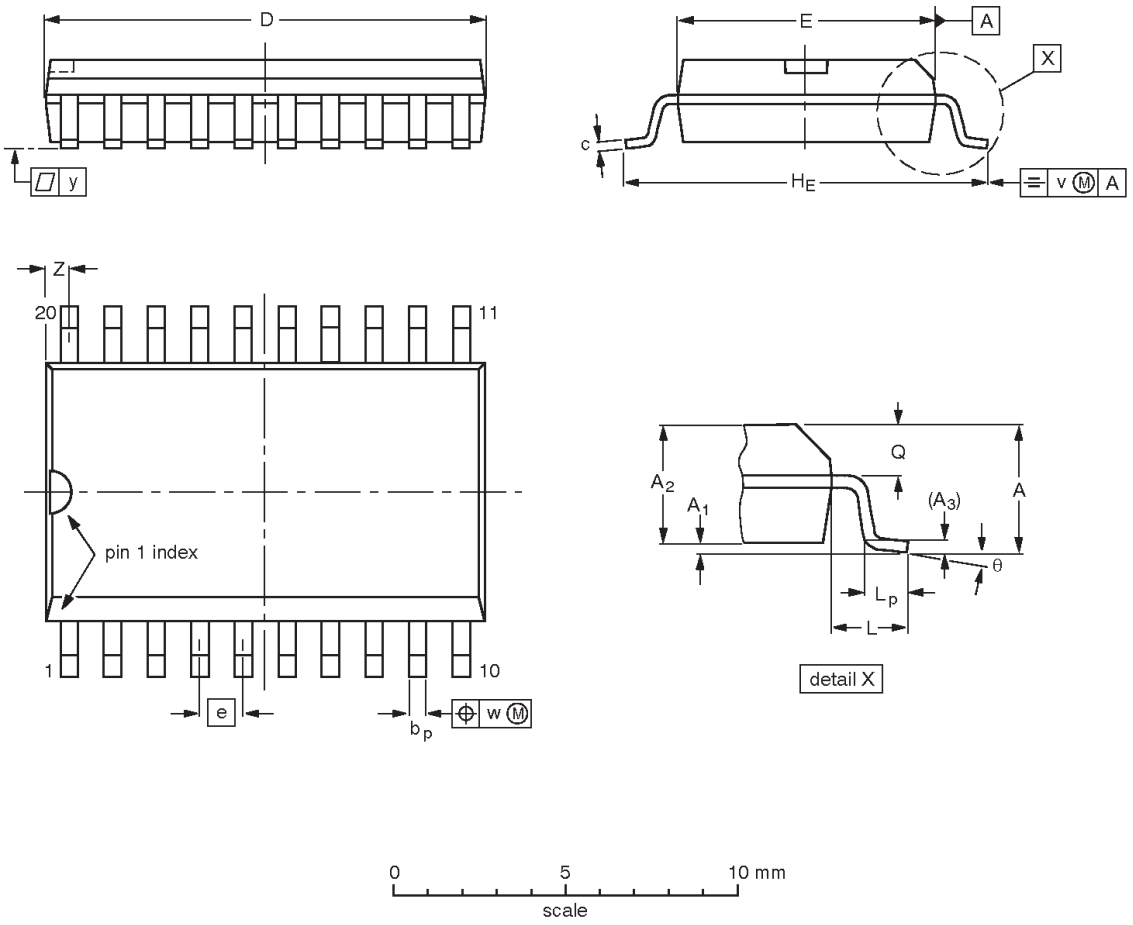
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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