

# 74HC02; 74HCT02

## Quad 2-input NOR gate

Rev. 03 — 18 September 2008

Product data sheet

### 1. General description

The 74HC02; 74HCT02 are high-speed Si-gate CMOS devices that comply with JEDEC standard no. 7A. They are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC02; 74HCT02 provides a quad 2-input NOR function.

### 2. Features

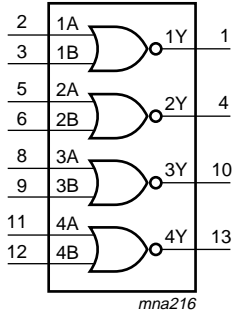
- Input levels:
  - ◆ For 74HC02: CMOS level
  - ◆ For 74HCT02: TTL level
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

### 3. Ordering information

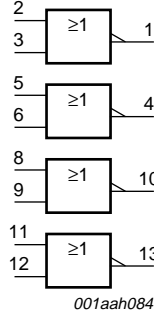
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC02N	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT02N				
74HC02D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT02D				
74HC02DB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT02DB				
74HC02PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT02PW				
74HC02BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1
74HCT02BQ				

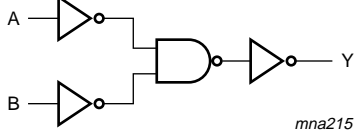
4. Functional diagram



*mna216*



*001aah084*



*mna215*

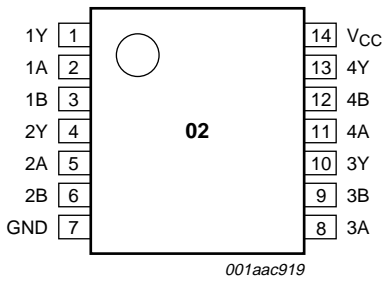
**Fig 1. Logic symbol**

**Fig 2. IEC logic symbol**

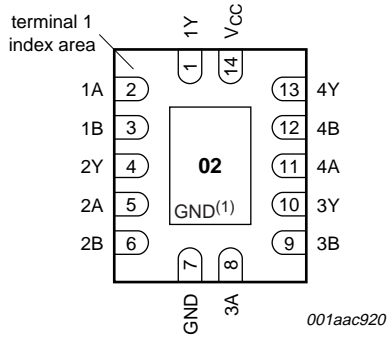
**Fig 3. Logic diagram (one gate)**

5. Pinning information

5.1 Pinning



*001aac919*



*001aac920*

Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

**Fig 4. Pin configuration DIP14, SO14 and (T)SSOP14**

**Fig 5. Pin configuration DHVQFN14**

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y to 4Y	1, 4, 10, 13	data output
1A to 4A	2, 5, 8, 11	data input
1B to 4B	3, 6, 9, 12	data input
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3.** Function table<sup>[1]</sup>

Input		Output
nA	nB	nY
L	L	H
X	H	L
H	X	L

- [1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

## 7. Limiting values

**Table 4.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	±20	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	±20	mA
$I_O$	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	±25	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation		[2]		
	DIP14 package		-	750	mW
	SO14, (T)SSOP14 and DHVQFN14 packages		-	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- [2] For DIP14 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.  
For SO14 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
For (T)SSOP14 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.  
For DHVQFN14 packages:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5.** Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC02			74HCT02			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	-40	-	+125	°C

**Table 5. Recommended operating conditions ...continued**  
*Voltages are referenced to GND (ground = 0 V) ...continued*

Symbol	Parameter	Conditions	74HC02			74HCT02			Unit
			Min	Typ	Max	Min	Typ	Max	
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC02</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -20\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\ \mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 20\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu\text{A}; V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A};$ $V_{CC} = 6.0\text{ V}$	-	-	2.0	-	20	-	40	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT02</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	2.0	-	20	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0 A; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V	-	150	540	-	675	-	735	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND = 0 V; C<sub>L</sub> = 50 pF; for load circuit see [Figure 7](#).

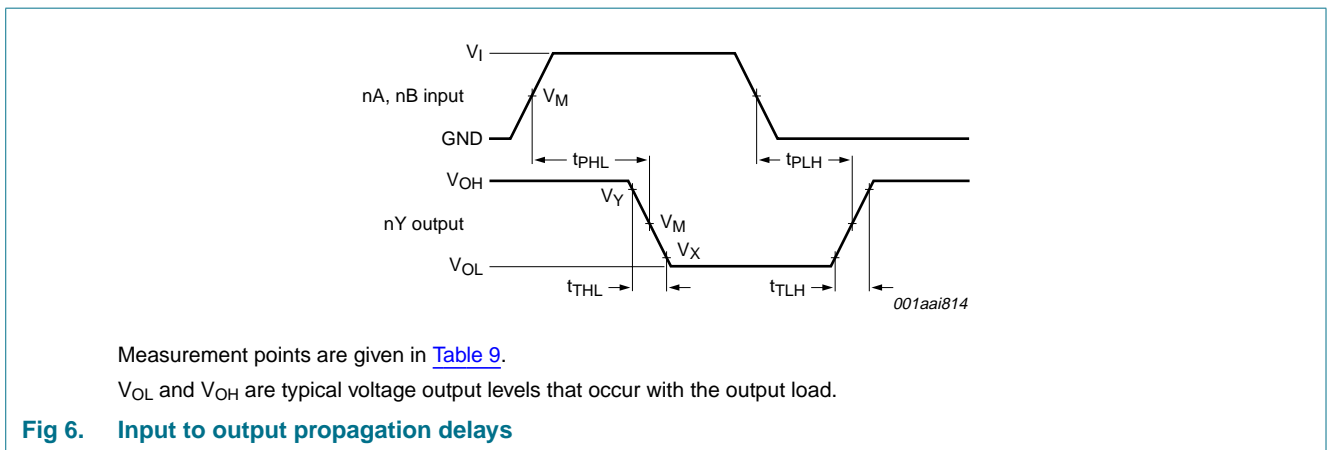
Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit	
			Min	Typ	Max	Max (85 °C)	Max (125 °C)		
<b>74HC02</b>									
t <sub>pd</sub>	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a>		<a href="#">[1]</a>					
		V <sub>CC</sub> = 2.0 V	-	25	90	115	135	ns	
		V <sub>CC</sub> = 4.5 V	-	9	18	23	27	ns	
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	7	-	-	-	ns	
		V <sub>CC</sub> = 6.0 V	-	7	15	20	23	ns	
t <sub>t</sub>	transition time	see <a href="#">Figure 6</a>		<a href="#">[2]</a>					
		V <sub>CC</sub> = 2.0 V	-	19	75	95	110	ns	
		V <sub>CC</sub> = 4.5 V	-	7	15	19	22	ns	
		V <sub>CC</sub> = 6.0 V	-	6	13	16	19	ns	
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub>		<a href="#">[3]</a>	-	22	-	-	pF

**Table 7. Dynamic characteristics**  
 GND = 0 V; C<sub>L</sub> = 50 pF; for load circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit	
			Min	Typ	Max	Max (85 °C)	Max (125 °C)		
<b>74HCT02</b>									
t <sub>pd</sub>	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a>	[1]						
		V <sub>CC</sub> = 4.5 V	-	11	19	24	29	ns	
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	9	-	-	-	ns	
t <sub>t</sub>	transition time	V <sub>CC</sub> = 4.5 V; see <a href="#">Figure 6</a>	[2]	-	7	15	19	22	ns
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V	[3]	-	24	-	-	-	pF

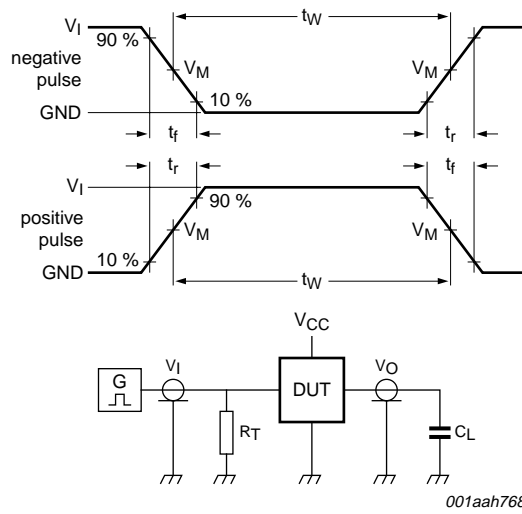
- [1] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.
- [2] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 11. Waveforms



**Table 8. Measurement points**

Type	Input	Output		
	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
74HC02	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	0.1V <sub>CC</sub>	0.9V <sub>CC</sub>
74HCT02	1.3 V	1.3 V	0.1V <sub>CC</sub>	0.9V <sub>CC</sub>



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

**Fig 7. Load circuitry for measuring switching times**

**Table 9. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74HC02	$V_{CC}$	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74HCT02	3.0 V	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

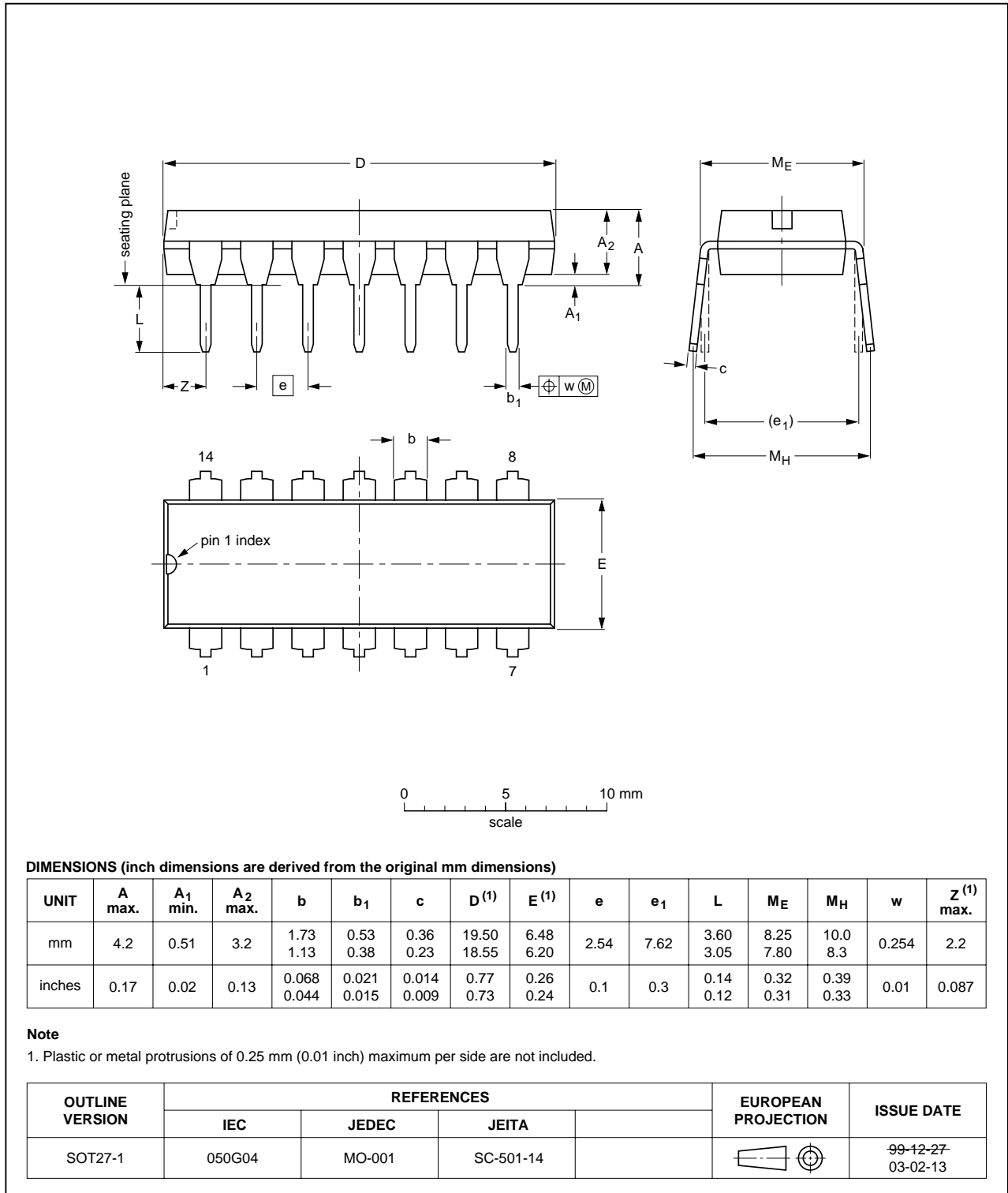


Fig 8. Package outline SOT27-1 (DIP14)



SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

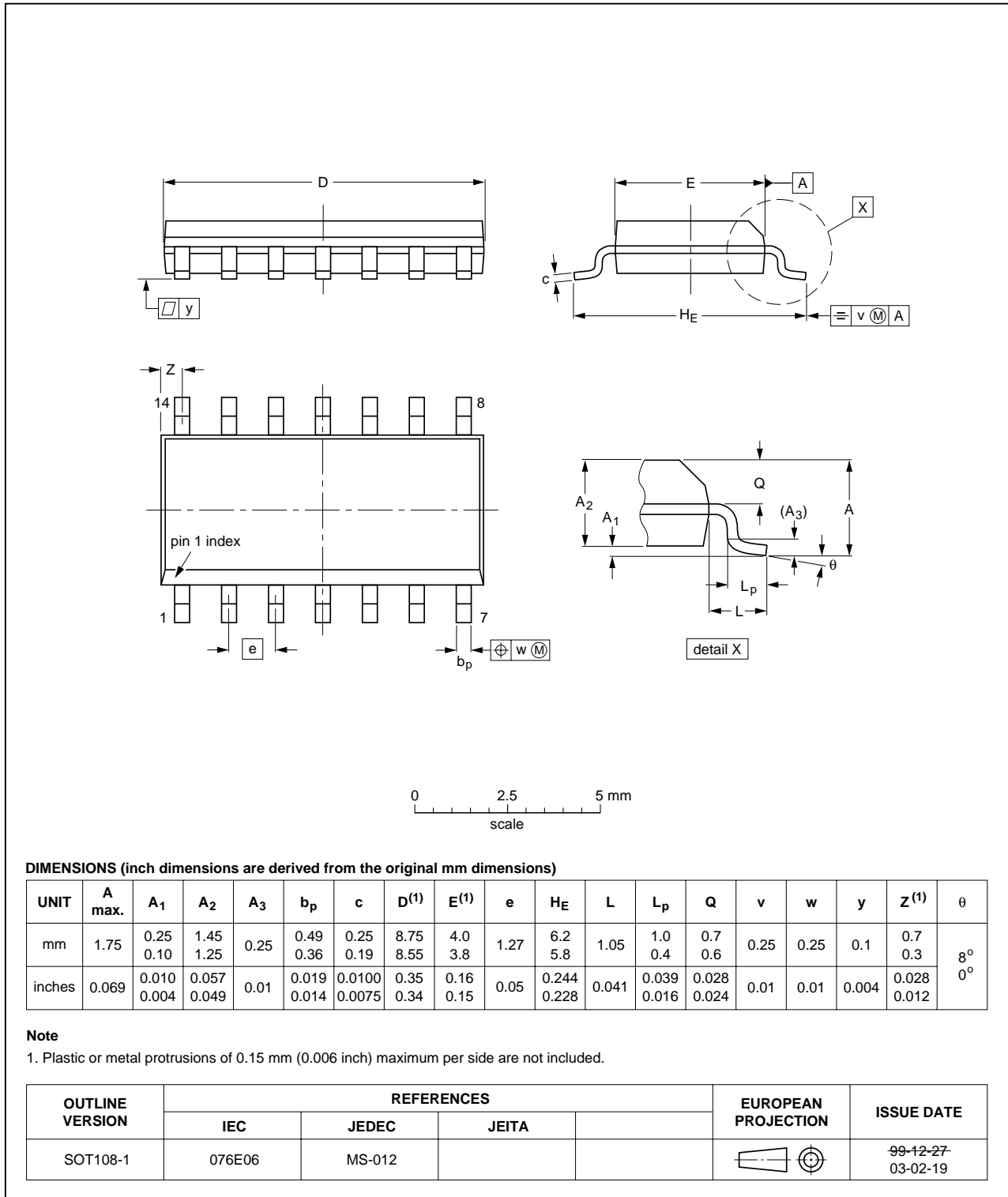


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

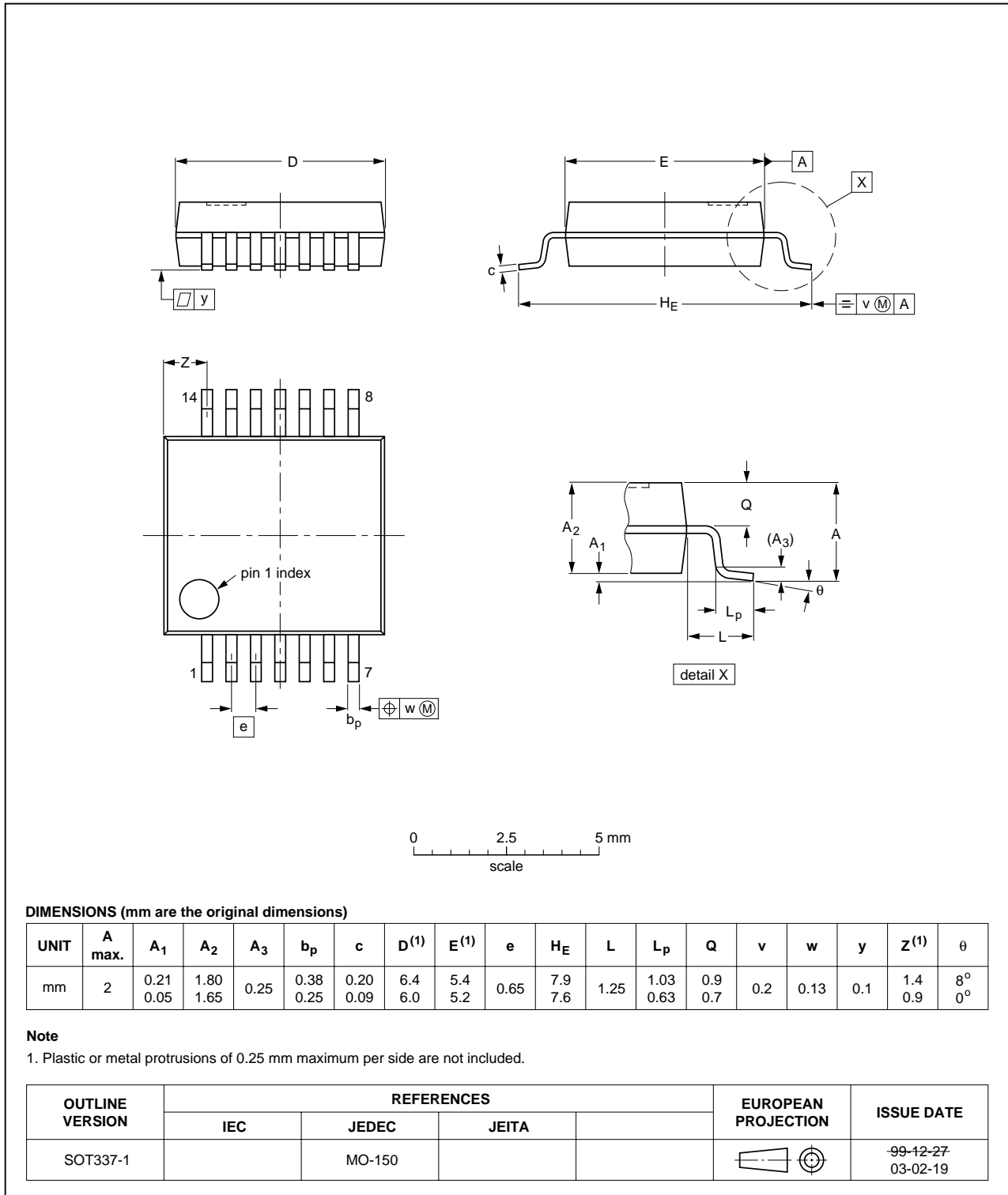


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

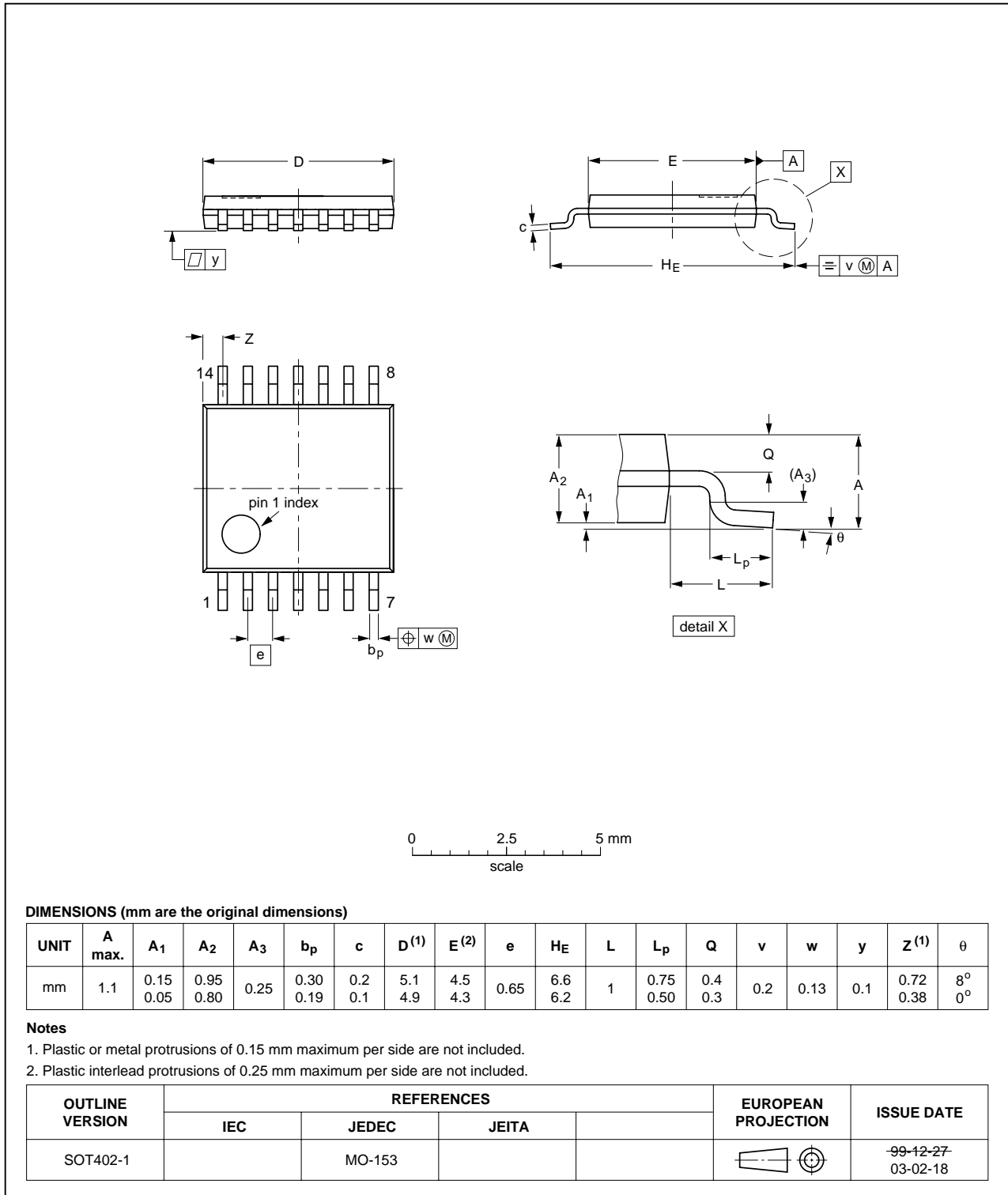


Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

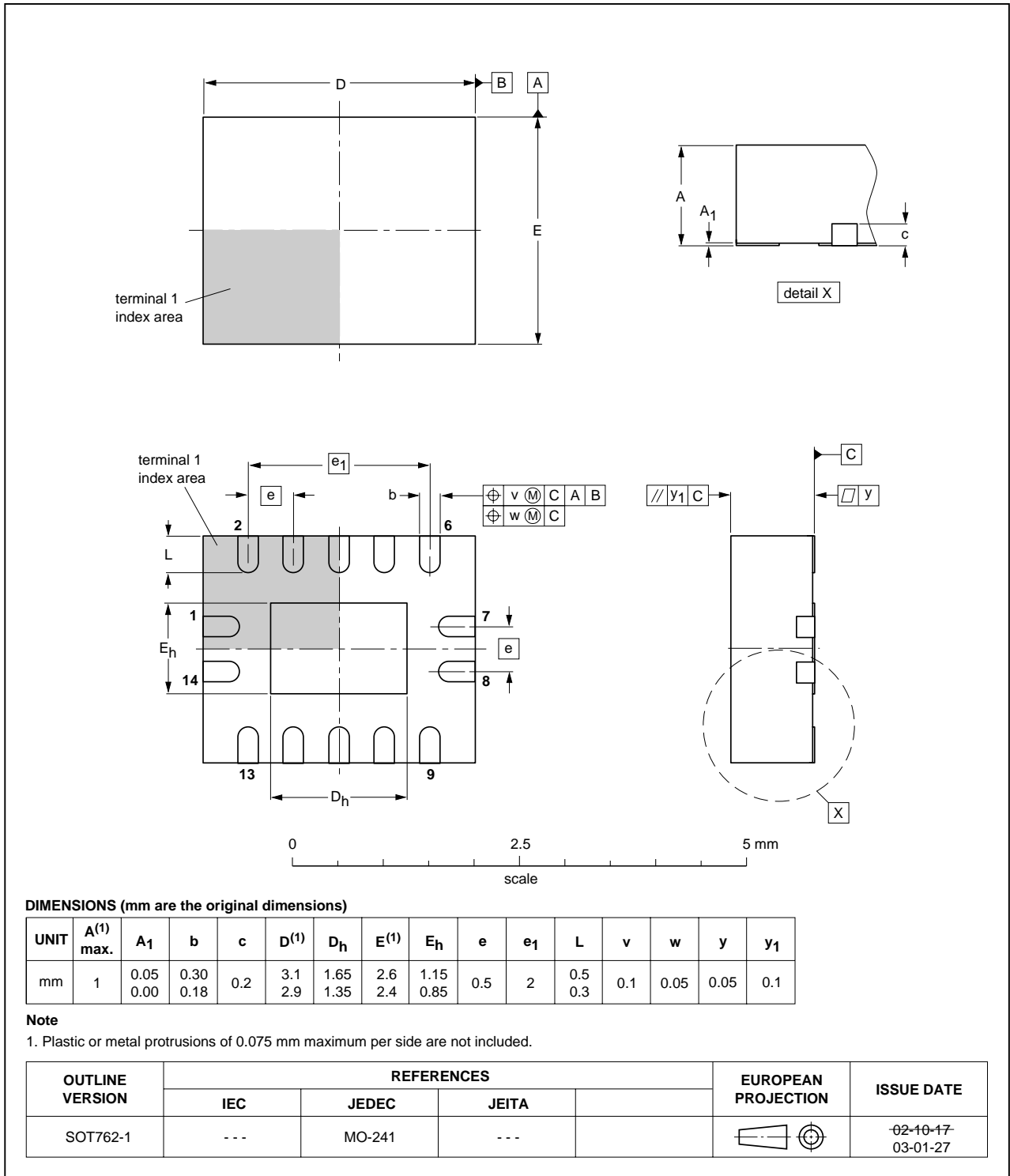


Fig 12. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT02_3	20080918	Product data sheet	-	74HC_HCT02_CNV_2
Modifications:				
				<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Added type numbers 74HC02BQ and 74HCT02BQ (DHVQFN14 package)</li></ul>
74HC_HCT02_CNV_2	19970827	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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