

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT7404**

**5-Bit x 64-word FIFO register;  
3-state**

Product specification  
Supersedes data of October 1990  
File under Integrated Circuits, IC06

September 1993

## 5-Bit x 64-word FIFO register; 3-state

## 74HC/HCT7404

## FEATURES

- Synchronous or asynchronous operation
- 3-state outputs
- 30 MHz (typical) shift-in and shift-out rates
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: driver (8 mA)
- $I_{CC}$  category: LSI.

## APPLICATIONS

- High-speed disc or tape controller
- Communications buffer.

## GENERAL DESCRIPTION

The 74HC/HCT7404 are high-speed Si-gate CMOS devices specified in compliance with JEDEC standard no.7A.

The "7404" is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 5 bits. A guaranteed 15 MHz data-rate makes it ideal for high-speed applications. A higher data-rate can be obtained in applications where the status flags are not used (burst-mode).

With separate controls for shift-in (SI) and shift-out ( $\overline{SO}$ ), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input ( $\overline{MR}$ ), an output enable input ( $\overline{OE}$ ) and flags. The data-in-ready (DIR) and data-out-ready (DOR) flags indicate the status of the device.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $\overline{SO}$ , SI to DIR and DOR	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	15	17	ns
$f_{max}$	maximum clock frequency		30	30	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	note 1	475	490	pF

## Note

1. For HC the condition is  $V_I = \text{GND to } V_{CC}$ .  
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ .

## ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7404N	18	DIL	plastic	SOT102
74HC/HCT7404D	20	SO20	plastic	SOT163A

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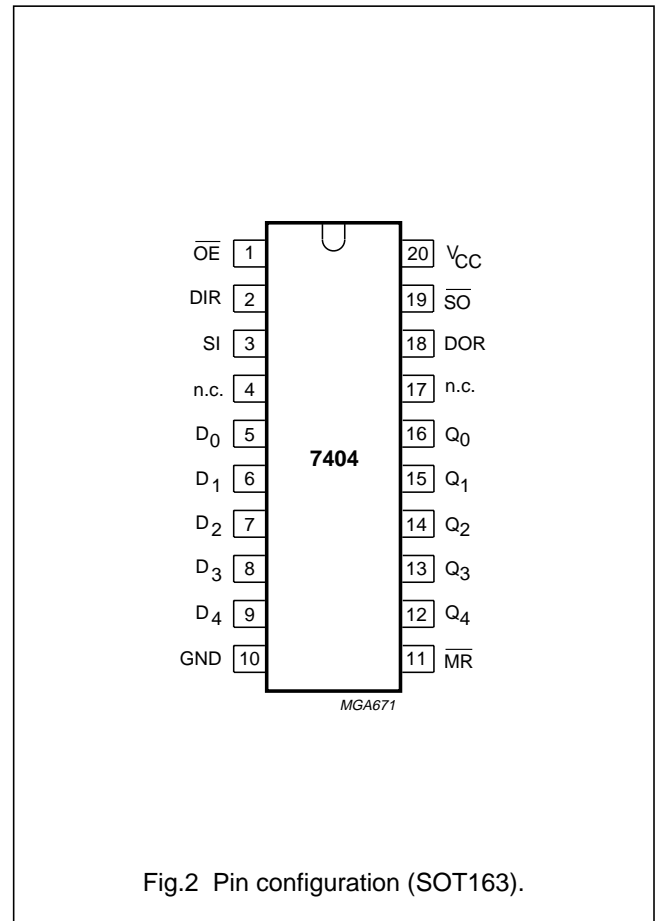
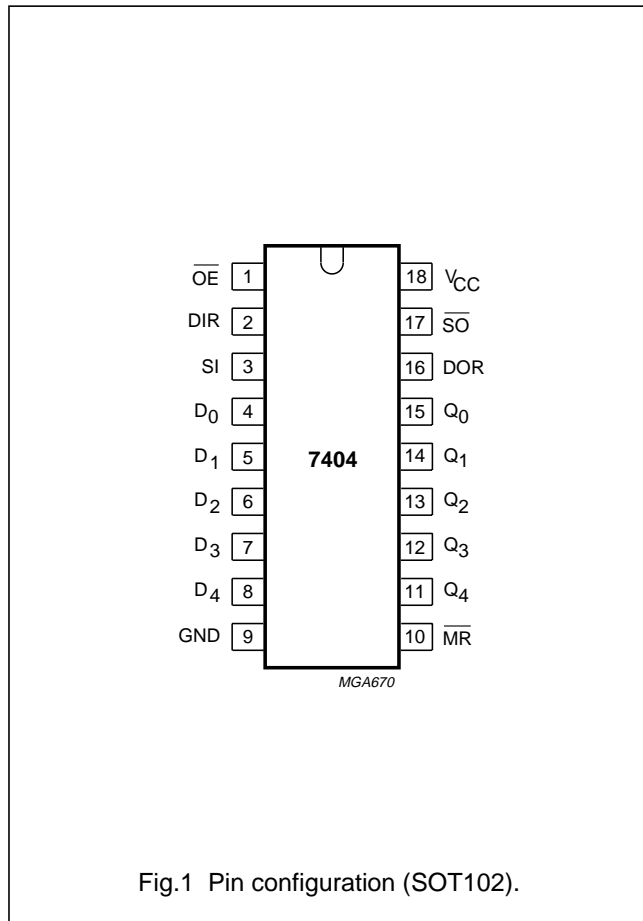
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PINNING (SOT102)

SYMBOL	PIN	DESCRIPTION
$\overline{OE}$	1	output enable input (active LOW)
DIR	2	data-in-ready output
SI	3	shift-in input (active HIGH)
D <sub>0</sub> to D <sub>4</sub>	4, 5, 6, 7, 8	parallel data inputs
GND	9	ground
$\overline{MR}$	10	asynchronous master-reset input (active LOW)
Q <sub>4</sub> to Q <sub>0</sub>	11, 12, 13, 14, 15	data outputs
DOR	16	data-out-ready output
$\overline{SO}$	17	shift-out input (active LOW)
V <sub>CC</sub>	18	positive supply voltage

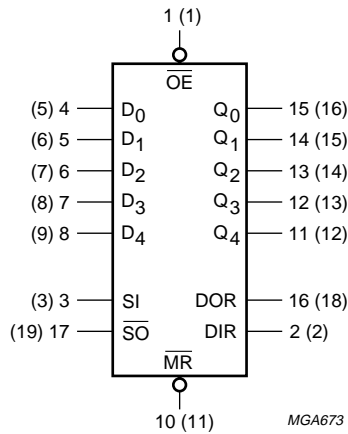
PINNING (SOT163A)

SYMBOL	PIN	DESCRIPTION
$\overline{OE}$	1	output enable input (active LOW)
DIR	2	data-in-ready output
SI	3	shift-in input (active HIGH)
n.c.	4	not connected
D <sub>0</sub> to D <sub>4</sub>	5, 6, 7, 8, 9	parallel data inputs
GND	10	ground
$\overline{MR}$	11	asynchronous master-reset input (active LOW)
Q <sub>4</sub> to Q <sub>0</sub>	12, 13, 14, 15, 16	data outputs
n.c.	17	not connected
DOR	18	data-out ready output
n.c.	19	not connected
V <sub>CC</sub>	20	positive supply voltage



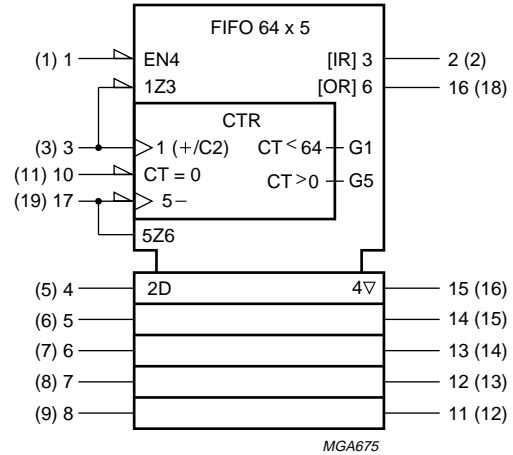
5-Bit x 64-word FIFO register; 3-state

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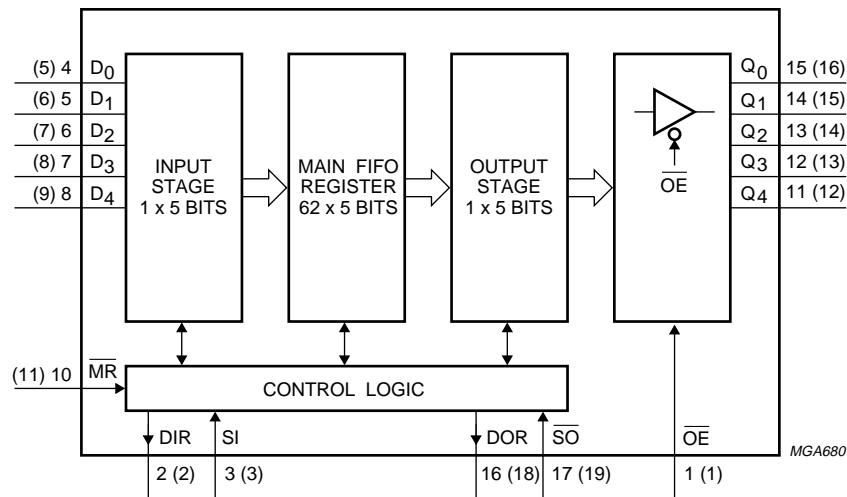
Pin numbers between parentheses refer to the SO package.

Fig.3 Logic symbol.



Pin numbers between parentheses refer to the SO package.

Fig.4 IEC logic symbol.



Pin numbers between parentheses refer to the SO package.

Fig.5 Functional diagram.

5-Bit x 64-word FIFO register; 3-state

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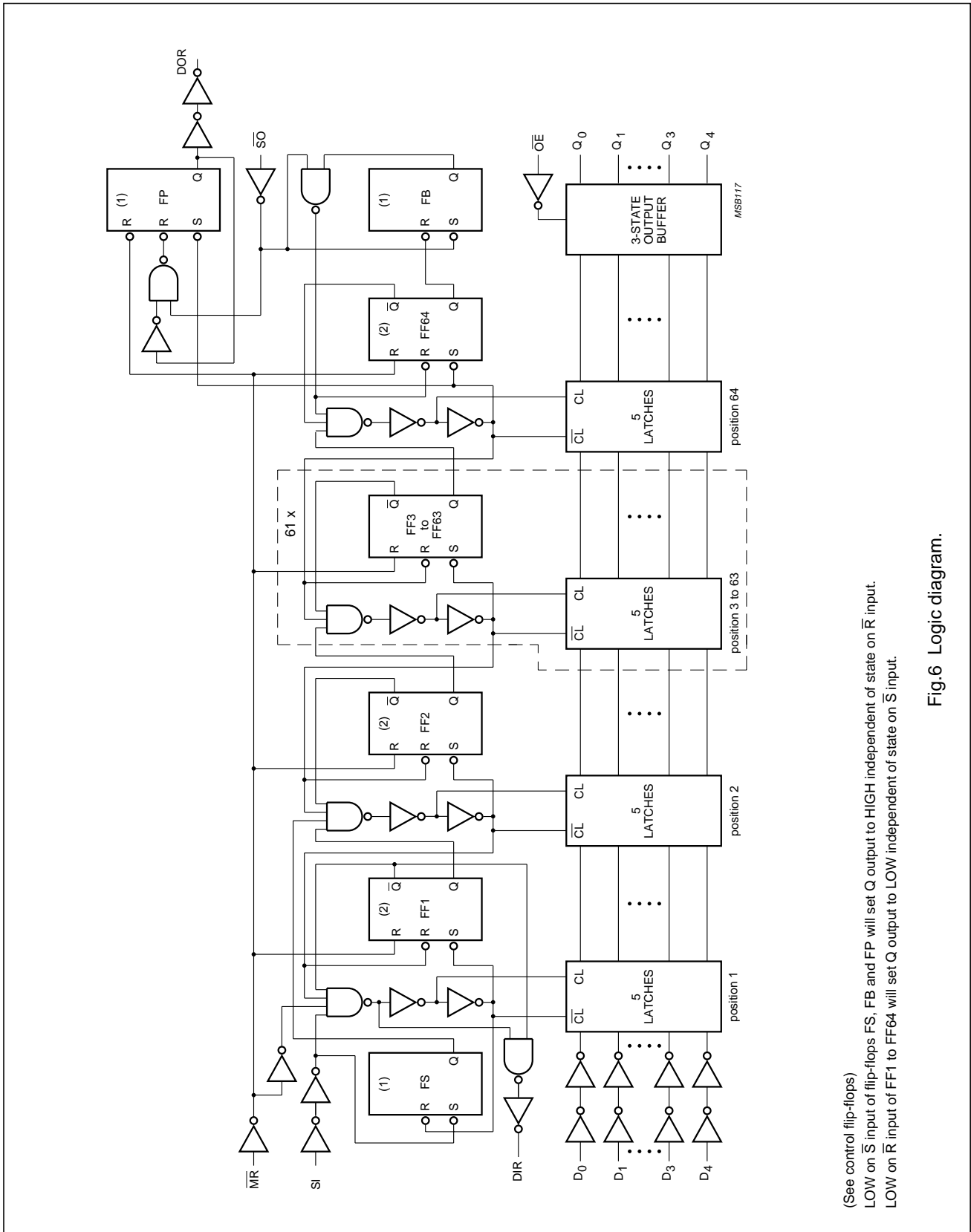


Fig.6 Logic diagram.

## 5-Bit x 64-word FIFO register; 3-state

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**FUNCTIONAL DESCRIPTION**

The DIR flag indicates the input stage status, either empty and ready to receive data (DIR = HIGH) or full and busy (DIR = LOW). When DIR and SI are HIGH, data present at D<sub>0</sub> to D<sub>4</sub> is shifted into the input stage; once complete DIR goes LOW. When SI is set LOW, data is automatically shifted to the output stage or to the last empty location. A FIFO which can receive data is indicated by DIR set HIGH.

A DOR flag indicates the output stage status, either data available (DOR = HIGH) or busy (DOR = LOW). When  $\overline{SO}$  and DOR are HIGH, data is available at the

outputs (Q<sub>0</sub> to Q<sub>4</sub>). When  $\overline{SO}$  is LOW new data may be shifted into the output stage, once complete DOR is set LOW.

**Expanded Format** (see Fig.18)

The DOR and DIR signals are used to allow the '7404' to be cascaded. Both parallel and serial expansion is possible. Serial expansion is only possible with typical devices.

**Parallel Expansion**

Parallel expansion is accomplished by logically ANDing the DOR and DIR signals to form a composite signal.

**Serial Expansion**

Serial expansion is accomplished by:

- tying the data outputs of the first device to the data inputs of the second device
- connecting the DOR pin of the first device to the SI pin of the second device
- connecting the  $\overline{SO}$  pin of the first device to the DIR pin of the second device.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: parallel outputs, bus driver; serial output, standard I<sub>CC</sub> category: MSI

Output capability: driver 8 mA

I<sub>CC</sub> category: LSI

Voltages are referenced to GND (ground = 0 V).

**DC CHARACTERISTICS FOR 74HC**

SYMBOL	PARAMETER	T <sub>amb</sub> °C							UNIT	TEST CONDITION		
		+25			-40 to +85		-40 to +125			V <sub>CC</sub> (V)	V <sub>I</sub>	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V <sub>OH</sub>	HIGH level output voltage	3.98	4.32	–	3.84	–	3.70	–	V	4.5 6	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = –8 mA I <sub>O</sub> = –10 mA
		5.48	5.81	–	5.34	–	5.20	–	V			
V <sub>OL</sub>	LOW level output voltage	–	0.15	0.26	–	0.33	–	0.4	V	4.5 6	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 8 mA I <sub>O</sub> = 10 mA
		–	0.15	0.26	–	0.33	–	0.4	V			

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## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	$T_{amb}$ °C							UNIT	TEST CONDITION	
		+25			-40 to +85		-40 to +125			$V_{CC}$ (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
$t_{PHL}/t_{PLH}$	propagation delay $\overline{MR}$ to DIR, DOR	–	69	210	–	265	–	315	ns	2.0	Fig.9
		–	25	42	–	53	–	63	ns	4.5	
		–	20	36	–	45	–	54	ns	6.0	
$t_{PHL}$	propagation delay MR to $Q_n$	–	52	160	–	200	–	240	ns	2.0	Fig.9
		–	19	32	–	40	–	48	ns	4.5	
		–	15	27	–	34	–	41	ns	6.0	
$t_{PHL}/t_{PLH}$	propagation delay SI to DIR	–	66	205	–	255	–	310	ns	2.0	Fig.7
		–	24	41	–	51	–	62	ns	4.5	
		–	19	35	–	43	–	53	ns	6.0	
$t_{PHL}/t_{PLH}$	propagation delay $\overline{SO}$ to DOR	–	94	290	–	365	–	435	ns	2.0	Fig.10
		–	34	58	–	73	–	87	ns	4.5	
		–	27	49	–	62	–	74	ns	6.0	
$t_{PHL}/t_{PLH}$	propagation delay DOR to $Q_n$	–	11	35	–	45	–	55	ns	2.0	Fig.11
		–	4	7	–	9	–	11	ns	4.5	
		–	3	6.0	–	8	–	9	ns	6.0	
$t_{PHL}/t_{PLH}$	propagation delay $\overline{SO}$ to $Q_n$	–	105	325	–	406	–	488	ns	2.0	Fig.15
		–	38	65	–	81	–	98	ns	4.5	
		–	30	55	–	69	–	83	ns	6.0	
$t_{PLH}$	propagation delay/ripple through delay SI to DOR	–	2.2	7.0	–	8.8	–	10.5	$\mu$ s	2.0	Fig.16
		–	0.8	1.4	–	1.8	–	2.1	$\mu$ s	4.5	
		–	0.6	1.2	–	1.5	–	1.8	$\mu$ s	6.0	
$t_{PLH}$	propagation delay/bubble-up delay $\overline{SO}$ to DIR	–	2.8	9.0	–	11.2	–	13.5	$\mu$ s	2.0	Fig.8
		–	1.0	1.8	–	2.2	–	2.7	$\mu$ s	4.5	
		–	0.8	1.5	–	1.9	–	2.3	$\mu$ s	6.0	
$t_{PZH}/t_{PZL}$	3-state output enable $\overline{OE}$ to $Q_n$	–	44	150	–	190	–	225	ns	2.0	Fig.17
		–	16	30	–	38	–	45	ns	4.5	
		–	13	26	–	32	–	38	ns	6.0	
$t_{PHZ}/t_{PLZ}$	3-state output disable $\overline{OE}$ to $Q_n$	–	50	150	–	190	–	225	ns	2.0	Fig.17
		–	18	30	–	38	–	45	ns	4.5	
		–	14	26	–	33	–	38	ns	6.0	
$t_{THL}/t_{TLH}$	output transition time	–	14	60	–	75	–	90	ns	2.0	Fig.17
		–	5	12	–	15	–	18	ns	4.5	
		–	4	10	–	13	–	15	ns	6.0	
$t_w$	SI pulse width HIGH or LOW	35	11	–	45	–	55	–	ns	2.0	Fig.7
		7	4	–	9	–	11	–	ns	4.5	
		6	3	–	8	–	9	–	ns	6.0	
$t_w$	$\overline{SO}$ pulse width HIGH or LOW	70	22	–	90	–	105	–	ns	2.0	Fig.10
		14	8	–	18	–	21	–	ns	4.5	
		12	6	–	15	–	18	–	ns	6.0	

## 5-Bit x 64-word FIFO register; 3-state

## 74HC/HCT7404

SYMBOL	PARAMETER	T <sub>amb</sub> °C							UNIT	TEST CONDITION	
		+25			-40 to +85		-40 to +125			V <sub>CC</sub> (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t <sub>w</sub>	DIR pulse width HIGH	10	41	130	8	165	8	195	ns	2.0	Fig.8
		5	15	26	4	33	4	39	ns	4.5	
		4	12	22	3	28	3	33	ns	6.0	
t <sub>w</sub>	DOR pulse width HIGH	14	52	160	12	200	12	240	ns	2.0	Fig.11
		7	19	32	6	40	6	48	ns	4.5	
		6	15	27	5	34	5	41	ns	6.0	
t <sub>w</sub>	$\overline{\text{MR}}$ pulse width LOW	120	39	–	150	–	180	–	ns	2.0	Fig.9
		24	14	–	30	–	36	–	ns	4.5	
		20	11	–	26	–	31	–	ns	6.0	
t <sub>rem</sub>	removal time MR to SI	80	24	–	100	–	120	–	ns	2.0	Fig.16
		16	8	–	20	–	24	–	ns	4.5	
		14	7	–	17	–	20	–	ns	6.0	
t <sub>su</sub>	set-up time D <sub>n</sub> to SI	–8	–36	–	–6	–	–6	–	ns	2.0	Fig.14
		–4	–13	–	–3	–	–3	–	ns	4.5	
		–3	–10	–	–3	–	–3	–	ns	6.0	
t <sub>h</sub>	hold time D <sub>n</sub> to SI	135	44	–	170	–	205	–	ns	2.0	Fig.14
		27	16	–	34	–	41	–	ns	4.5	
		23	13	–	29	–	35	–	ns	6.0	
f <sub>max</sub>	maximum clock pulse frequency SI, $\overline{\text{SO}}$ burst mode	3.6	9.9	–	2.8	–	2.4	–	MHz	2.0	Fig.12 and Fig.13
		18	30	–	14	–	12	–	MHz	4.5	
		21	36	–	16	–	14	–	MHz	6.0	
f <sub>max</sub>	maximum clock pulse frequency SI, $\overline{\text{SO}}$ using flags	3.6	9.9	–	2.8	–	2.4	–	MHz	2.0	Fig.7 and Fig.10
		18	30	–	14	–	12	–	MHz	4.5	
		21	36	–	16	–	14	–	MHz	6.0	
f <sub>max</sub>	maximum clock pulse frequency SI, $\overline{\text{SO}}$ cascaded	–	7.6	–	–	–	–	–	MHz	2.0	Fig.7 and Fig.10
		–	23	–	–	–	–	–	MHz	4.5	
		–	27	–	–	–	–	–	MHz	6.0	



## 5-Bit x 64-word FIFO register; 3-state

## 74HC/HCT7404

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*", except that  $V_{OH}$  and  $V_{OL}$  are not valid for driver output. They are replaced by the values given below.

Output capability: driver 8 mA

$I_{CC}$  category: LSI.

Voltages are referenced to GND (ground = 0 V).

**DC CHARACTERISTICS FOR 74HCT**

SYMBOL	PARAMETER	$T_{amb} \text{ } ^\circ\text{C}$							UNIT	TEST CONDITION		
		+25			-40 to +85		-40 to +125			$V_{CC}$ (V)	$V_I$	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
$V_{OH}$	HIGH level output voltage	3.98	4.32	–	3.84	–	3.7	–	V	4.5	$V_{IH}$ or $V_{IL}$	$I_O = -8 \text{ mA}$
$V_{OL}$	LOW level output voltage	–	0.15	0.26	–	0.33	–	0.40	V	4.5	$V_{IH}$ or $V_{IL}$	$I_O = 8 \text{ mA}$

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

**UNIT LOAD COEFFICIENT**

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	1
SI	1.5
$D_n$	0.75
$\overline{MR}$	1.5
$\overline{SO}$	1.5

## 5-Bit x 64-word FIFO register; 3-state

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## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	$T_{amb}$ °C							UNIT	TEST CONDITION	
		+25			-40 to +85		-40 to +125			$V_{CC}$ (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
$t_{PHL}/t_{PLH}$	propagation delay $\overline{MR}$ to DIR, DOR	–	30	51	–	53	–	63	ns	4.5	Fig.9
$t_{PHL}$	propagation delay $\overline{MR}$ to $Q_n$	–	22	38	–	48	–	57	ns	4.5	Fig.9
$t_{PHL}/t_{PLH}$	propagation delay SI to DIR	–	25	43	–	54	–	65	ns	4.5	Fig.7
$t_{PHL}/t_{PLH}$	propagation delay $\overline{SO}$ to DOR	–	36	61	–	76	–	92	ns	4.5	Fig.10
$t_{PHL}/t_{PLH}$	propagation delay $\overline{SO}$ to $Q_n$	–	42	72	–	90	–	108	ns	4.5	Fig.15
$t_{PHL}/t_{PLH}$	propagation delay DOR to $Q_n$	–	7	12	–	15	–	18	ns	4.5	Fig.11
$t_{PLH}$	propagation delay/ripple through delay SI to DOR	–	0.8	1.4	–	1.75	–	2.1	$\mu$ s	4.5	Fig.11
$t_{PLH}$	propagation delay/bubble- up delay $\overline{SO}$ to DIR	–	1	1.8	–	2.25	–	2.7	$\mu$ s	4.5	Fig.8
$t_{PZH}/t_{PZL}$	3-state output enable $\overline{OE}$ to $Q_n$	–	16	30	–	38	–	45	ns	4.5	Fig.17
$t_{PHZ}/t_{PLZ}$	3-state output disable $\overline{OE}$ to $Q_n$	–	19	30	–	38	–	45	ns	4.5	Fig.17
$t_{THL}/t_{TLH}$	output transition time	–	5	12	–	15	–	18	ns	4.5	Fig.17
$t_w$	SI pulse width HIGH or LOW	9	5	–	6	–	8	–	ns	4.5	Fig.7
$t_w$	$\overline{SO}$ pulse width HIGH or LOW	14	8	–	18	–	21	–	ns	4.5	Fig.10
$t_w$	DIR pulse width HIGH	5	17	29	4	36	4	44	ns	4.5	Fig.8

## 5-Bit x 64-word FIFO register; 3-state

## 74HC/HCT7404

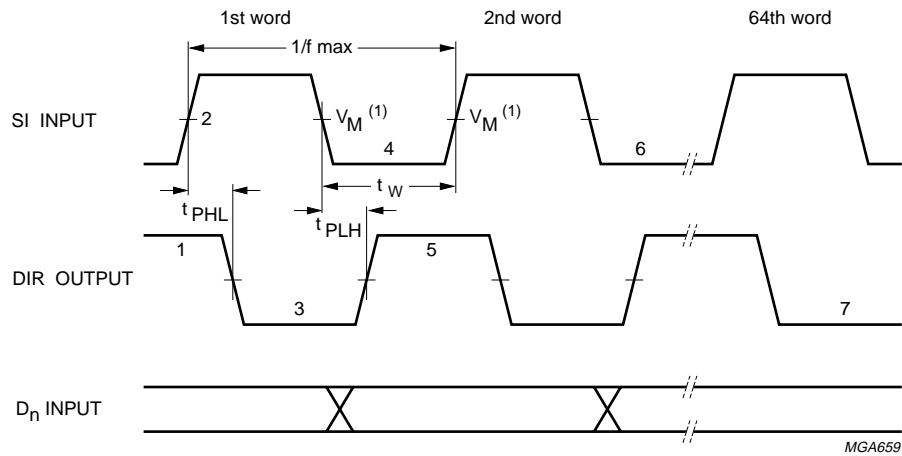
SYMBOL	PARAMETER	T <sub>amb</sub> °C							UNIT	TEST CONDITION	
		+25			-40 to +85		-40 to +125			V <sub>CC</sub> (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t <sub>w</sub>	DOR pulse width HIGH	7	21	36	6	45	6	54	ns	4.5	Fig.11
t <sub>w</sub>	$\overline{\text{MR}}$ pulse width LOW	26	15	–	33	–	39	–	ns	4.5	Fig.9
t <sub>rem</sub>	removal time MR to SI	18	10	–	23	–	27	–	ns	4.5	Fig.16
t <sub>su</sub>	set-up time D <sub>n</sub> to SI	–5	–16	–	–4	–	–4	–	ns	4.5	Fig.14
t <sub>h</sub>	hold time D <sub>n</sub> to SI	30	18	–	38	–	45	–	ns	4.5	Fig.14
f <sub>max</sub>	maximum clock pulse frequency SI, $\overline{\text{SO}}$ burst mode	18	30	–	14	–	12	–	MHz	4.5	Fig.12 and Fig.13
f <sub>max</sub>	maximum clock pulse frequency SI, $\overline{\text{SO}}$ using flags	18	30	–	14	–	12	–	MHz	4.5	Fig.7 and Fig.10
f <sub>max</sub>	maximum clock pulse frequency SI, $\overline{\text{SO}}$ cascaded	–	23	–	–	–	–	–	MHz	4.5	Fig.7 and Fig.10

## 5-Bit x 64-word FIFO register; 3-state

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## AC WAVEFORMS

## Shifting in sequence FIFO empty to FIFO full



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT :  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the SI input to DIR output propagation delay, the SI pulse width and SI maximum pulse frequency.

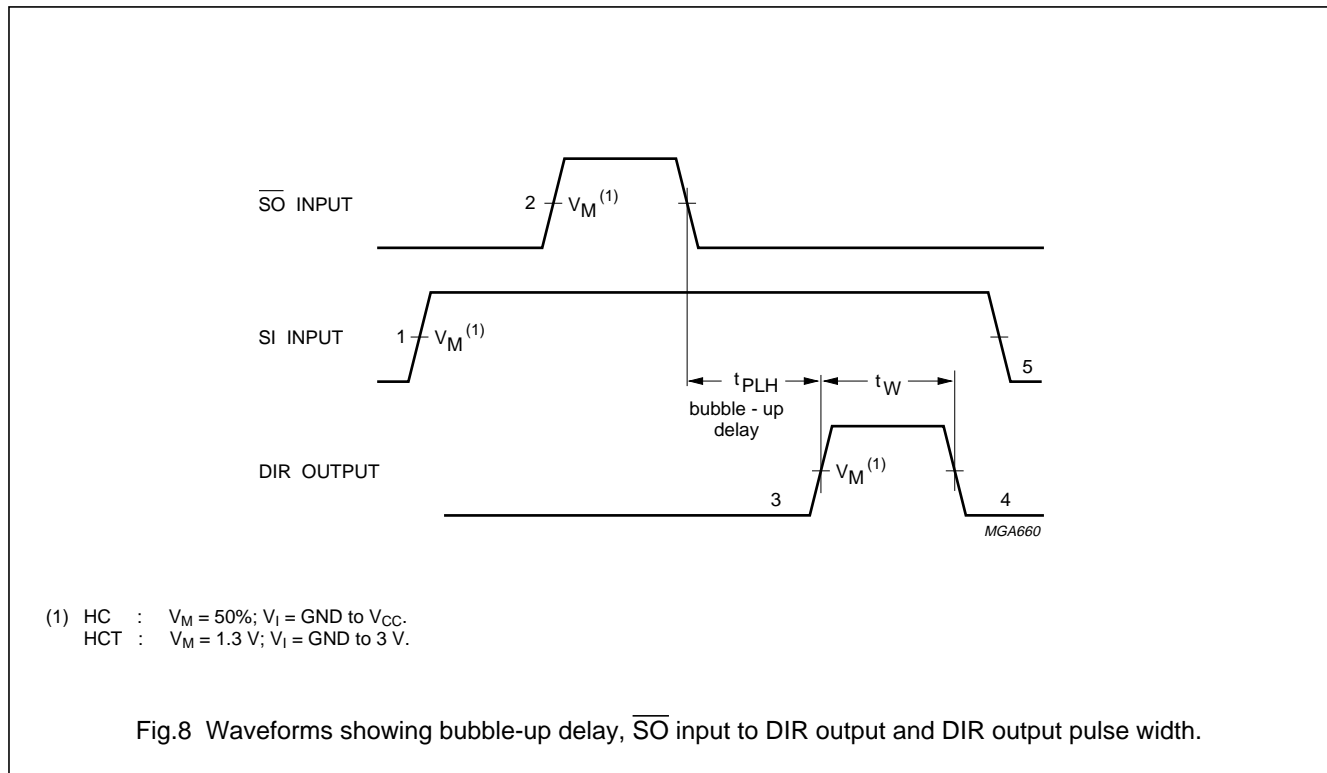
## Notes to Fig.7

1. DIR initially HIGH; FIFO is prepared for valid data
2. SI set HIGH; data loaded into input stage
3. DIR goes LOW, input stage "busy"
4. SI set LOW; data from first location "ripple through"
5. DIR goes HIGH, status flag indicates FIFO prepared for additional data
6. Repeat process to load 2nd word through to 64th word into FIFO  
 DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

## 5-Bit x 64-word FIFO register; 3-state

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With FIFO full; SI held HIGH in anticipation of empty location

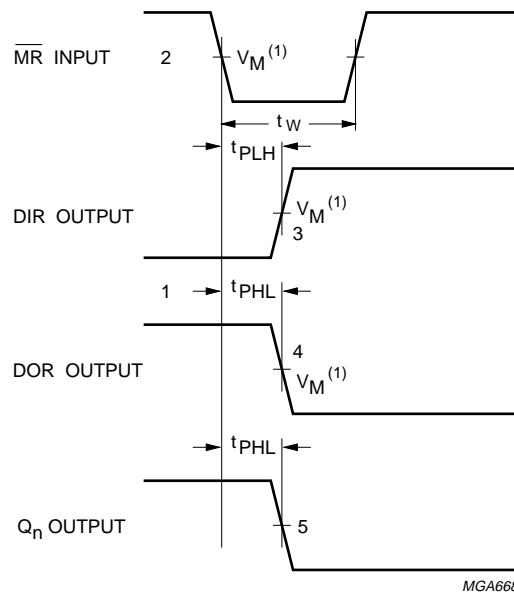
**Notes to Fig.8**

1. FIFO is initially full, shift-in is held HIGH
2.  $\overline{SO}$  pulse; data in the output stage is unloaded, "bubble-up" process of empty location begins
3. DIR HIGH; when empty location reaches input stage, flag indicates FIFO is prepared for data input
4. DIR returns to LOW; data shift-in to empty location is complete, FIFO is full again
5. SI set LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

## 5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404

## Master reset applied with FIFO full



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT :  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

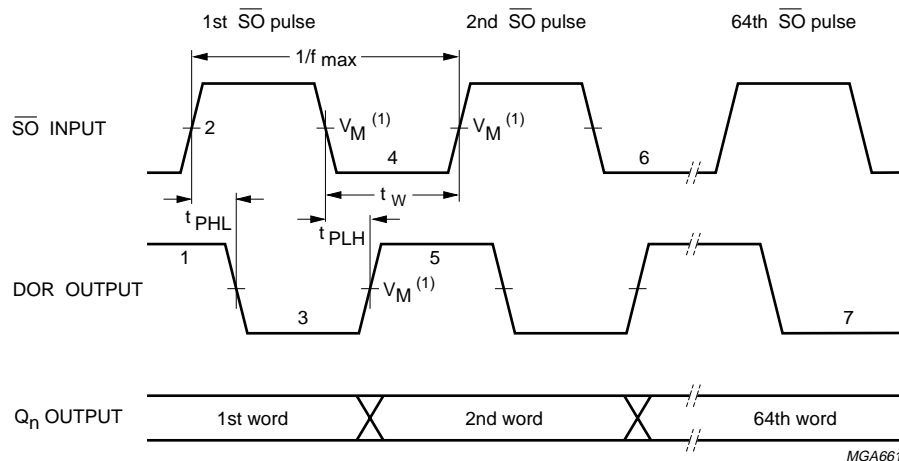
Fig.9 Waveforms showing the  $\overline{\text{MR}}$  input to DIR, DOR and  $Q_n$  output propagation delays and the  $\overline{\text{MR}}$  pulse width.

## Notes to Fig.9

1. DIR LOW, output ready HIGH; assume FIFO is full
2.  $\overline{\text{MR}}$  pulse LOW; clears FIFO
3. DIR goes HIGH; flag indicates input prepared for valid data
4. DOR goes LOW; flag indicates FIFO empty
5.  $Q_n$  outputs go LOW (only last bit will be reset).

## 5-Bit x 64-word FIFO register; 3-state

## 74HC/HCT7404



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT :  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.10 Waveforms showing the  $\overline{S_O}$  input to DOR output propagation delay, the  $\overline{S_O}$  pulse widths and maximum pulse frequency.

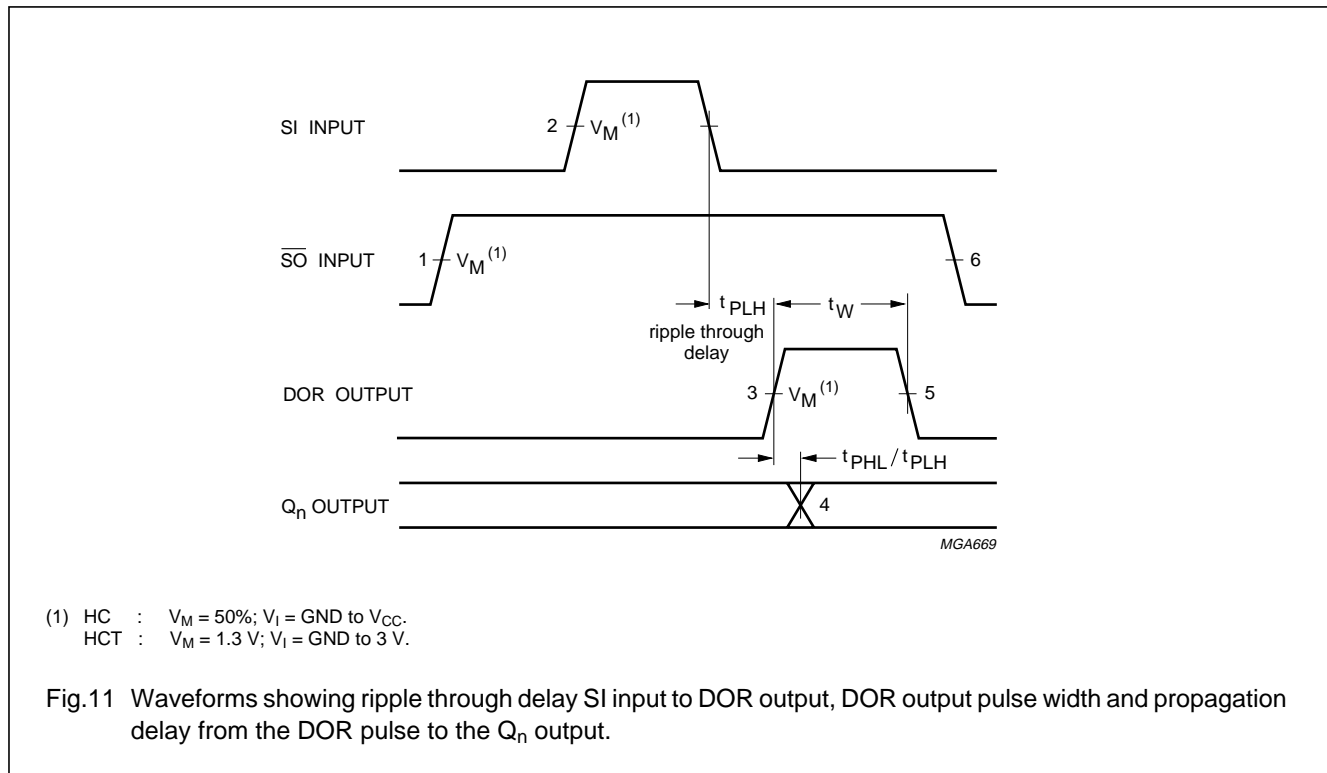
#### Notes to Fig.10

1. DOR HIGH; no data transfer in progress, valid data is present at output stage
2.  $\overline{S_O}$  set HIGH; results in DOR going LOW
3. DOR goes LOW; output stage "busy"
4.  $\overline{S_O}$  set LOW; data in the input stage is unloaded, and new data replaces it as empty location "bubbles-up" to input stage
5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay
6. Repeat process to unload the 3rd through to the 64th word from FIFO.
7. DOR remains LOW; FIFO is empty.

## 5-Bit x 64-word FIFO register; 3-state

## 74HC/HCT7404

With FIFO empty;  $\overline{S\bar{O}}$  is held HIGH in anticipation



**Notes to Fig.11**

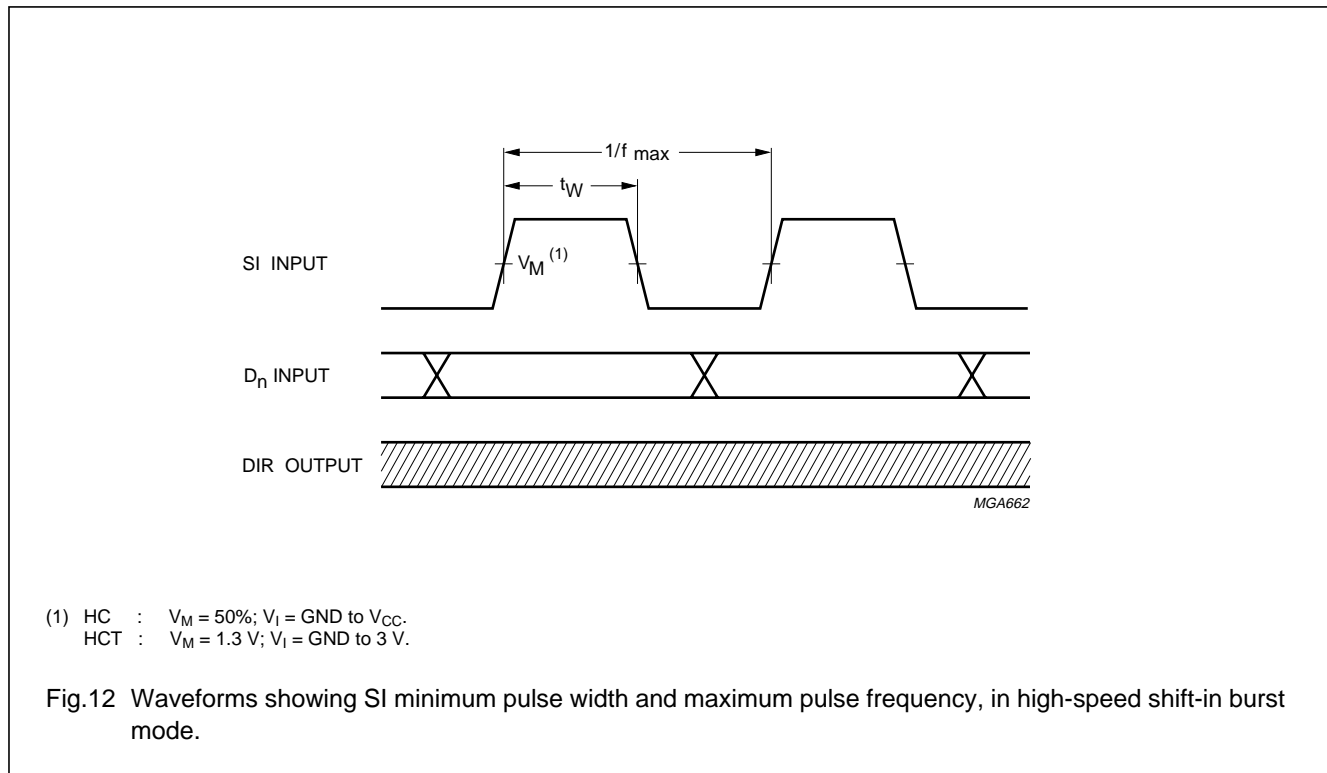
1. FIFO is initially empty,  $\overline{S\bar{O}}$  is held HIGH
2. SI pulse; loads data into FIFO and initiates ripple through process
3. DOR flag signals the arrival of valid data at the output stage
4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the  $Q_n$  output
5. DOR goes LOW; data shift-out is complete, FIFO is empty again
6.  $\overline{S\bar{O}}$  set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.



## 5-Bit x 64-word FIFO register; 3-state

## 74HC/HCT7404

## Shift-in operation; high-speed burst mode

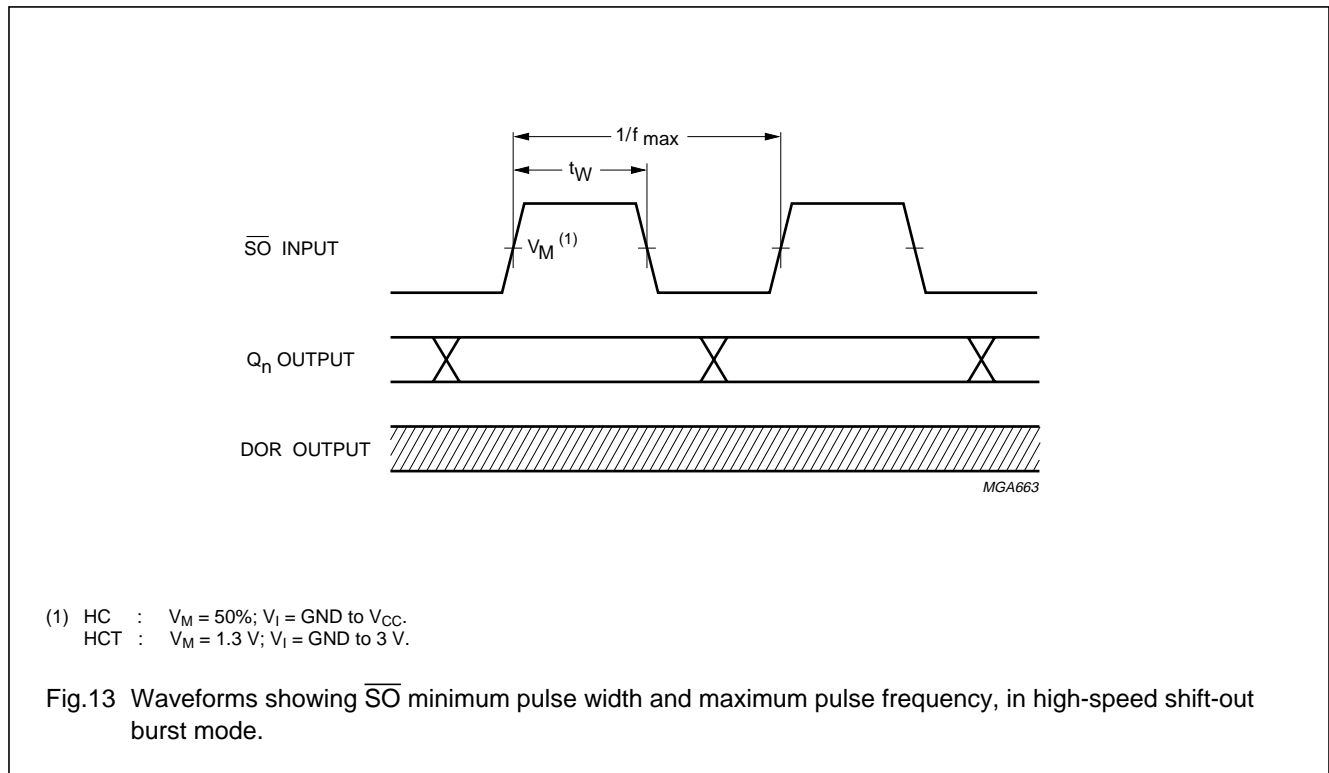
**Note to Fig.12**

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404

Shift-out operation; high-speed burst mode

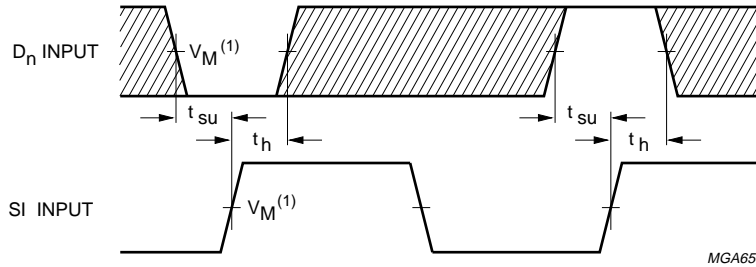


Note to Fig.13

In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and an  $\overline{SO}$  pulse can be applied without regard to the flag.

5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404

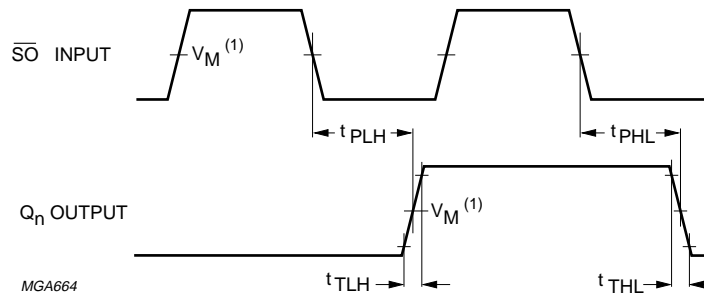


MGA657

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.
- HCT : V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

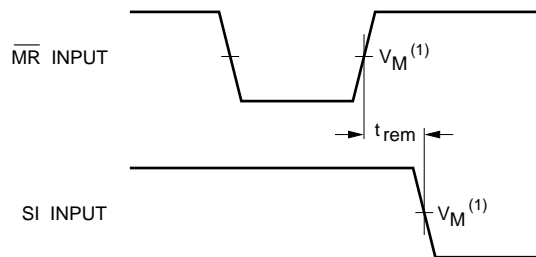
Fig.14 Waveforms showing hold and set-up times for D<sub>n</sub> input to SI input.



MGA664

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.
- HCT : V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

Fig.15 Waveforms showing  $\overline{S}O$  input to Q<sub>n</sub> output propagation delays and output transition time.



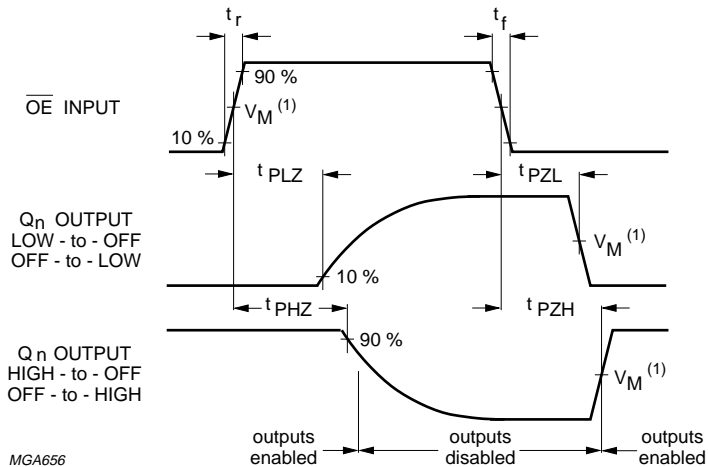
MGA665

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.
- HCT : V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

Fig.16 Waveform showing the  $\overline{M}R$  input to SI input removal time.

5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT :  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.17 Waveforms showing the 3-state enable and disable times for input  $\overline{OE}$ .

5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404

APPLICATION INFORMATION

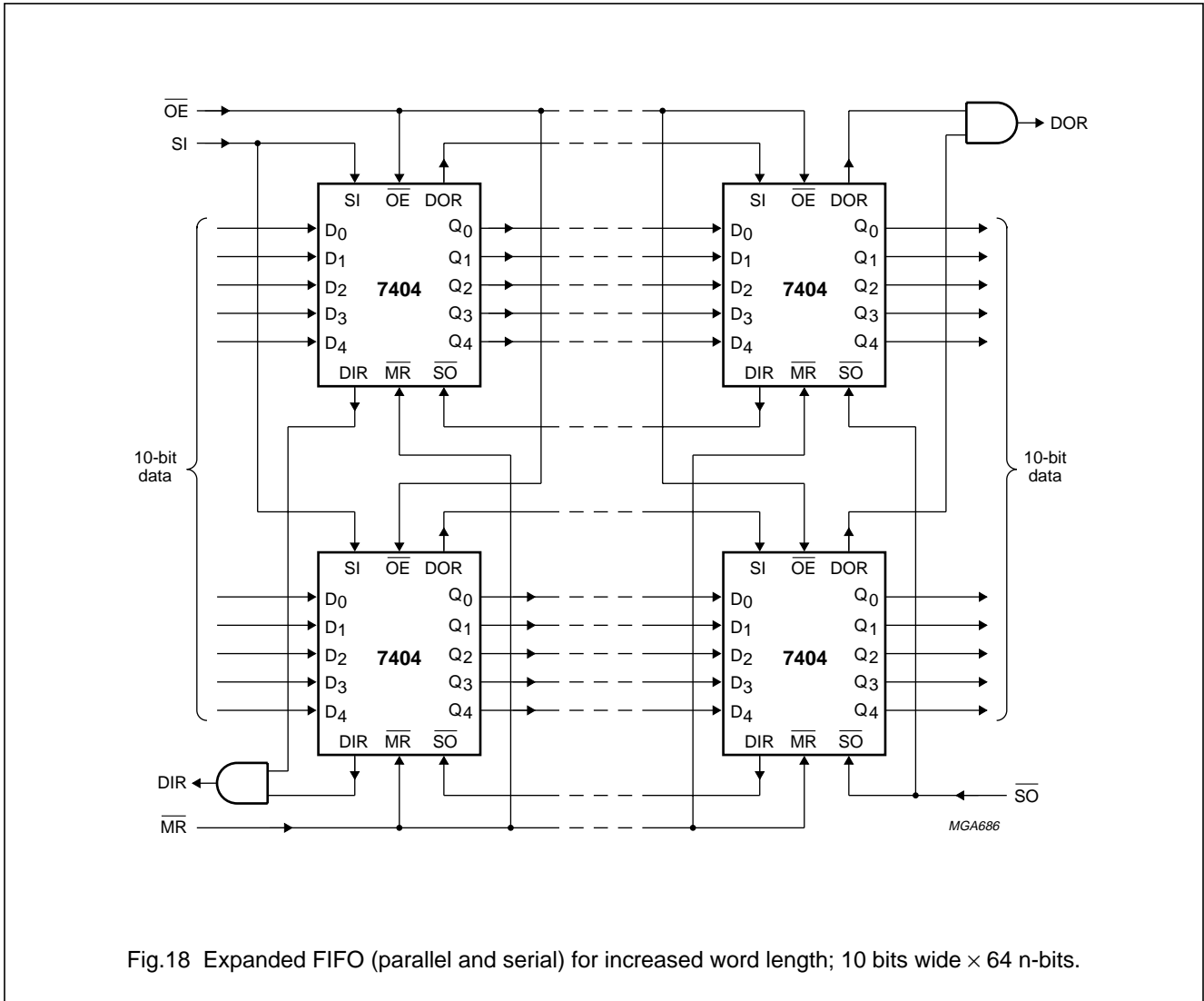


Fig.18 Expanded FIFO (parallel and serial) for increased word length; 10 bits wide x 64 n-bits.

5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404

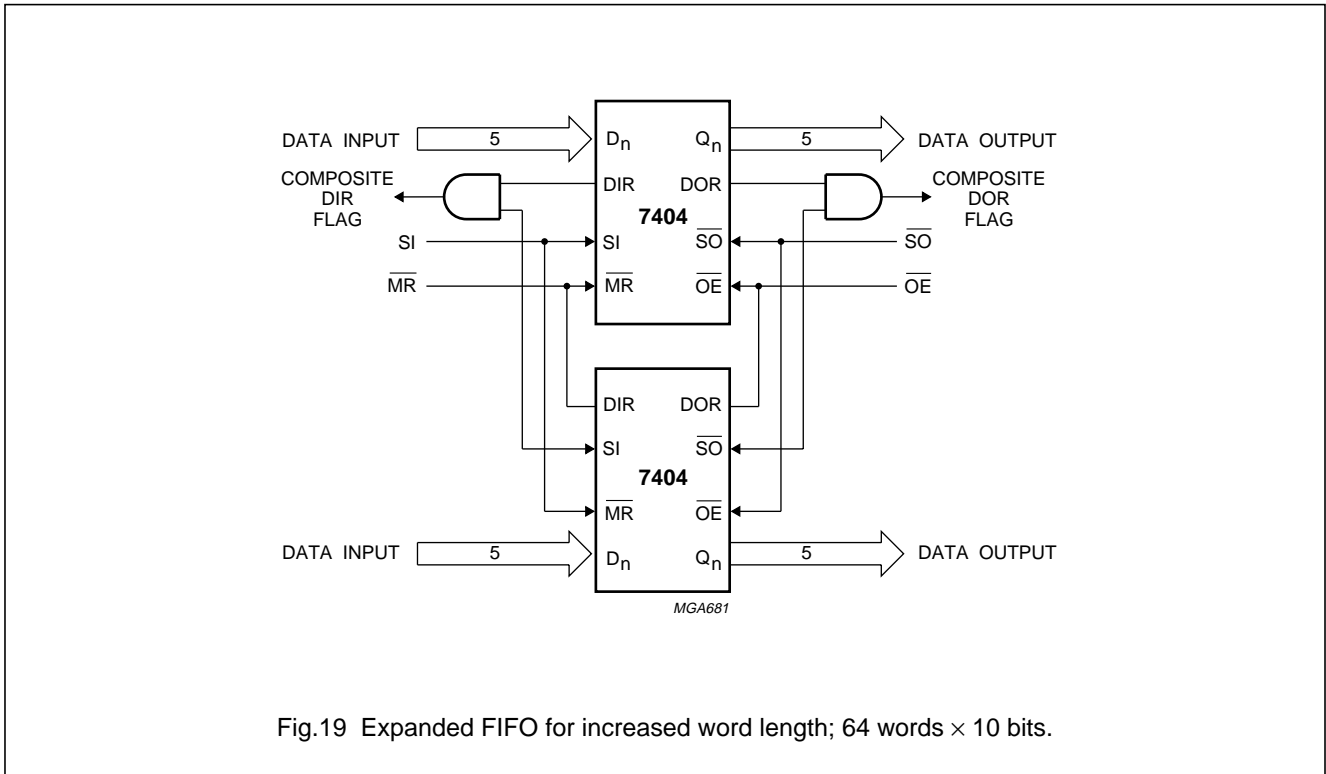


Fig.19 Expanded FIFO for increased word length; 64 words × 10 bits.

**Note to Fig.19**

The "7404" is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404

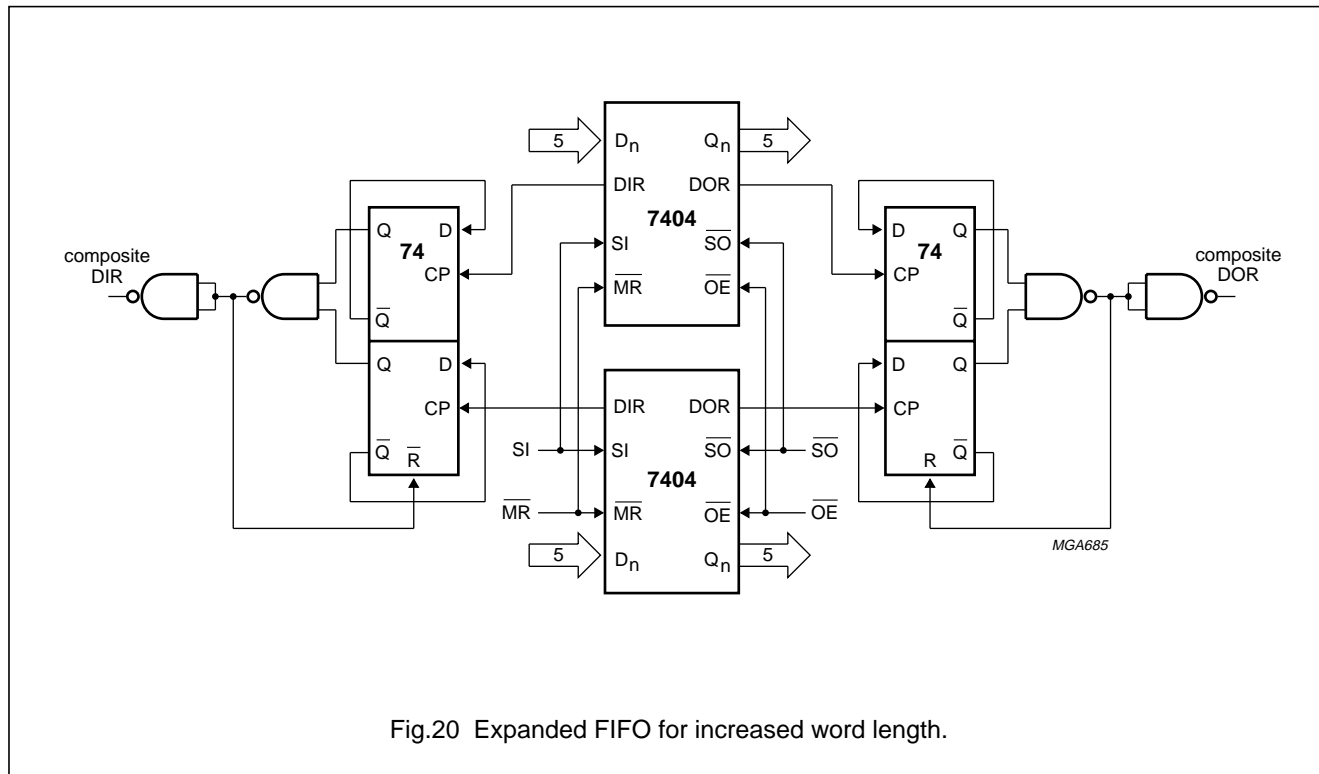


Fig.20 Expanded FIFO for increased word length.

**Note to Fig.20**

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started or if  $\overline{SO}$  output is constantly held HIGH, when the FIFO is full and the automatic shift-out cycles are started (see Fig.8 and Fig.10).

**Expanded format**

Figure 21 shows two cascaded FIFOs providing a capacity of 128 words x 5 bits. Figure 22 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a ripple through delay, data arrives at the output of FIFO<sub>A</sub>. Due to  $\overline{SO}_A$  being HIGH, a DOR<sub>A</sub> pulse is generated. The requirements of SI<sub>B</sub> and D<sub>nB</sub> are satisfied by the DOR<sub>A</sub> pulse width and the timing between the rising edge of DOR<sub>A</sub> and Q<sub>nA</sub>. After a second ripple through delay, data arrives at the output of FIFO<sub>B</sub>.

Figure 23 shows the signals on the nodes of both FIFOs after the application of a  $\overline{SO}_B$  pulse, when both FIFOs are initially full. After a bubble-up delay a DIR<sub>B</sub> pulse is generated, which acts as a  $\overline{SO}_A$  pulse for FIFO<sub>A</sub>. One word is transferred from the output of FIFO<sub>A</sub> to the input of FIFO<sub>B</sub>. The requirements of the  $\overline{SO}_A$  pulse for FIFO<sub>A</sub> is satisfied by the pulse width of DOR<sub>B</sub>. After a second bubble-up delay an empty space arrives at D<sub>nA</sub>, at which time DIR<sub>A</sub> goes HIGH. Figure 24 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.

5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404

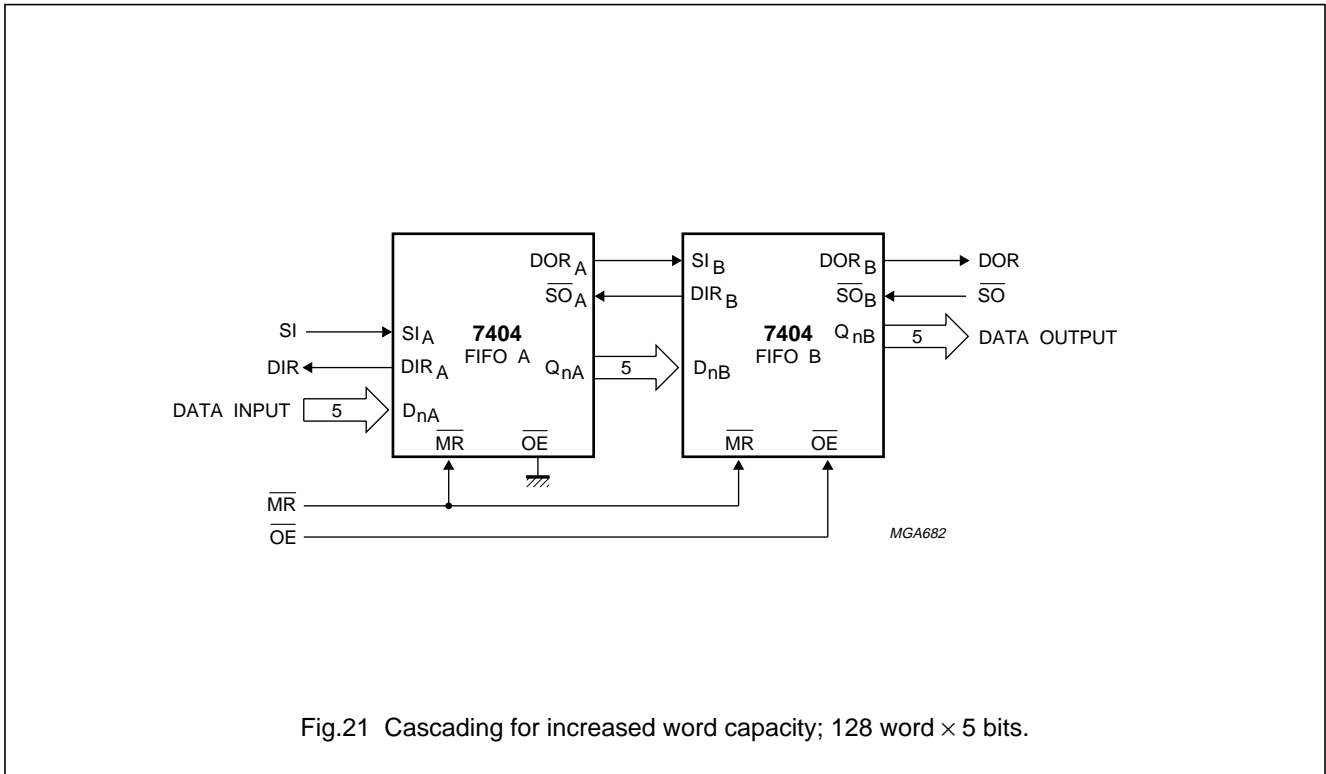


Fig.21 Cascading for increased word capacity; 128 word x 5 bits.

**Note to Fig.21**

The “7404” is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figures 22 and 23 demonstrate the intercommunication timing between FIFO<sub>A</sub> and FIFO<sub>B</sub>. Figure 24 provides an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.



5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404

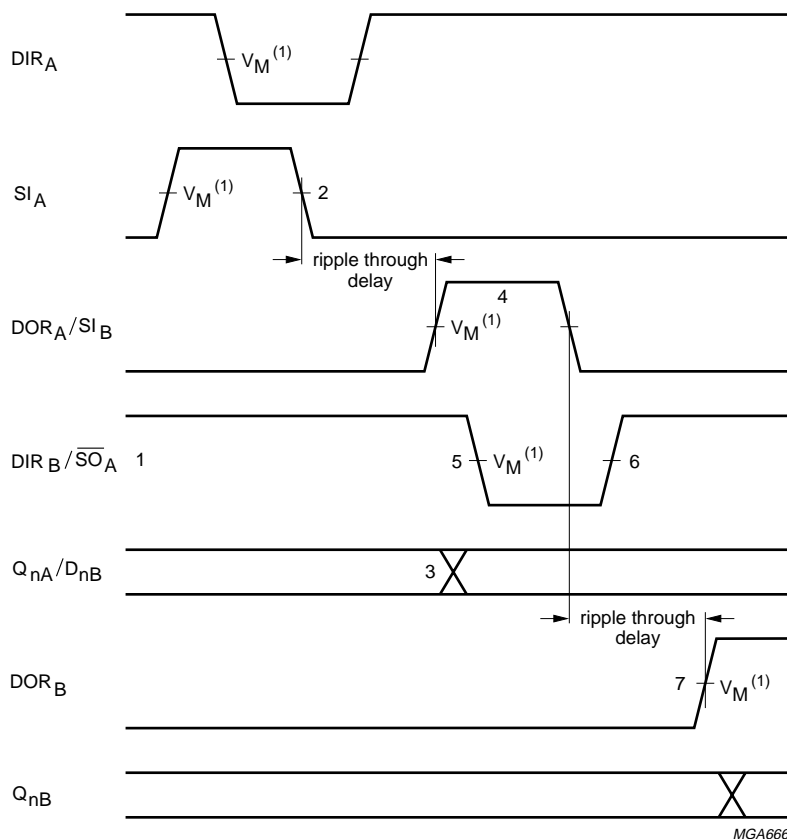


Fig.22 FIFO to FIFO communication; input timing under empty condition.

Notes to Fig.22

1. FIFO<sub>A</sub> and FIFO<sub>B</sub> initially empty,  $\overline{SO}_A$  held HIGH in anticipation of data
2. Load one word into FIFO<sub>A</sub>; SI pulse applied, results in DIR pulse
3. Data-out<sub>A</sub>/data-in<sub>B</sub> transition; valid data arrives at FIFO<sub>A</sub> output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFO<sub>B</sub>
4. DOR<sub>A</sub> and SI<sub>B</sub> pulse HIGH; (ripple through delay after SI<sub>A</sub> LOW) data is unloaded from FIFO<sub>A</sub> as a result of the data output ready pulse, data is shifted into FIFO<sub>B</sub>
5. DIR<sub>B</sub> and  $\overline{SO}_A$  go LOW; flag indicates input stage of FIFO<sub>B</sub> is busy, shift-out of FIFO<sub>A</sub> is complete
6. DIR<sub>B</sub> and  $\overline{SO}_A$  go HIGH automatically; the input stage of FIFO<sub>B</sub> is again able to receive data,  $\overline{SO}$  is held HIGH in anticipation of additional data
7. DOR<sub>B</sub> goes HIGH; (ripple through delay after SI<sub>B</sub> LOW) valid data is present one propagation delay later at the FIFO<sub>B</sub> output stage.

## 5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404

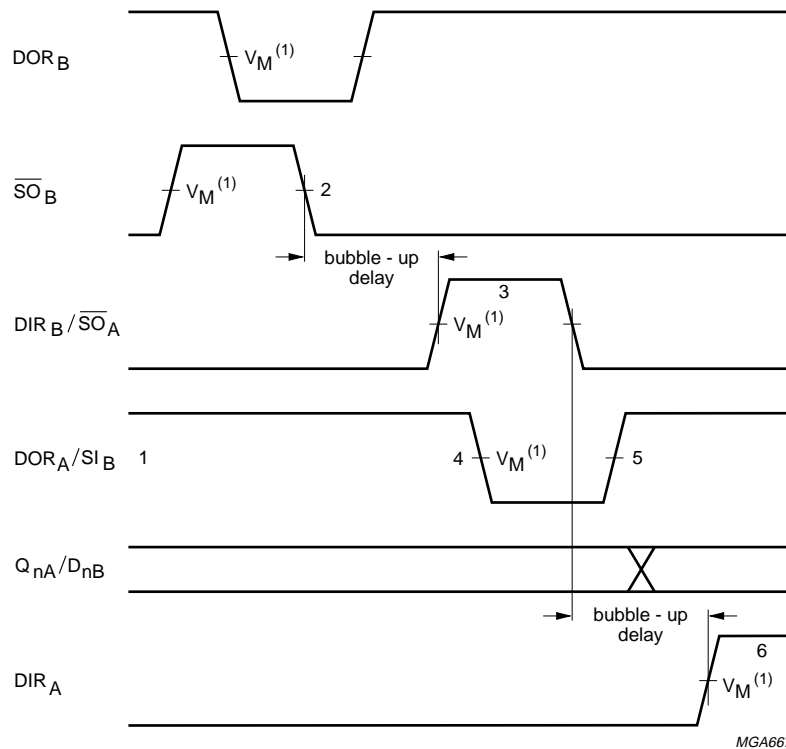


Fig.23 FIFO to FIFO communication; output timing under full condition.

**Notes to Fig.23**

1. FIFO<sub>A</sub> and FIFO<sub>B</sub> initially full, SI<sub>B</sub> held HIGH in anticipation of shifting in new data as an empty location bubbles-up
2. Unload one word from FIFO<sub>B</sub>;  $\overline{SO}$  pulse applied, results in DOR pulse
3. DIR<sub>B</sub> and  $\overline{SO}_A$  pulse HIGH; (bubble-up delay after  $\overline{SO}_B$  LOW) data is loaded into FIFO<sub>B</sub> as a result of the DIR pulse, data is shifted out of FIFO<sub>A</sub>
4. DOR<sub>A</sub> and SI<sub>B</sub> go LOW; flag indicates the output stage of FIFO<sub>A</sub> is busy, shift-in to FIFO<sub>B</sub> is complete
5. DOR<sub>A</sub> and SI<sub>B</sub> go HIGH; flag indicates valid data is again available at FIFO<sub>A</sub> output stage, SI<sub>B</sub> is held HIGH, awaiting bubble-up of empty location
6. DIR<sub>A</sub> goes HIGH; (bubble-up delay after  $\overline{SO}_A$  LOW) an empty location is present at input stage of FIFO<sub>A</sub>.

5-Bit x 64-word FIFO register; 3-state

74HC/HCT7404

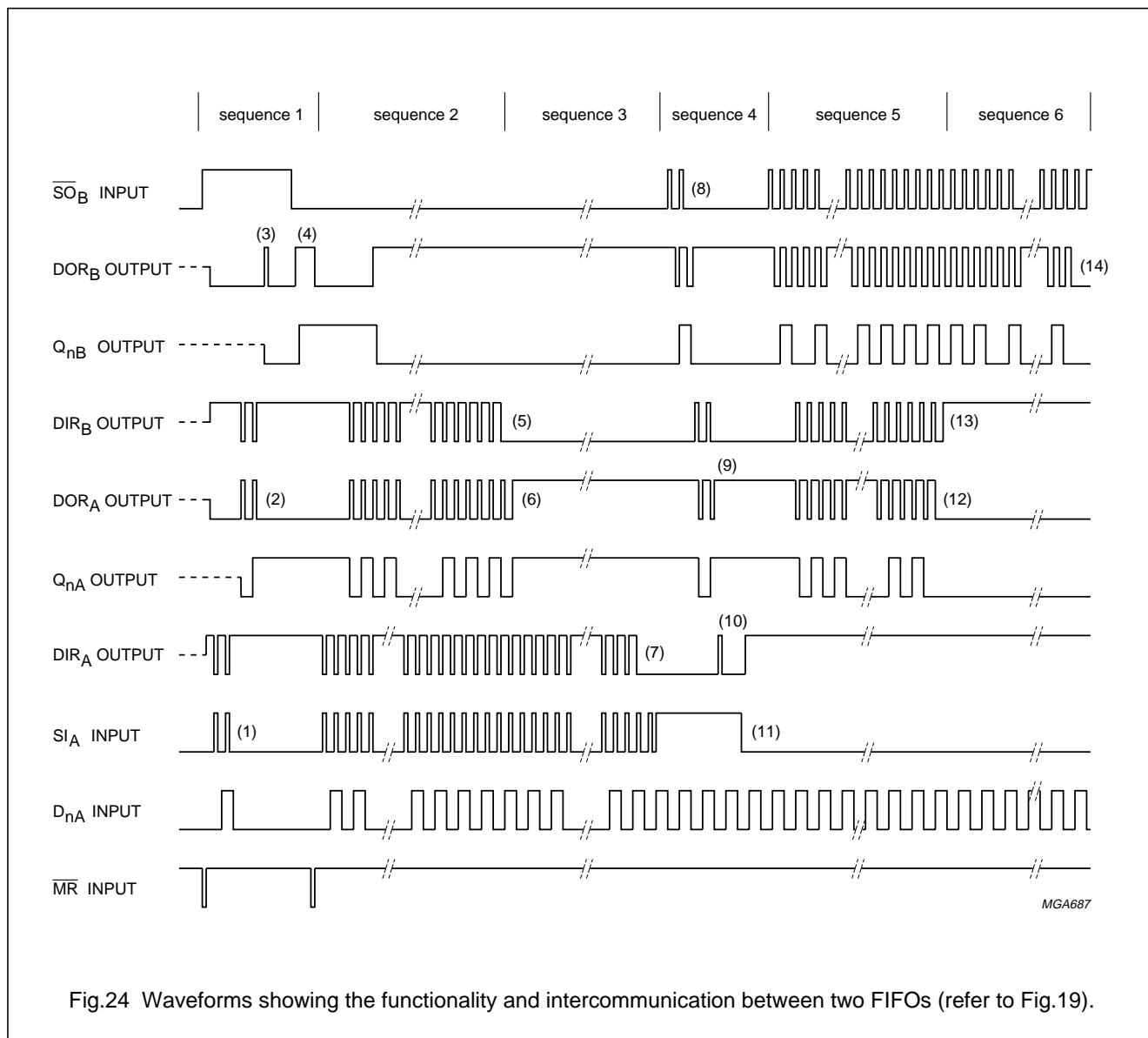


Fig.24 Waveforms showing the functionality and intercommunication between two FIFOs (refer to Fig.19).

**Note to Fig.24**

**Sequence 1 (both FIFOs empty, starting SHIFT-IN process)**

After a  $\overline{M}_R$  pulse has been applied  $FIFO_A$  and  $FIFO_B$  are empty. The  $DOR$  flags of  $FIFO_A$  and  $FIFO_B$  go LOW due to no valid data being present at the outputs. The  $DIR$  flags are set HIGH due to the FIFOs being ready to accept data.  $\overline{S}_O_B$  is held HIGH and two  $S_{IA}$  pulses are applied (1). These pulses allow two data words to ripple through to the output stage of  $FIFO_A$  and to the input stage of  $FIFO_B$  (2). When data arrives at the output of  $FIFO_B$ , a  $DOR_B$  pulse is generated (3). When  $\overline{S}_O_B$  goes LOW, the first bit is shifted out and a second bit ripples through to the output after which  $DOR_B$  goes HIGH (4).

## 5-Bit x 64-word FIFO register; 3-state

## 74HC/HCT7404

**Sequence 2 (FIFO<sub>B</sub> runs full)**

After the  $\overline{\text{MR}}$  pulse, a series of 64 SI pulses are applied. When 64 words are shifted in, DIR<sub>B</sub> remains LOW due to FIFO<sub>B</sub> being full (5). DOR<sub>A</sub> goes LOW due to FIFO<sub>A</sub> being empty.

**Sequence 3 (FIFO<sub>A</sub> runs full)**

When 65 words are shifted in, DOR<sub>A</sub> remains HIGH due to valid data remaining at the output of FIFO<sub>A</sub>. Q<sub>nA</sub> remains HIGH, being the polarity of the 65th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

**Sequence 4 (both FIFOs full, starting SHIFT-OUT process)**

SI<sub>A</sub> is held HIGH and two  $\overline{\text{SO}}_{\text{B}}$  pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of FIFO<sub>B</sub>, and proceed to FIFO<sub>A</sub> (9). When the first empty location arrives at the input of FIFO<sub>A</sub>, a DIR<sub>A</sub> pulse is generated (10) and a new word is shifted into FIFO<sub>A</sub>. SI<sub>A</sub> is made LOW and now the second empty location reaches the input stage of FIFO<sub>A</sub>, after which DIR<sub>A</sub> remains HIGH (11).

**Sequence 5 (FIFO<sub>A</sub> runs empty)**

At the start of sequence 5 FIFO<sub>A</sub> contains 63 valid words due to two words being shifted out and one word being shifted in, in sequence 4. An additional series of  $\overline{\text{SO}}_{\text{B}}$  pulses are applied. After 63  $\overline{\text{SO}}_{\text{B}}$  pulses, all words from FIFO<sub>A</sub> are shifted into FIFO<sub>B</sub>. DOR<sub>A</sub> remains LOW (12).

**Sequence 6 (FIFO<sub>B</sub> runs empty)**

After the next  $\overline{\text{SO}}_{\text{B}}$  pulse, DIR<sub>B</sub> remains HIGH due to the input stage of FIFO<sub>B</sub> being empty. After another 63  $\overline{\text{SO}}_{\text{B}}$  pulses, DOR<sub>B</sub> remains LOW due to both FIFOs being empty (14). Additional  $\overline{\text{SO}}_{\text{B}}$  pulses have no effect. The last word remains available at the output Q<sub>n</sub>.

**PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.