

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT147** 10-to-4 line priority encoder

Product specification  
File under Integrated Circuits, IC06

December 1990

## 10-to-4 line priority encoder

## 74HC/HCT147

## FEATURES

- Encodes 10-line decimal to 4-line BCD
- Useful for 10-position switch encoding
- Used in code converters and generators
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT147 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT147 9-input priority encoders accept data from nine active LOW inputs ( $\bar{A}_0$  to  $\bar{A}_8$ ) and provide a binary representation on the four active LOW outputs ( $\bar{Y}_0$  to  $\bar{Y}_3$ ). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line  $\bar{A}_8$  having the highest priority.

The devices provide the 10-line to 4-line priority encoding function by use of the implied decimal "zero". The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{A}_n$ to $\bar{Y}_n$	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	15	17	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	30	33	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

## ORDERING INFORMATION

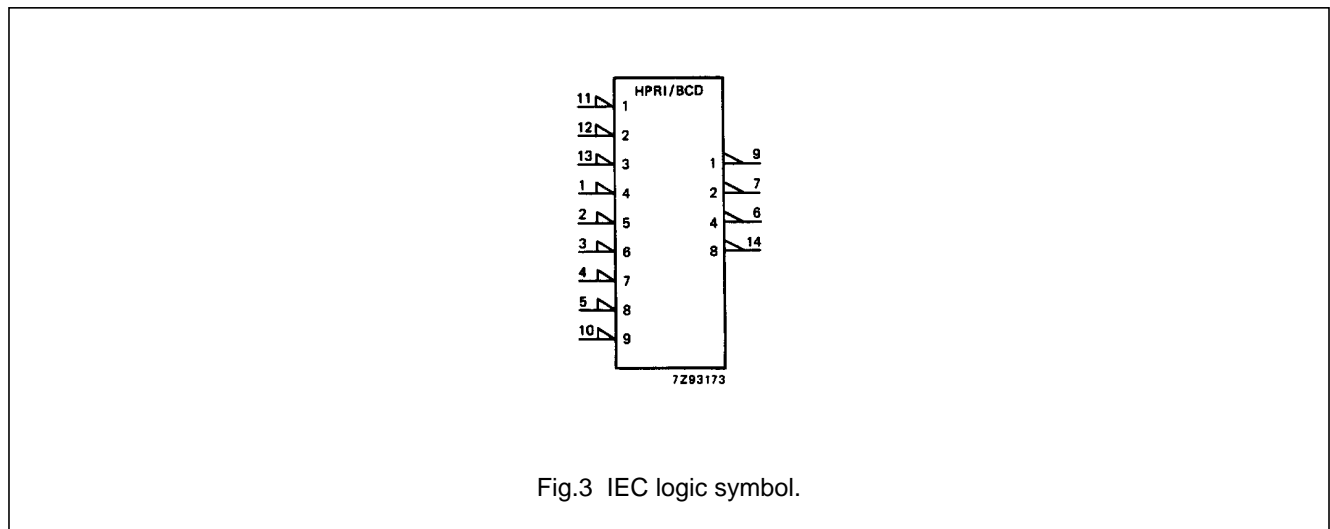
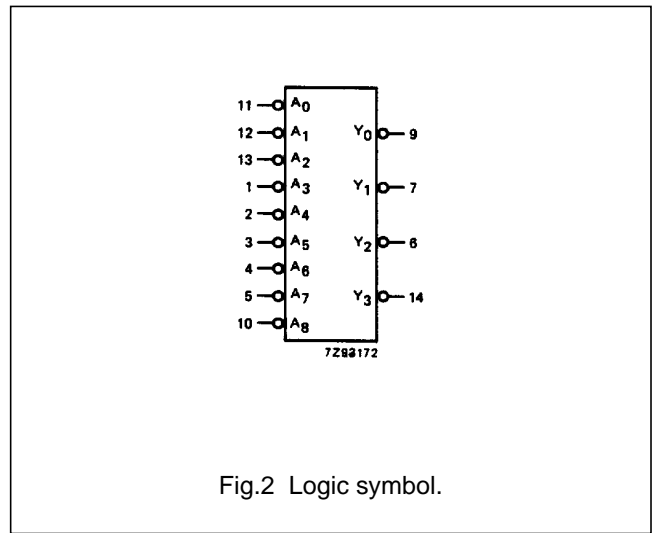
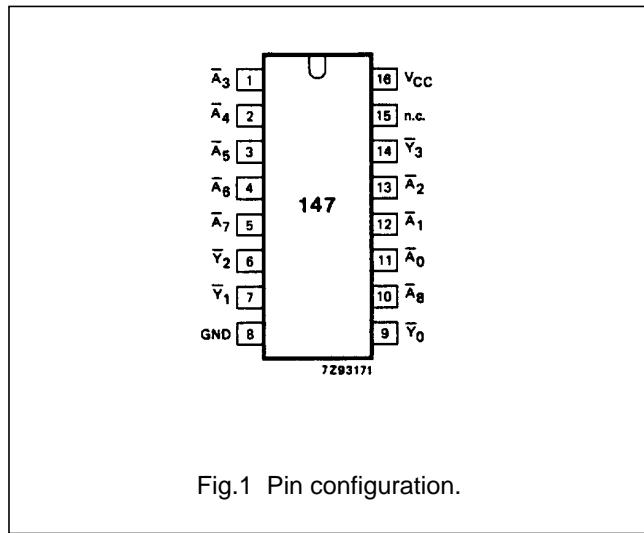
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 14	$\bar{Y}_0$ to $\bar{Y}_3$	BCD address outputs (active LOW)
11, 12, 13, 1, 2, 3, 4, 5, 10	$\bar{A}_0$ to $\bar{A}_8$	decimal data inputs (active LOW)
15	n.c.	not connected
16	V <sub>CC</sub>	positive supply voltage



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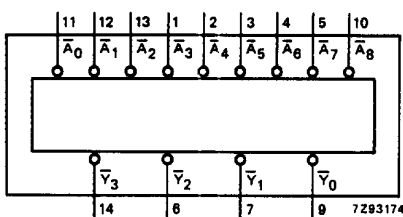


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS									OUTPUTS			
$\bar{A}_0$	$\bar{A}_1$	$\bar{A}_2$	$\bar{A}_3$	$\bar{A}_4$	$\bar{A}_5$	$\bar{A}_6$	$\bar{A}_7$	$\bar{A}_8$	$\bar{Y}_3$	$\bar{Y}_2$	$\bar{Y}_1$	$\bar{Y}_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Notes

1. H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care

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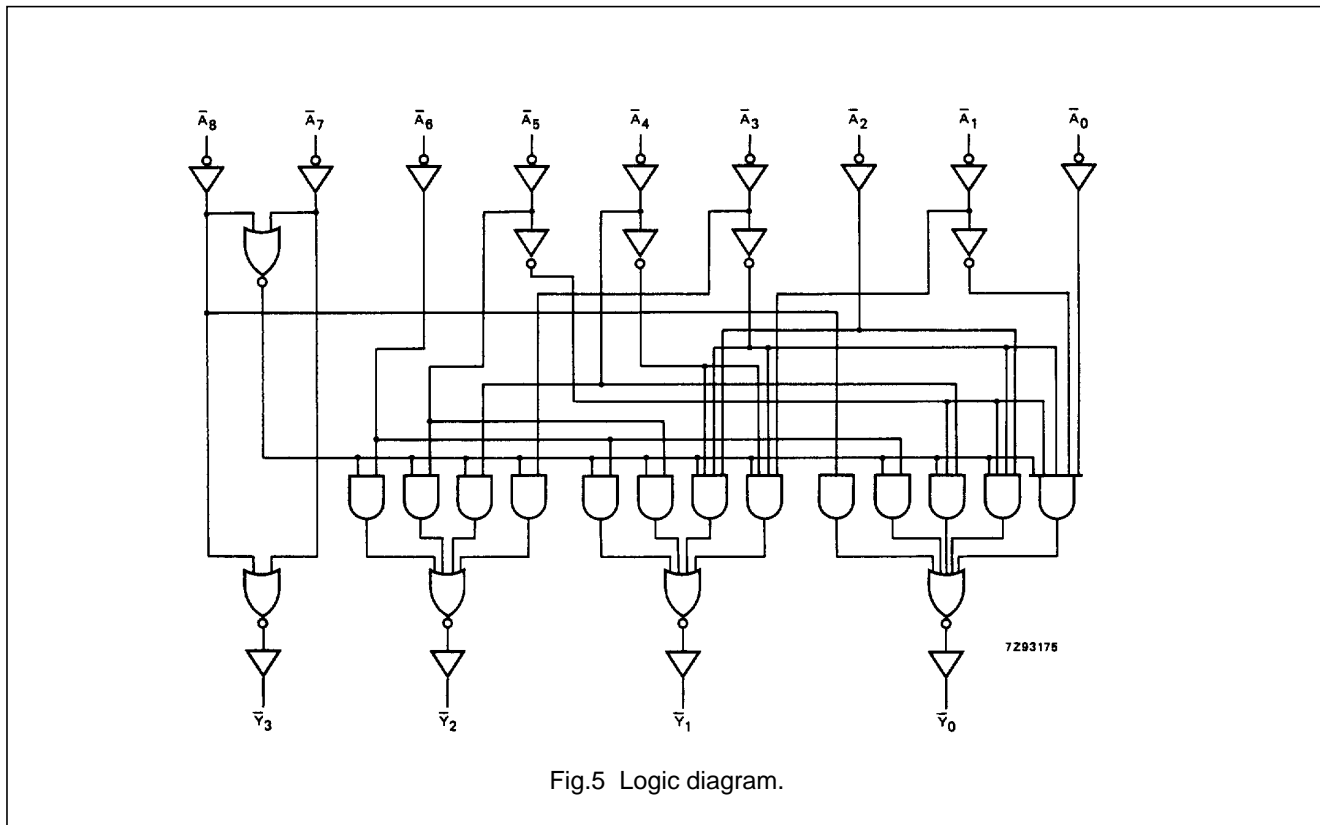


Fig.5 Logic diagram.

## 10-to-4 line priority encoder

## 74HC/HCT147

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{A}_n$ to $\bar{Y}_n$		50 18 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 6		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard  
 $I_{CC}$  category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

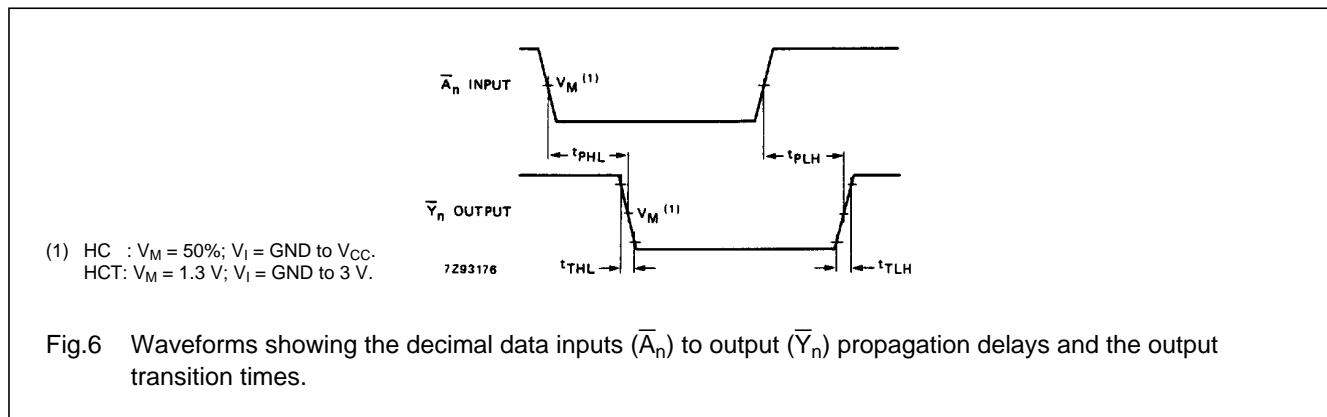
INPUT	UNIT LOAD COEFFICIENT
$\bar{A}_3, \bar{A}_4, \bar{A}_7, \bar{A}_8$	1.50
$\bar{A}_5, \bar{A}_6, \bar{A}_0, \bar{A}_1, \bar{A}_2$	1.10

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL} / t_{PLH}$	propagation delay $\bar{A}_n$ to $\bar{Y}_n$		20	35		44		53	ns	4.5	Fig.6
$t_{THL} / t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig.6

## AC WAVEFORMS



## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.