# 74HC175; 74HCT175

## Quad D-type flip-flop with reset; positive-edge trigger

Rev. 4 — 8 April 2014 Product data sheet

## 1. General description

The 74HC175; 74HCT175 are quad positive edge-triggered D-type flip-flops with individual data inputs (Dn) and both Qn and $\overline{Q}$n outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset all flip-flops simultaneously. The D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition is stored in the flip-flop and appears at the Q output. A LOW on $\overline{MR}$ causes the flip-flops and outputs to be reset LOW.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

## 2. Features and benefits

- Input levels:
  - For 74HC175: CMOS level
  - For 74HCT175: TTL level
- Four edge-triggered D-type flip-flops
- Asynchronous master reset
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C.

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74HC175N | −40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74HCT175N | | | | |
| 74HC175D | −40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HCT175D | | | | |
| 74HC175DB | −40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HCT175DB | | | | |
| 74HC175PW | −40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT175PW | | | | |

## 4. Functional diagram

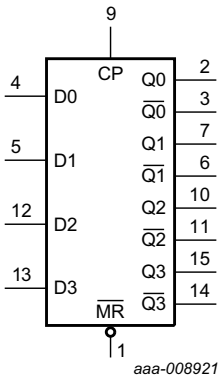



Fig 1. Logic symbol

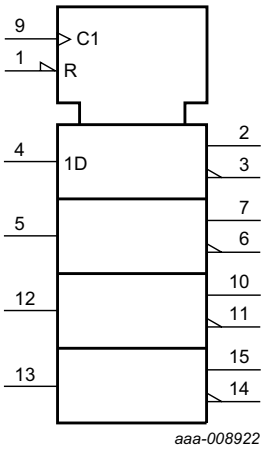



Fig 2. IEC logic symbol

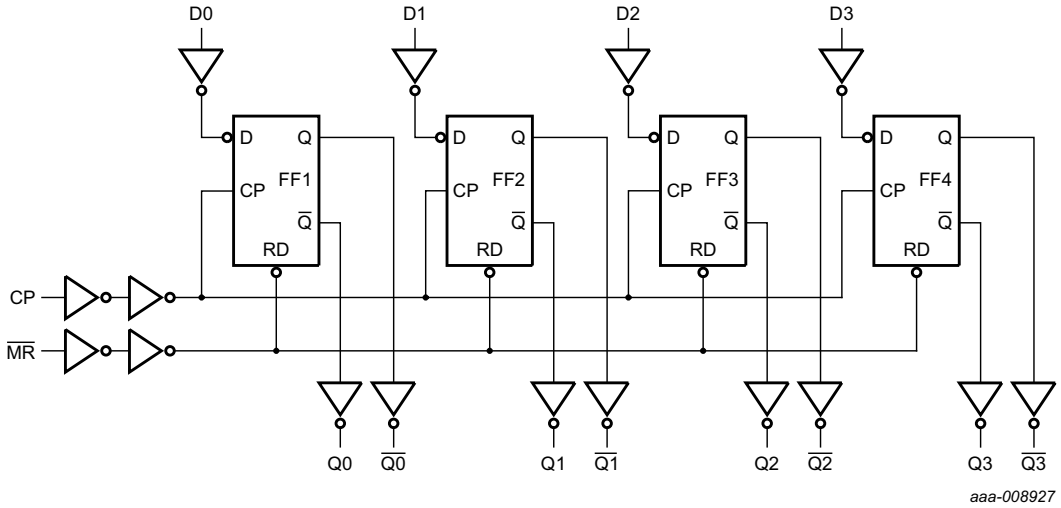



Fig 3. Logic diagram

# 5. Pinning information

## 5.1 Pinning

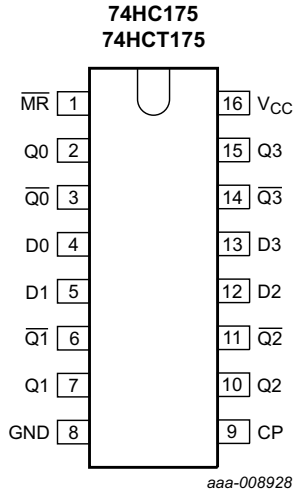



Fig 4. Pin configuration DIP16

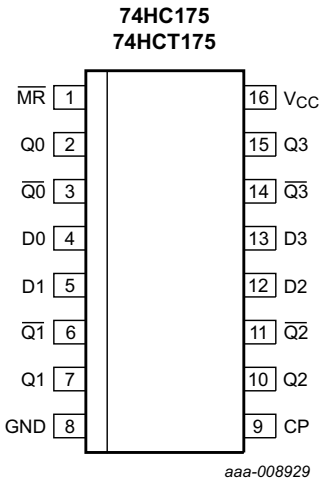



Fig 5. Pin configuration SO16

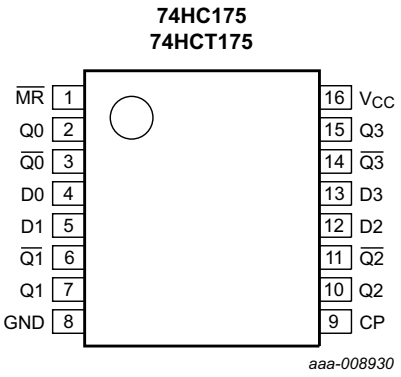



Fig 6. Pin configuration SSOP16 and TSSOP16

## 5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|---|---|
| $\overline{MR}$ | 1 | asynchronous master reset input (active LOW) |
| Q0 to Q3 | 2, 7, 10, 15 | flip-flop output |
| $\overline{Q0}$ to $\overline{Q3}$ | 3, 6, 11, 14 | complementary flip-flop output |
| D0 to D3 | 4, 5, 12, 13 | data input |
| GND | 8 | ground (0 V) |
| CP | 9 | clock input (LOW-to-HIGH edge-triggered) |
| $V_{CC}$ | 16 | positive supply voltage |

# 6. Functional description

**Table 3. Function table[1]**

| Operating modes | Inputs | | | Outputs | |
|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | Dn | Qn | $\overline{Qn}$ |
| reset (clear) | L | X | X | L | H |
| load “1” | H | ↑ | h | H | L |
| load “0” | H | ↑ | l | L | H |

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
X = don’t care;
↑ = LOW-to-HIGH clock transition.

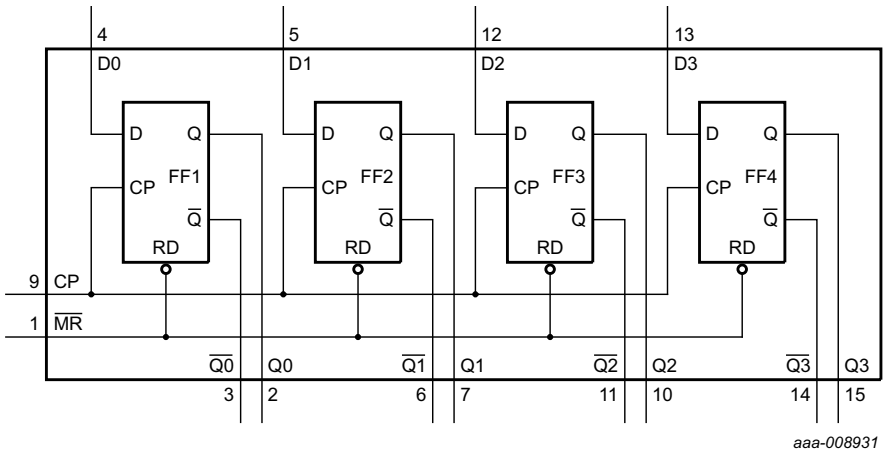



**Fig 7. Functional diagram**

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | −0.5 | +7 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | - | ±20 | mA |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | - | ±20 | mA |
| $I_O$ | output current | $-0.5$ V $< V_O < V_{CC} + 0.5$ V | - | ±25 | mA |
| $I_{CC}$ | supply current | | - | 50 | mA |
| $I_{GND}$ | ground current | | −50 | - | mA |
| $T_{stg}$ | storage temperature | | −65 | +150 | °C |

**Table 4. Limiting values** *...continued*

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +125 °C | | | |
| | | DIP16 package [1] | - | 750 | mW |
| | | SO16, SSOP16 and TSSOP16 [2] | - | 500 | mW |

[1] For DIP16 package: above 70 °C the value of $P_{tot}$ derates linearly with 12 mW/K.

[2] For SO16 package: above 70 °C the value of $P_{tot}$ derates linearly with 8 mW/K.
For SSOP16 and TSSOP16 packages: above 60 °C the value of $P_{tot}$ derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V)*

| Symbol | Parameter | Conditions | 74HC175 | | | 74HCT175 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | −40 | - | +125 | −40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | $V_{CC}$ = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | $V_{CC}$ = 6.0 V | - | - | 83 | - | - | - | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74HC175** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | $V_{CC}$ = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | $V_{CC}$ = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = −20 μA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = −20 μA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = −20 μA; $V_{CC}$ = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | $I_O$ = −4.0 mA; $V_{CC}$ = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | $I_O$ = −5.2 mA; $V_{CC}$ = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |

**Table 6. Static characteristics** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 20 μA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 μA; $V_{CC}$ = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $I_O$ = 5.2 mA; $V_{CC}$ = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| **74HCT175** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = –20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –4.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = 20 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 5.2 mA; $V_{CC}$ = 5.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | Dn input | - | 40 | 144 | - | 180 | - | 196 | μA |
| | | CP input | - | 60 | 216 | - | 270 | - | 294 | μA |
| | | $\overline{MR}$ input | - | 100 | 360 | - | 450 | - | 490 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND (ground = 0 V); $C_L$ = 50 pF unless otherwise specified; for test circuit, see Figure 11*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74HC175** | | | | | | | | | | |
| $t_{pd}$ | propagation delay | CP to Qn, $\overline{Q}n$; see Figure 8 [1] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 55 | 175 | - | 220 | - | 265 | ns |
| | | $V_{CC}$ = 4.5 V | - | 20 | 35 | - | 44 | - | 53 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 17 | - | - | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | - | 16 | 30 | - | 37 | - | 45 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | $\overline{MR}$ to Qn, $\overline{Q}n$; see Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 50 | 150 | - | 190 | - | 225 | ns |
| | | $V_{CC}$ = 4.5 V | - | 18 | 30 | - | 38 | - | 45 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 15 | - | - | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | - | 14 | 26 | - | 33 | - | 38 | ns |
| $t_t$ | transition time | Qn output; see Figure 8 [2] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | $V_{CC}$ = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC}$ = 6.0 V | - | 6 | 13 | - | 16 | - | 19 | ns |
| $t_W$ | pulse width | CP input HIGH or LOW; see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 80 | 22 | - | 100 | - | 120 | - | ns |
| | | $V_{CC}$ = 4.5 V | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | $V_{CC}$ = 6.0 V | 14 | 6 | - | 17 | - | 20 | - | ns |
| | | $\overline{MR}$ input LOW; see Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 80 | 19 | - | 100 | - | 120 | - | ns |
| | | $V_{CC}$ = 4.5 V | 16 | 7 | - | 20 | - | 24 | - | ns |
| | | $V_{CC}$ = 6.0 V | 14 | 6 | - | 17 | - | 20 | - | ns |
| $t_{rec}$ | recovery time | $\overline{MR}$ to CP; see Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 5 | –33 | - | 5 | - | 5 | - | ns |
| | | $V_{CC}$ = 4.5 V | 5 | –12 | - | 5 | - | 5 | - | ns |
| | | $V_{CC}$ = 6.0 V | 5 | –10 | - | 5 | - | 5 | - | ns |
| $t_{su}$ | set-up time | Dn to CP; see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 80 | 3 | - | 100 | - | 120 | - | ns |
| | | $V_{CC}$ = 4.5 V | 16 | 1 | - | 20 | - | 24 | - | ns |
| | | $V_{CC}$ = 6.0 V | 14 | 1 | - | 17 | - | 20 | - | ns |

**Table 7. Dynamic characteristics** *...continued*

*GND (ground = 0 V); $C_L$ = 50 pF unless otherwise specified; for test circuit, see Figure 11*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_h$ | hold time | Dn to CP; see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 25 | 2 | - | 30 | - | 40 | - | ns |
| | | $V_{CC}$ = 4.5 V | 5 | 0 | - | 6 | - | 8 | - | ns |
| | | $V_{CC}$ = 6.0 V | 4 | 0 | - | 5 | - | 7 | - | ns |
| $f_{max}$ | maximum frequency | CP input; see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 6 | 25 | - | 4.8 | - | 4 | - | MHz |
| | | $V_{CC}$ = 4.5 V | 30 | 75 | - | 24 | - | 20 | - | MHz |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 83 | - | - | - | - | - | MHz |
| | | $V_{CC}$ = 6.0 V | 35 | 89 | - | 28 | - | 24 | - | MHz |
| $C_{PD}$ | power dissipation capacitance | per package; $V_I$ = GND to $V_{CC}$ [3] | - | 32 | - | - | - | - | - | pF |
| **74HCT175** | | | | | | | | | | |
| $t_{pd}$ | propagation delay | CP to Qn, $\overline{Q}$n; see Figure 8 [1] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 19 | 33 | - | 41 | - | 50 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 16 | - | - | - | - | - | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | $\overline{MR}$ to Qn; see Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 22 | 38 | - | 48 | - | 57 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 19 | - | - | - | - | - | ns |
| | | $\overline{MR}$ to $\overline{Q}$n; see Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 19 | 35 | - | 44 | - | 53 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 16 | - | - | - | - | - | ns |
| $t_t$ | transition time | Qn output; see Figure 8 [2] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| $t_W$ | pulse width | CP input; see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 20 | 12 | - | 25 | - | 30 | - | ns |
| | | $\overline{MR}$ input LOW; see Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 20 | 11 | - | 25 | - | 30 | - | ns |
| $t_{rec}$ | recovery time | $\overline{MR}$ to CP; see Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 5 | –10 | - | 5 | - | 5 | - | ns |
| $t_{su}$ | set-up time | Dn to CP; see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 16 | 5 | - | 20 | - | 24 | - | ns |
| $t_h$ | hold time | Dn to CP; see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 5 | 0 | - | 5 | - | 5 | - | ns |

**Table 7. Dynamic characteristics** *...continued*

*GND (ground = 0 V); $C_L$ = 50 pF unless otherwise specified; for test circuit, see Figure 11*

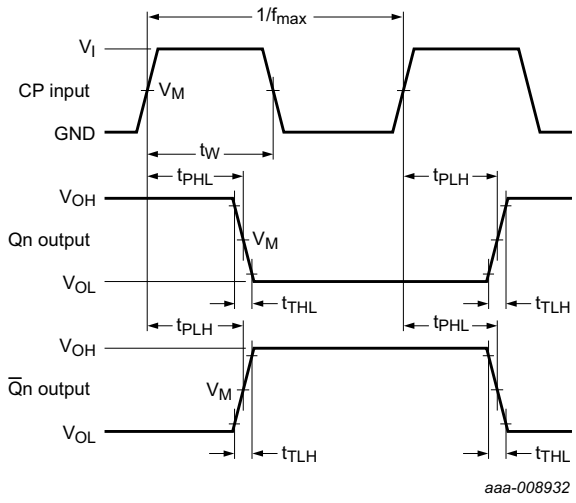
| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $f_{max}$ | maximum frequency | CP input; see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 25 | 49 | - | 20 | - | 17 | - | MHz |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 54 | - | - | - | - | - | MHz |
| $C_{PD}$ | power dissipation capacitance | per package; $V_I$ = GND to $V_{CC}$ − 1.5 V [3] | - | 34 | - | - | - | - | - | pF |

[1] $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.

[2] $t_t$ is the same as $t_{THL}$ and $t_{TLH}$.

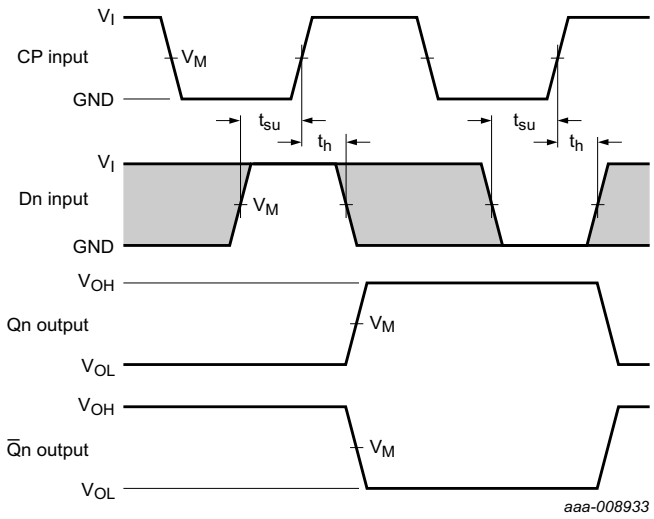
[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V.

## 11. Waveforms



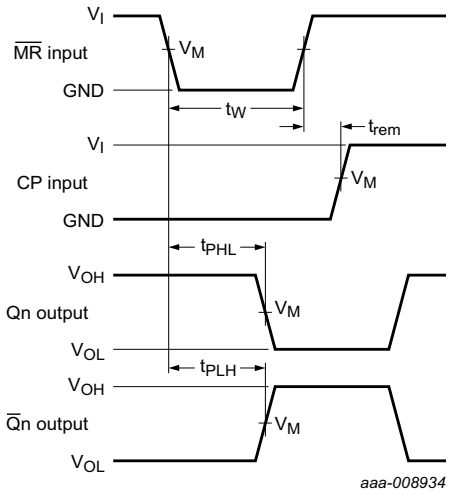

Measurement points are given in Table 8.

**Fig 8. Input to output propagation delay, output transition time, clock input pulse width and maximum frequency**




Measurement points are given in Table 8.

**Fig 9. Data set-up and hold times for data input**

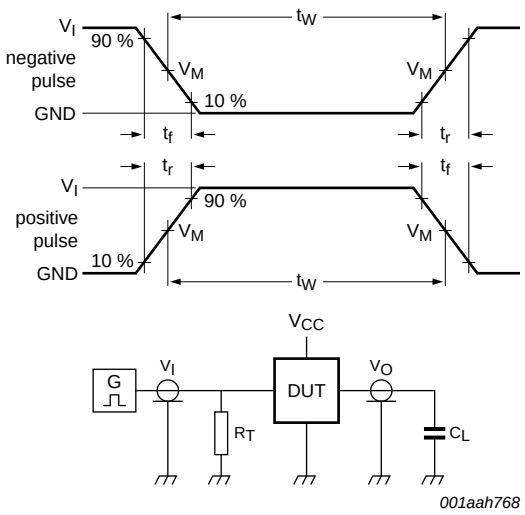



Measurement points are given in Table 8.

**Fig 10. Master reset to output propagation delays, master reset pulse width and master reset to clock recovery time**

**Table 8. Measurement points**

| Type | Input | | Output |
|---|---|---|---|
| | $V_I$ | $V_M$ | $V_M$ |
| 74HC175 | $V_{CC}$ | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT175 | 3 V | 1.3 V | 1.3 V |




Test data is given in Table 9.

Definitions for test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_L$ = Load resistance.

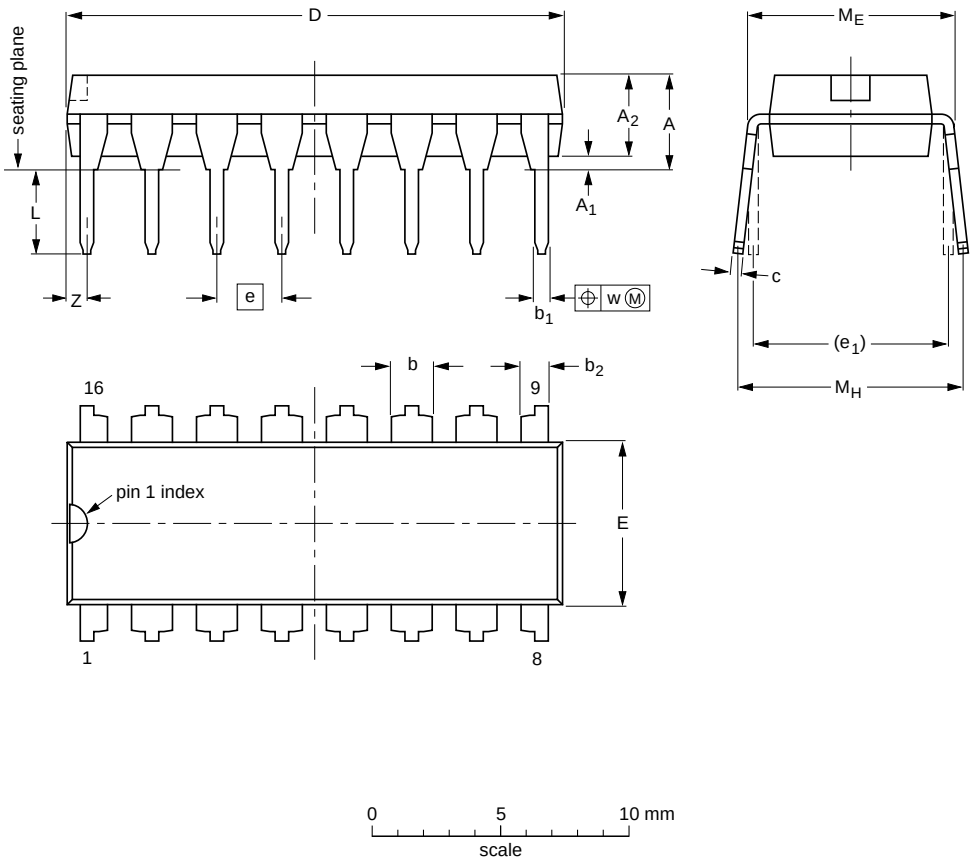
**Fig 11. Test circuit for measuring switching times**

**Table 9. Test data**

| Type | Input | | Load | | Test |
|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | |
| 74HC175 | $V_{CC}$ | 6 ns | 15 pF, 50 pF | 1 kΩ | $t_{PLH}$, $t_{PHL}$ |
| 74HCT175 | 3 V | 6 ns | 15 pF, 50 pF | 1 kΩ | $t_{PLH}$, $t_{PHL}$ |

## 12. Package outline

**DIP16: plastic dual in-line package; 16 leads (300 mil)** **SOT38-4**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.03 |

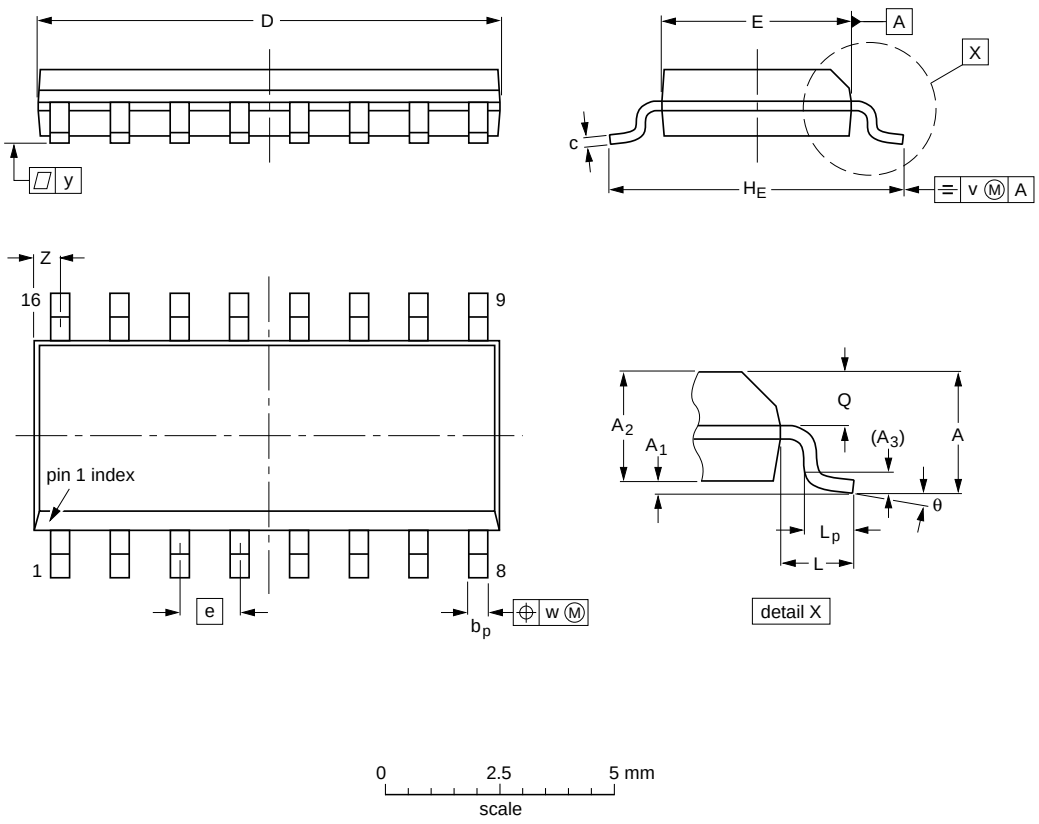
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | ~~95-01-14~~<br>03-02-13 |

**Fig 12. Package outline SOT38-4 (DIP16)**

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

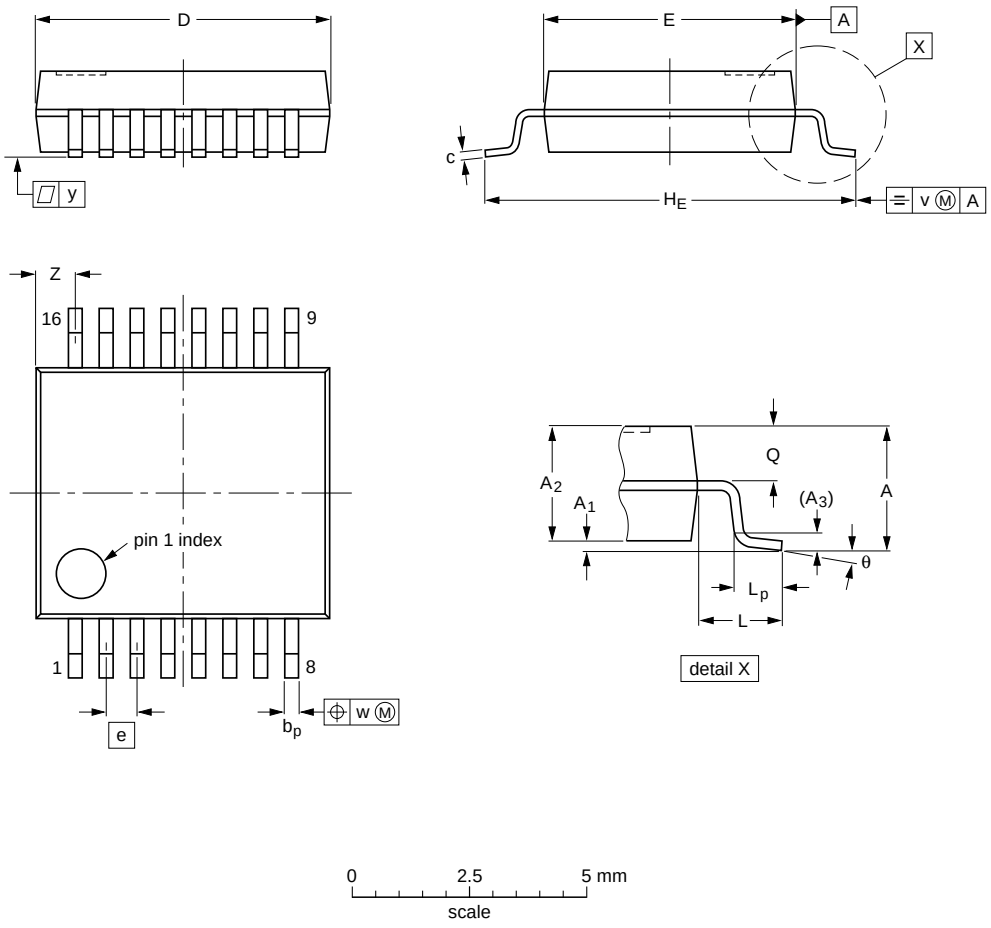
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 13. Package outline SOT109-1 (SO16)**

**SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm** **SOT338-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.00<br>0.55 | $8^o$<br>$0^o$ |

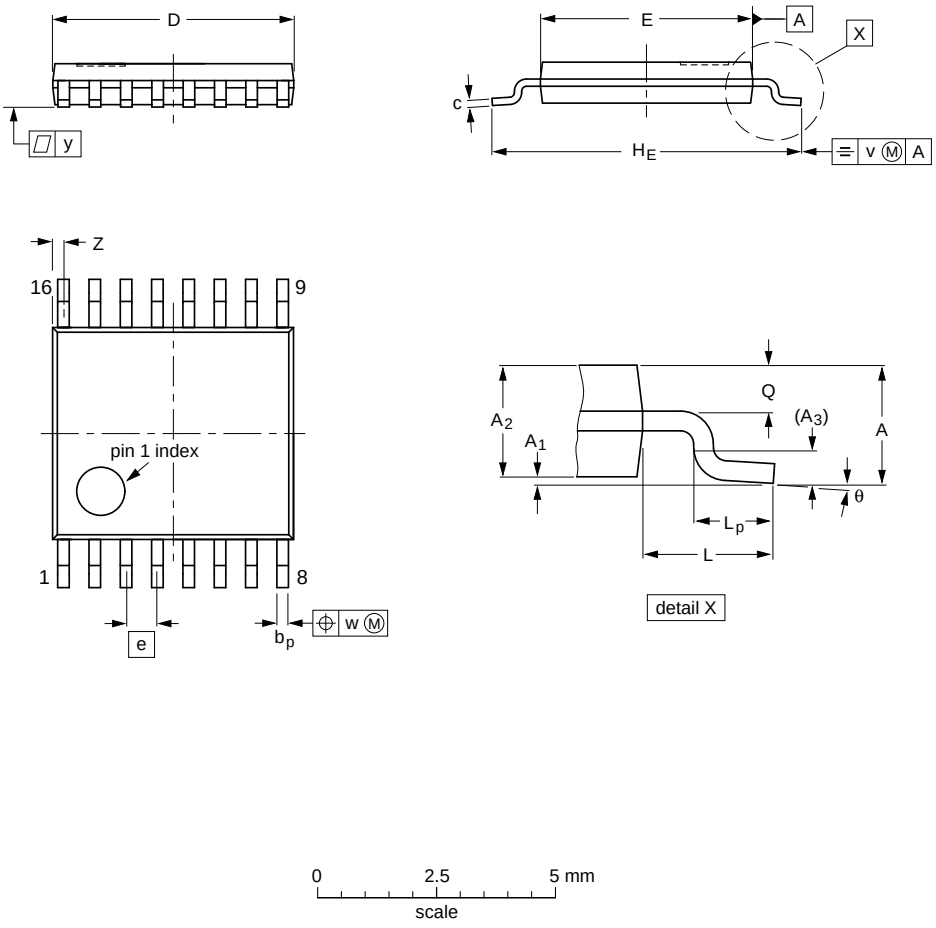
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT338-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 14. Package outline SOT338-1 (SSOP16)**

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 15. Package outline SOT403-1 (TSSOP16)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74HC_HCT175 v.4 | 20140408 | Product data sheet | - | 74HC_HCT175 v.3 |
| Modifications: | • General description corrected (errata). | | | |
| 74HC_HCT175 v.3 | 20140331 | Product data sheet | - | 74HC_HCT175_CNV_2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| 74HC_HCT175_CNV_2 | 19980708 | Product specification | - | - |

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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 17. Contents





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**Date of release: 8 April 2014**
**Document identifier: 74HC_HCT175**