

DATA SHEET

74HCT7273

Octal D-type flip-flop with reset;
positive edge-trigger; open drain
outputs

Product specification
File under Integrated Circuits, IC06

1999 Oct 01

Octal D-type flip-flop with reset; positive edge-trigger; open drain outputs

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FEATURES

- ESD protection:
HBM EIA/JESD22-A114-A
Exceeds 2000 V
MM EIA/JESD22-A115-A
Exceeds 200 V
- Ideal buffer for MOS microprocessor or memory
- Eight positive edge-triggered D-type flip-flops
- Common clock and master reset
- Output capability: standard (open drain)
- I_{CC} category: MSI.

DESCRIPTION

The 74HCT7273 is a high-speed SI-gate CMOS device and is pin compatible with Low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no 7A.

The 74HCT7273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

A LOW level on the \overline{MR} input forces all outputs LOW, independently of the clock or data inputs.

The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

The 74HCT7273 has open-drain N-outputs, which are clamped by a diode connected to V_{CC}. When a HIGH is clocked in the flip-flop, the output comes in the high-impedance OFF-state. The output may now be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, the device must have a pull-up resistor to establish a logic HIGH level.

QUICK REFERENCE DATA

Ground = 0 V; T_{amb} = 25 °C; t_r = t_f = 6.0 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PZL} /t _{PLZ}	propagation delay CP to Q _n \overline{MR} to Q _n	C _L = 50 pF; V _{CC} = 4.5 V	16 23	ns ns
f _{max}	maximum clock frequency		56	MHz
C _I	input capacitance		3.5	pF
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; notes 1 and 2	37	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + \sum (V_0^2/R_L) \times \text{duty factor LOW}$$
where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
R_L = pull-up resistor in MΩ;
V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC} - 1.5 V.

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FUNCTION TABLE

See note 1.

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{\text{MR}}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	Z
Load '0'	H	↑	l	L

Note

- 1. H = HIGH voltage level;
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
- L = LOW voltage level.
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
- Z = high-impedance OFF-state;
- X = don't care;
- ↑ = LOW-to-HIGH CP transition.

ORDERING INFORMATION

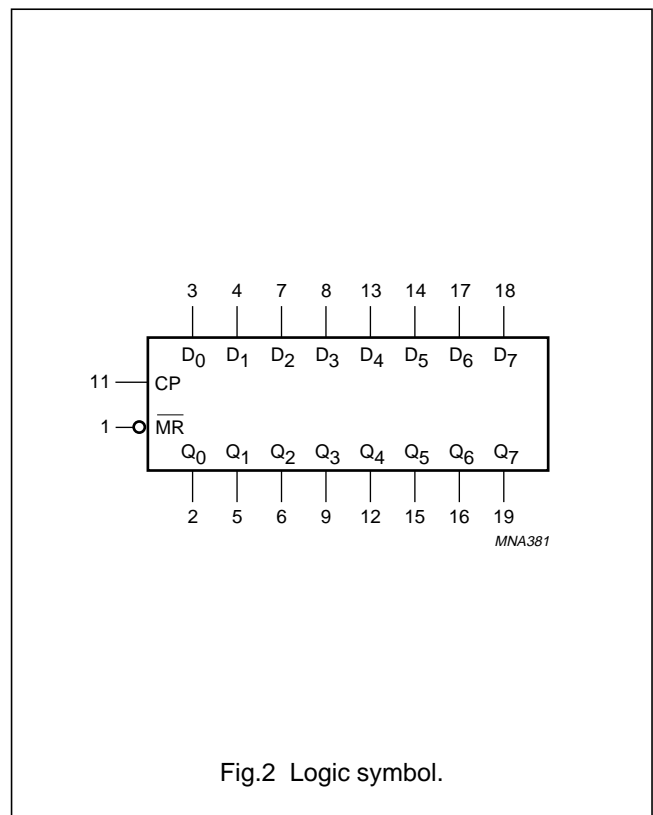
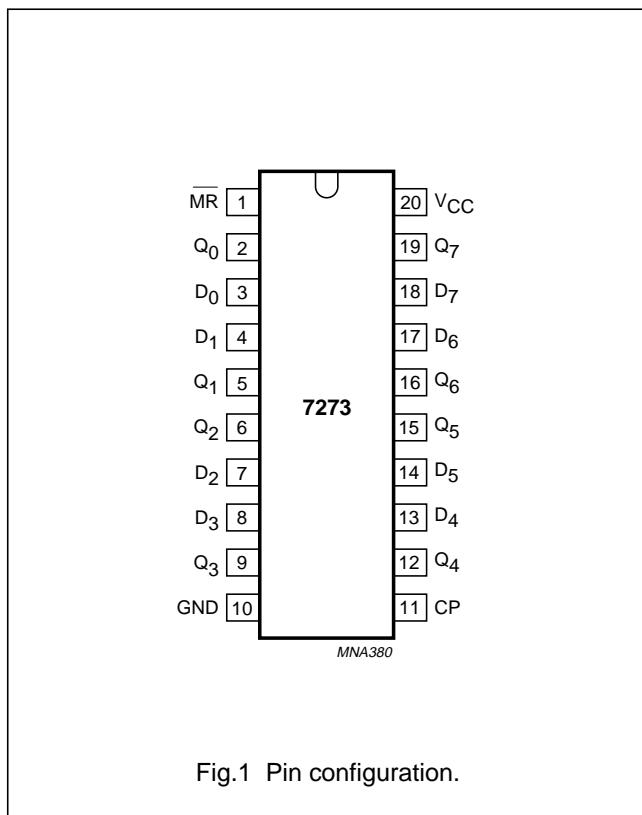
OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGE				
		TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HCT7273D	74HCT7273D	-40 to +125 °C	20	SO	plastic	SOT163-1
74HCT7273N	74HCT7273N		20	DIP	plastic	SOT146-1

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PINNING

PIN	SYMBOL	DESCRIPTION
1	\overline{MR}	asynchronous master reset (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge triggered)
20	V_{CC}	DC supply voltage



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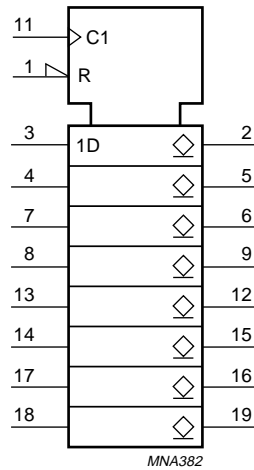


Fig.3 IEC logic symbol.

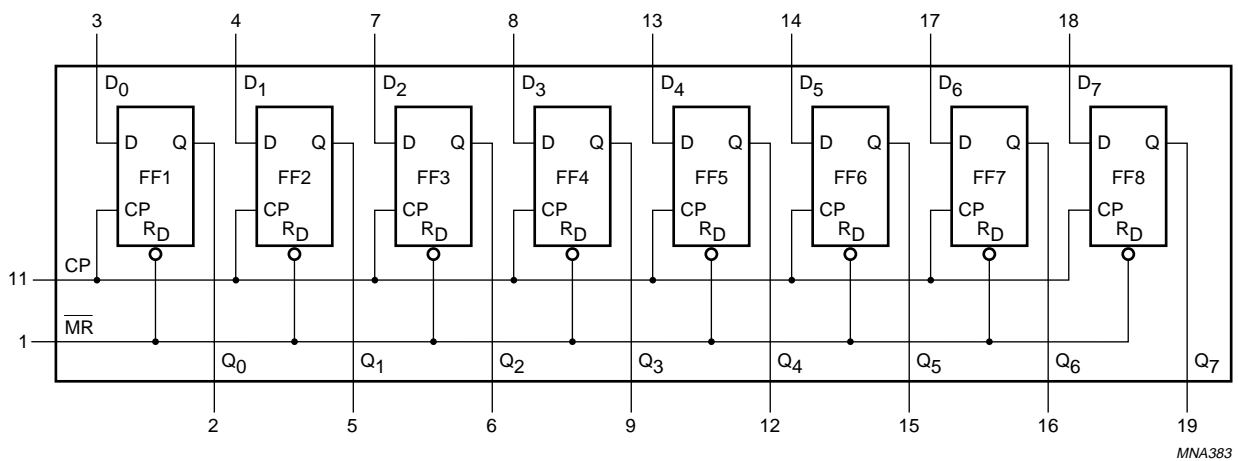


Fig.4 Functional diagram.

Octal D-type flip-flop with reset; positive edge-trigger; open drain outputs

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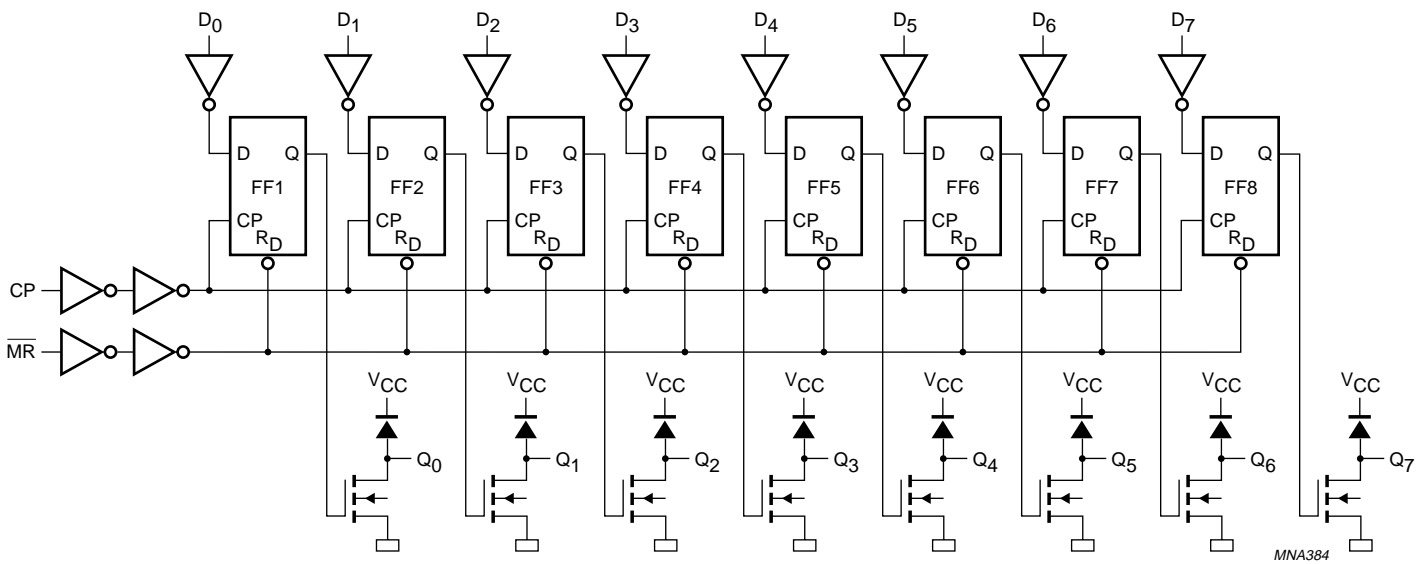


Fig.5 Logic diagram.

Octal D-type flip-flop with reset; positive edge-trigger; open drain outputs

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	TYPE			UNIT
			MIN.	TYP.	MAX.	
V_{CC}	DC supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	–	+85	°C
			–40	–	+125	°C
$t_r, t_f (\Delta t/\Delta f)$	input rise and fall times except for Schmitt-trigger inputs	$V_{CC} = 2.0\text{ V}$	–	6.0	500	ns/V
		$V_{CC} = 4.5\text{ V}$	–	6.0	500	
		$V_{CC} = 6.0\text{ V}$	–	6.0	500	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+7.0	V
V_O	output voltage		–0.5	+7.0	V
I_{IK}	DC input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	–	20	mA
I_{OK}	DC output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	–	±20	mA
I_O	DC output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	–	25	mA
I_{CC}	DC V_{CC} or GND current		–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package plastic DIP plastic mini-pack (SO)	for temperature range: –40 to +125 °C note 1 note 2	–	750	mW
			–	500	
			–	500	

Note

- For DIP package: above 70 °C the value of P_D derates linearly with 12 mW/K.
- For SO package: above 70 °C the value of P_D derates linearly with 8 mW/K.

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DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)						UNIT	
		OTHER	V _{CC} (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	2.0	–	2.0	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	–	0.8	–	0.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 20 μA	4.5	–	0	0.1	–	0.1	–	0.1	V
		V _I = V _{IH} or V _{IL} ; I _O = 4.0 mA	4.5	–	0.15	0.26	–	0.33	–	0.4	V
I _I	input leakage current	V _I = V _{IH} or V _{IL}	5.5	–	–	0.1	–	1.0	–	1.0	μA
I _{OZ}	HIGH level output leakage current	V _I = V _{IL} ; V _O = V _{CC} or GND	4.5 to 5.5	–	–	±0.5	–	±5.0	–	±10.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	8.0	–	80	–	160	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} – 2.1 V other inputs at V _{CC} or GND; I _O = 0; note 1	4.5 to 5.5	–	100	360	–	450	–	490	μA

Note

- The value off additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in Table 1.

Table 1

INPUT	UNIT LOAD COEFFICIENT
$\overline{\text{MR}}$	1.50
CP	1.50
D _n	0.40

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AC CHARACTERISTICS

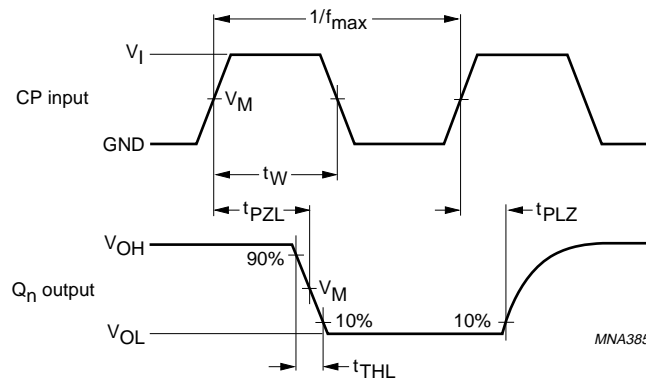
Ground = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)						UNIT	
		WAVEFORMS	V_{CC} (V)	25			-40 to +85		-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.		MAX.
t_{PZL}/t_{PLZ}	propagation delay CP to Q_n	see Figs 6 and 9	4.5	–	16	30	–	38	–	45	ns
t_{PZL}	propagation delay MR to Q_n	see Figs 6 and 9	4.5	–	23	34	–	43	–	51	ns
t_{THL}	output transition time	see Figs 6 and 9	4.5	–	7	15	–	19	–	22	ns
t_{TLH}	output transition time	see Figs 7 and 9	4.5	–	–	110	–	110	–	110	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 9	4.5	16	9	–	20	–	24	–	ns
t_W	master reset pulse width; LOW	see Figs 7 and 9	4.5	16	8	–	20	–	24	–	ns
t_{rem}	removal time MR to CP	see Figs 7 and 9	4.5	10	–2	–	13	–	15	–	ns
t_{su}	set-up time D_n to CP	see Figs 8 and 9	4.5	12	5	–	15	–	18	–	ns
t_h	hold time D_n to CP	see Figs 8 and 9	4.5	3	–4	–	3	–	3	–	ns
f_{max}	maximum clock pulse frequency	see Figs 6 and 9	4.5	30	56	–	24	–	20	–	MHz

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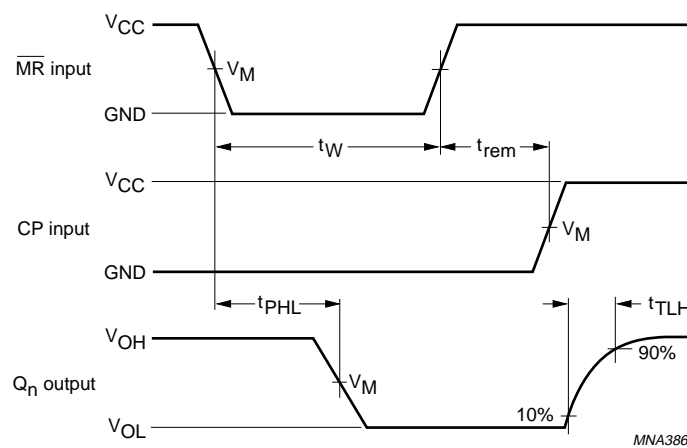
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AC WAVEFORMS



$V_M = 1.3\text{ V}$; $V_I = \text{GND to } 3\text{ V}$.

Fig.6 The clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and maximum clock pulse frequency.

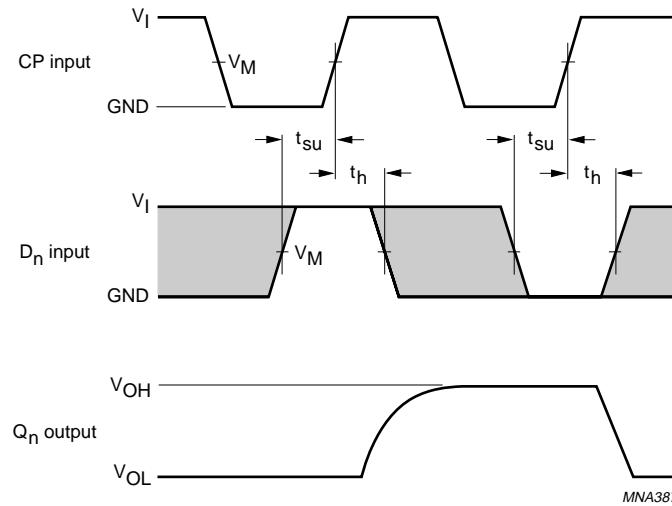


$V_M = 1.3\text{ V}$; $V_I = \text{GND to } 3\text{ V}$.

Fig.7 Master reset ($\overline{\text{MR}}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP).

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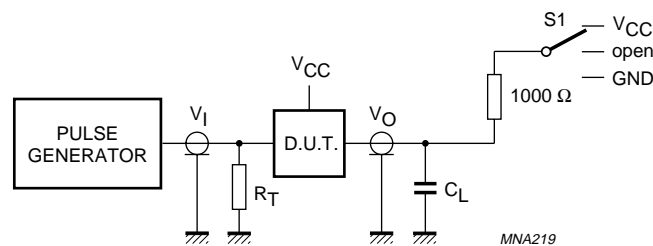
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V_M = 1.3 V; V_I = GND to 3 V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.8 Data set-up and hold times for the data input (D_n).



TEST	S1
t _{PLH} /t _{PHL}	open
t _{PLZ} /t _{PZL}	V _{CC}
t _{PHZ} /t _{PZH}	GND

Definitions for test circuit.

C_L = load capacitance including jig and probe capacitance (See Chapter "AC characteristics").

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.9 Load circuit for switching times.

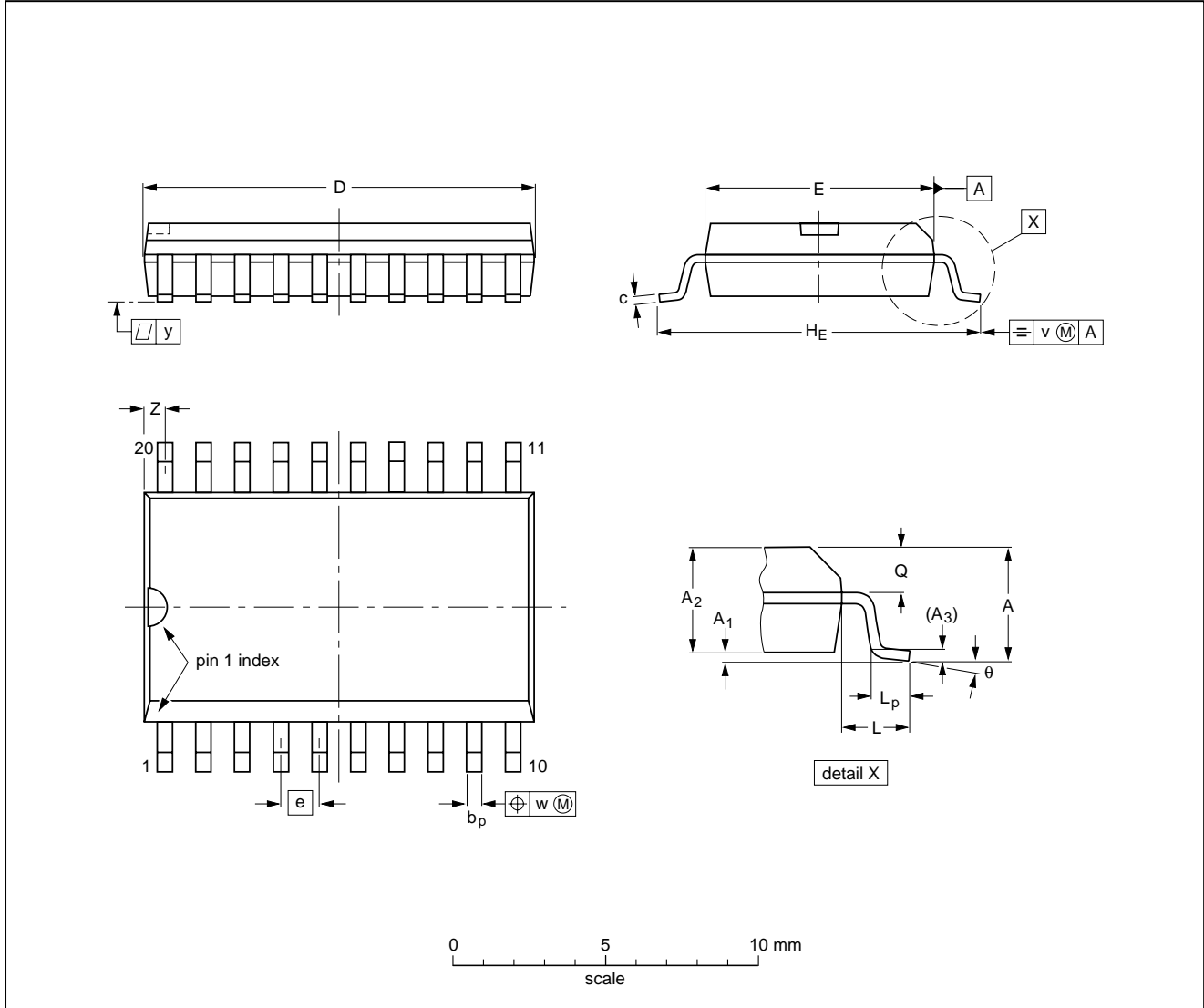
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PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

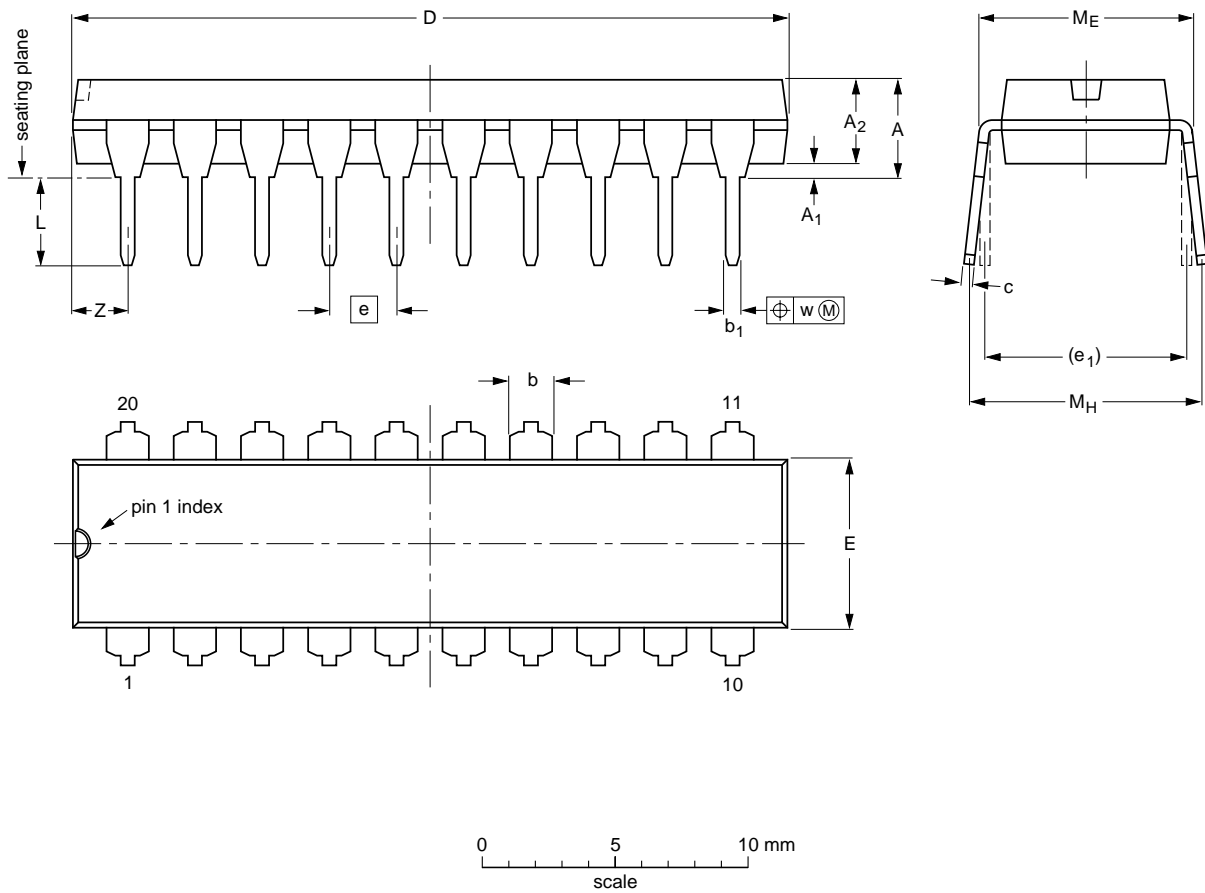
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

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Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable ⁽¹⁾

Note

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax.+381 11 63 5777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

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Printed in The Netherlands

245002/01/pp20

Date of release: 1999 Oct 01

Document order number: 9397 750 05733

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